1.1 Scope.

This specification covers the detail requirements for a voltage-to-frequency with full-scale range of up to 2MHz.

1.2 Part Number.

The complete part numbers per Table 1 of this specification is as follows:

Device	Part Number[1]
−1	AD652S(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Lead Ceramic DIP
E	E-20A	20-Terminal Leadless Chip Carrier

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Total Supply Voltage $+V_S$ to $-V_S$ 36V
Open Collector Output Voltage Above Digital Ground 36V
Open Collector Output Current 50mA
Amplifier Short Circuit to Ground . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 25°C/W for Q-16
θ_{JA} = 100°C/W for Q-16
θ_{JC} = 35°C/W for E-20A
θ_{JA} = 120°C/W for E-20A

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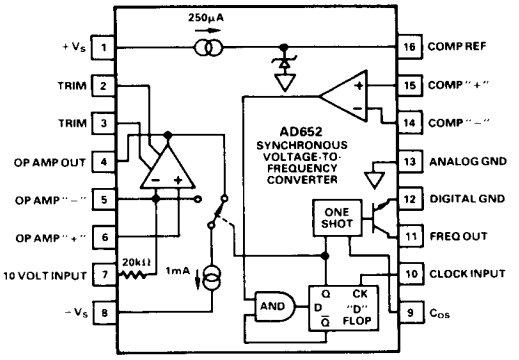
Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition[1]	Units
Linearity Error[2]	LE	−1	0.02	0.02		f_{CLOCK} = 1MHz, V_{IN} = 0.01, 0.1; 1.0 to 9.4V in 1.05V Steps	% of FS max
			0.05	0.05		f_{CLOCK} = 4MHz, V_{IN} = 0.01, 0.1; 1.0 to 9.4V in 1.05V Steps	% of FS max
Gain Error[2]	A_E	−1	1	1		f_{CLOCK} = 1MHz, V_{IN} = 0.01, 9.4V	% of FS max
			1.5	1.5		f_{CLOCK} = 4MHz, V_{IN} = 0.01, 9.4V	% of FS max
Gain Temperature Coefficient	TCA	−1			50	f_{CLOCK} = 1MHz, V_{IN} = 0.01, 9.4V	± ppm/°C max
					75	f_{CLOCK} = 4MHz, V_{IN} = 0.01, 9.4V	± ppm/°C max
Power Supply Rejection Ratio	P_{SRR}	−1	0.01	0.01		12V ≤ V_S ≤ 18V, f_{CLOCK} = 4MHz	%/V
Offset Voltage[3] (Transfer Function, RTI)	V_{IO}	−1	3	3		f_{CLOCK} = 1MHz, V_{IN} = 0.01, 9.4V f_{CLOCK} = 4MHz, V_{IN} = 0.01, 9.4V	± mV max
Input Offset Voltage Temperature Coefficient (RTI)	TCV_{IO}	−1			50	f_{CLOCK} = 1MHz	± µV/°C max
Input Resistor	R_I	−1	20.2	20.2			kΩ max
			19.8	19.8			kΩ min
Input Resistor Temperature Coefficient	TCR_{IN}	−1			100		± ppm/°C max
Op Amp Input Bias Current	I_{IB}	−1	20	20		V_{IN} = 0V, Inverting Input	± nA max
			50	50		V_{IN} = 0V, Noninverting Input	nA max
Op Amp Input Offset Current	I_{OS}	−1	70	70		V_{IN} = 0V	nA max
Op Amp Input Offset Voltage	V_{OS}	−1	3	3		V_{IN} = 0V	± mV max
Op Amp Output Voltage Range	V_R	−1	11	11		V_S = ± 15V, Op-Amp Railed High	V min
			−1	−1		V_S = ± 15V, Op-Amp Railed Low	V max
Max Clock Frequency	f_{CLOCK}	−1	4	4		V_{IN} = 0.01, 9.4V	MHz min
Clock Threshold Voltage	V_{CT}	−1			2.0	Referred to Pin 12	V max
					0.8	Referred to Pin 12	V min
Clock Input Current	I_C	−1	20	20		Pin 10 = 0V dc	µA max
Low Level Output Voltage	V_{OL}	−1	0.8	0.8		I_{OUT} = 15mA	V max
			0.4	0.4		I_{OUT} = 10mA	V max
					0.4	I_{OUT} = 8.0mA	V max
Leakage Current	I_L	−1	10	10		V_{OUT} = 36V	µA max
Delay Time Positive Clock Edge to Output Pulse	t_D	−1	150	150		f_{CLOCK} = 200kHz Pin 9 to Pin 1	ns min
			250	250		f_{CLOCK} = 200kHz Pin 9 to Pin 1	ns max
Output Pulse Width	t_{PW}	−1	1	1		C_{OS} = 300pF	µs min
			2	2		C_{OS} = 300pF	µs max
Reference Voltage	V_{REF}	−1	5.05	5.05		I_{REF} = 0mA	V max
			4.95	4.95		I_{REF} = 0mA	V min
Reference Voltage Temperature Coefficient	TCV_{REF}	−1	100		100	I_{REF} = 0mA	± ppm/°C max
Quiescent Current	$+I_{SS}$	−1	15	15		V_S = ± 15V, V_{IN} = 0.1V	mA max
	$-I_{SS}$	−1	15	15		V_S = ± 15V, V_{IN} = 0.1V	− mA max

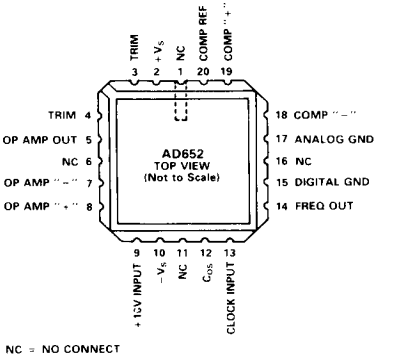
NOTES
[1]V_S = ± 15V, unless otherwise specified. 0.1µF decoupling capacitors from + V_S to ground and − V_S to ground.
[2]Nonlinearity is defined as the deviation from a straight line from zero to full scale, expressed as a fraction of full scale.
[3]Offset is guaranteed adjustable to zero using a 10kΩ potentiometer on Pins 2 and 3 with the wiper connected to + V_S through a 250kΩ resistor.

3.2.1 Functional Block Diagram and Terminal Assignments.

"Q" PACKAGE (16-LEAD DIP)



"E" PACKAGE (20-TERMINAL LCC)



NC = NO CONNECT

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).