ANALOG DEVICES

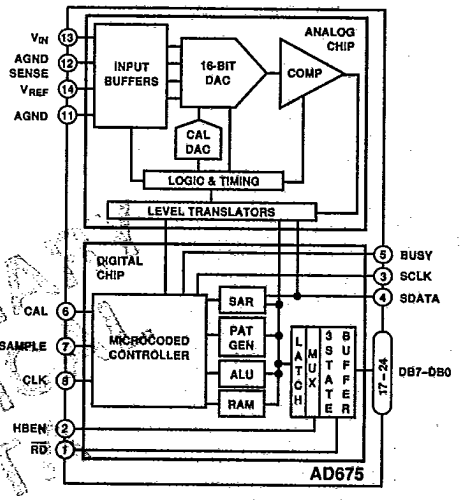
16-Bit 100 kSPS Sampling ADC

T-51-10-16 **AD675**

2

FEATURES
AC and DC Specified
Autocalibrating
On-Chip Sample-Hold Function
Two-Byte or Serial Output
16-Bits No Missing Codes
±1 LSB INL
0.001% THD
90 dB S/(N+D)
1 MHz Full Power Bandwidth
24-Pin "Skinny" DIP Package

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD675 is a multipurpose 16-bit parallel output analog-to-digital converter which utilizes a switched capacitor/charge redistribution architecture to achieve a 100 kSPS conversion rate (10 µs total conversion time). Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration.

The AD675 includes a sample-hold amplifier (SHA) and microprocessor compatible bus interface with three-state output buffers and two-byte read. Output data is also available in serial format.

The AD675 circuitry is segmented onto two monolithic chips—a digital control chip fabricated on Analog Devices' DSP CMOS process and an analog ADC chip fabricated on our BiMOS II process. Both chips are contained in a single package.

The AD675 is specified for ac (or "dynamic") parameters such as S/N+D Ratio, THD and IMD which are important in signal processing applications. In addition, dc parameters are specified which are important in measurement applications.

The AD675 operates from +5 V and ±12 V supplies and typically consumes 235 mW during conversion. The digital supply (V_{DD}) is separated from the analog supplies (V_{CC}, V_{EE}) for reduced digital crosstalk. An analog ground sense is provided for the analog input. Separate analog and digital grounds are also provided.

The AD675 is available in a 24-pin plastic "skinny" DIP or 24-pin side-brazed "skinny" DIP ceramic package. Screening to MIL-STD-883C Class B is available.

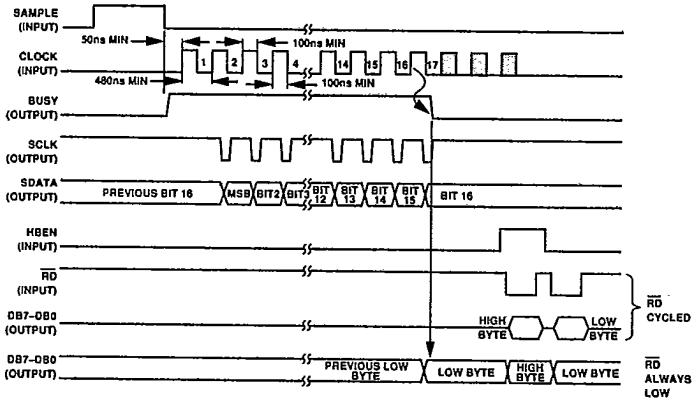
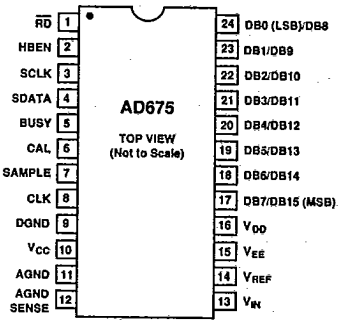


Figure 1. Conversion Timing

PIN CONFIGURATION



AD675—SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = + 12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter			Min	Typ	Max	Units
TOTAL HARMONIC DISTORTION (THD)						
−0.05 dB Input				−98	−90	dB
				0.0015	0.003	%
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/(N+D))						
−0.05 dB Input, 50 kHz Bandwidth			87	90		dB
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT				−100	−92	dB
INTERMODULATION DISTORTION (IMD)[2]						
2nd Order Products				−102		dB
3rd Order Products				−98		dB
FULL POWER BANDWIDTH				1		MHz
TEMPERATURE RANGE			−40		+85	°C
ACCURACY						
Resolution			16			Bits
Integral Nonlinearity (INL)					±1	LSB
Differential Nonlinearity (DNL)—No Missing Codes			16			Bits
Bipolar Zero Error[3]					±1	LSB
Gain Error[3]					0.003	% FSR
Temperature Drift						
Bipolar Zero				0.002		% FSR
Gain				0.002		% FSR
VOLTAGE REFERENCE INPUT RANGE[1] (V_{REF})			5.0		10	V
ANALOG INPUT						
Input Range (V_{IN})					$\pm V_{REF}$	V
Input Capacitance During Sample				50		pF
Aperture Delay				6		ns
Aperture Jitter				100		ps
POWER SUPPLIES						
Power Supply Rejection						
V_{CC} = +12 V ± 5%				±1	±2	LSB
V_{EE} = −12 V ± 5%				±1	±2	LSB
V_{DD} = +5 V ± 10%				±1	±2	LSB
Operating Current						
I_{CC}				9	12	mA
I_{EE}				9	12	mA
I_{DD}				3	12	mA
Power Consumption				235	350	mW
LOGIC INPUTS						
V_{IH}	High Level Input Voltage		2.4			V
V_{IL}	Low Level Input Voltage		−0.3		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = V_{DD}$	−10		+10	μA
I_{IL}	Low Level Input Current	V_{IL} = 0 V	−10		+10	μA
C_{IN}	Input Capacitance			10		pF
LOGIC OUTPUTS						
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	V_{DD} −1 V			V
		= 0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA			0.4	V
I_{OZ}	High-Z Leakage Current	V_{IN} = 0 or V_{DD}	−10		+10	μA
V_{OL}	High-Z Output Capacitance				10	pF

NOTES
[1]Conversion rate = 100 kSPS. Values are post calibration.
[2]fa = 1008 Hz, fb = 1055 Hz.
[3]Values shown apply to any temperature from T_{MIN} to T_{MAX} after calibration at that temperature.
Specifications subject to change without notice.