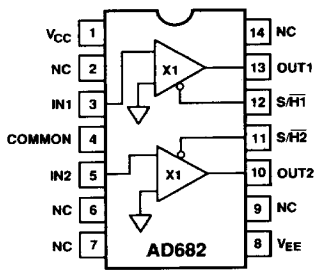
Two-Channel 700 ns Sample-and-Hold Amplifier

AD682*

FEATURES

Two Matched Sample-and-Hold Amplifiers
Fully Specified and Tested Hold Mode Distortion
Acquisition Time to 0.01%: 700 ns Maximum
Independent Inputs, Outputs and Control Pins
Low Power Dissipation: 190 mW
Low Droop Rate: 0.01 μV/μs
Total Harmonic Distortion: −80 dB Maximum
Aperture Jitter: 75 ps Maximum
Internal Hold Capacitors
Self-Correcting Architecture
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

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PRODUCT DESCRIPTION

The AD682 is a two-channel high speed monolithic sample-and-hold amplifier (SHA). The AD682 guarantees a maximum acquisition time of 700 ns to 0.01% over temperature. Interchannel characteristics are fully specified and tested. The AD682 is also specified and tested for hold mode total harmonic distortion and hold mode signal-to-noise and distortion. The AD682 is configured as two independent unity gain amplifiers. The AD682 uses a self-correcting architecture that minimizes hold mode errors and insures accuracy over temperature. The AD682 is self-contained and requires no external components or adjustments.

The AD682 is ideal for systems demanding interchannel and hold mode characteristic requirements, such as in data acquisition systems and in-phase (I) and quadrature (Q) modulated systems. The independent inputs, outputs and controls allow maximum user configuration flexibility. The AD682 is ideal for 12- and 14-bit high speed analog-to-digital converters.

The AD682 is manufactured on a BiMOS process which merges high performance bipolar circuitry with low power CMOS to provide an accurate, high speed, low power SHA.

The AD682 is specified for three temperature ranges. The J grade device is specified for operation from 0°C to 70°C, the A grade from −40°C to +85°C and the S grade from −55°C to +125°C. The J and A grades are available in 14-pin plastic DIPs. The S grade is available in a 14-pin cerdip package.

*Protected by Patent Number 4,962,325.

PRODUCT HIGHLIGHTS

1. Fast acquisition time (700 ns) and low aperture jitter (75 ps) make the AD682 the best choice for multiple channel data acquisition systems.
2. Monolithic construction insures excellent interchannel matching, while testing guarantees the fully specified performance.
3. Independent inputs, outputs and sample-and-hold controls allow user flexibility.
4. Low droop (0.01 μV/μs) and internally compensated hold mode error results in superior system accuracy.
5. Fully specified and tested hold mode distortion and signal-to-noise and distortion guarantees the AD682's performance in sampled data systems.
6. The AD682's fast settling time and low output impedance make it ideal for driving high speed analog-to-digital converters such as the AD578, AD674B, AD774B, AD7572 and the AD7672.
7. The AD682 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD682/883B data sheet for detailed specifications.

AD682—SPECIFICATIONS

DC SPECIFICATIONS (T_{min} to T_{max} with V_{CC} = +12 V ± 10%, V_{EE} = −12 V ± 10%, C_L = 20 pF, unless otherwise specified)

Parameter	AD682J Min	AD682J Typ	AD682J Max	AD682A Min	AD682A Typ	AD682A Max	AD682S Min	AD682S Typ	AD682S Max	Units
SAMPLING CHARACTERISTICS										
Acquisition Time										
10 V Step to 0.01%		600	700		600	700		600	700	ns
10 V Step to 0.1%		500	600		500	600		500	600	ns
Small Signal Bandwidth		4			4			4		MHz
Full Power Bandwidth		1			1			1		MHz
HOLD CHARACTERISTICS										
Effective Aperture Delay (25°C)	−35	−25	−15	−35	−25	−15	−35	−25	−15	ns
Aperture Jitter (25°C)		50	75		50	75		50	75	ps
Hold Settling (to 1 mV, 25°C)		250	500		250	500		250	500	ns
Droop Rate		0.01	1		0.01	1		0.01	1	μV/μs
Feedthrough (25°C)										
(V_{IN} = ±5 V, 100 kHz)		−90			−90			−90		dB
ACCURACY CHARACTERISTICS[1]										
Hold Mode Offset	−4	−1	+3	−4	−1	+3	−4	−1	+3	mV
Hold Mode Offset Drift		10			10			10		μV/°C
Sample Mode Offset		50	200		50	200		50	200	mV
Nonlinearity		±0.002	±0.003		±0.002	±0.003		±0.003	±0.005	% FS
Gain Error		±0.03	±0.05		±0.03	±0.05		±0.03	±0.05	% FS
OUTPUT CHARACTERISTICS										
Output Drive Current	−5		+5	−5		+5	−5		+5	mA
Output Resistance, DC		0.3	0.5		0.3	0.5		0.3	0.5	Ω
Total Output Noise (DC to 5 MHz)		150			150			150		μV rms
Sampled DC Uncertainty		85			85			85		μV rms
Hold Mode Noise (DC to 5 MHz)		125			125			125		μV rms
Short Circuit Current										
Source		20			20			20		mA
Sink		10			10			10		mA
INPUT CHARACTERISTICS										
Input Voltage Range	−5		+5	−5		+5	−5		+5	V
Bias Current		100	250		100	250		100	250	nA
Input Impedance		50			50			50		MΩ
Input Capacitance		2			2			2		pF
DIGITAL CHARACTERISTICS										
Input Voltage Low			0.8			0.8			0.8	V
Input Voltage High	2.0			2.0			2.0			V
Input Current High (V_{IN} = 5 V)		2	10		2	10		2	10	μA
POWER SUPPLY CHARACTERISTICS										
Operating Voltage Range	±10.8	±12	±13.2	±10.8	±12	±13.2	±10.8	±12	±13.2	V
Supply Current		8	12.5		8	12.5		8	13	mA
+PSRR (+12 V ± 10%)	70	80		70	80		70	80		dB
−PSRR (−12 V ± 10%)	65	75		65	75		65	75		dB
Power Consumption		190	300		190	300		190	320	mW
TEMPERATURE RANGE										
Specified Performance	0		+70	−40		+85	−55		+125	°C

NOTE
[1]Specified and tested over an input range of ±5 V.
Specifications subject to change without notice.

INTERCHANNEL SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ±10%, V_{EE} = −12 V ±10%, C_L = 20 pF, unless otherwise specified)

Parameter	AD682J Min	AD682J Typ	AD682J Max	AD682A Min	AD682A Typ	AD682A Max	AD682S Min	AD682S Typ	AD682S Max	Units
INTERCHANNEL ISOLATION (V_{IN} = ±5 V, 100 kHz)	90	96		90	96		90	96		dB
INTERCHANNEL APERTURE OFFSET		150	300		150	300		150	300	ps
INTERCHANNEL OFFSET		0.1	1.5		0.1	1.5		0.1	1.5	mV

HOLD MODE AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ±10%, V_{EE} = −12 V ±10%, C_L = 20 pF, unless otherwise specified)[1]

Parameter	AD682J Min	AD682J Typ	AD682J Max	AD682A Min	AD682A Typ	AD682A Max	AD682S Min	AD682S Typ	AD682S Max	Units
TOTAL HARMONIC DISTORTION										
F_{IN} = 10 kHz		−90	−80		−90	−80		−90	−80	dB
F_{IN} = 50 kHz		−73			−73			−73		dB
F_{IN} = 100 kHz		−68			−68			−68		dB
SIGNAL-TO-NOISE AND DISTORTION										
F_{IN} = 10 kHz	72	78		72	78		72	78		dB
F_{IN} = 50 kHz		73			73			73		dB
F_{IN} = 100 kHz		67			67			67		dB
INTERMODULATION DISTORTION										
F_{IN1} = 49 kHz, F_{IN2} = 50 kHz										
2nd Order Products		−77			−77			−77		dB
3rd Order Products		−78			−78			−78		dB

NOTE
[1]F_{IN} amplitude = 0 dB and F_{SAMPLE} = 500 kHz unless otherwise indicated.

Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in **boldface** are tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Spec	With Respect to	Min	Max	Unit
V_{CC}	Common	−0.3	+15	V
V_{EE}	Common	−15	+0.3	V
Control Inputs	Common	−0.5	+7	V
Analog Inputs	Common	−12	+12	V
Output Short Circuit to Ground, V_{CC}, or V_{EE}		Indefinite		
Maximum Junction Temperature			+175	°C
Storage		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C
Power Dissipation			340	mW

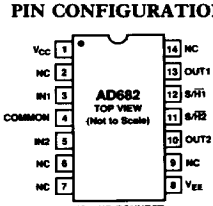
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
AD682JN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD682AN	−40°C to +85°C	14-Pin Plastic DIP	N-14
AD682SQ	−55°C to +125°C	14-Pin Cerdip	Q-14

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD682/883B data sheet.
[2]N = Plastic DIP; Q = Cerdip. For outline information see Package Information section.

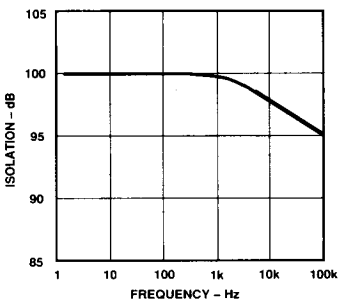
PIN CONFIGURATION



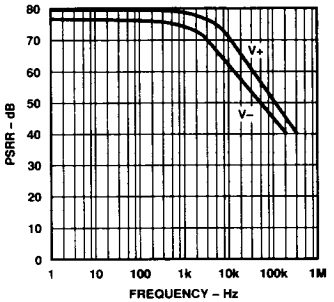
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.

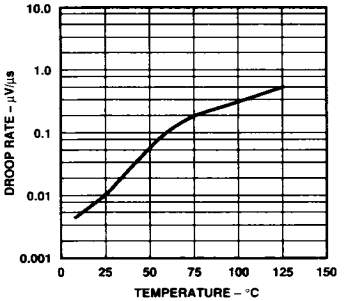
AD682—Typical Characteristics



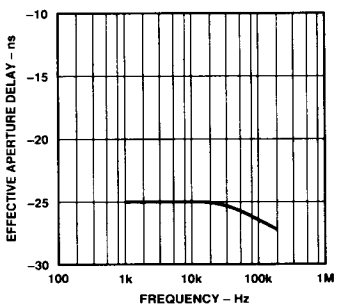
Interchannel Isolation vs. Frequency



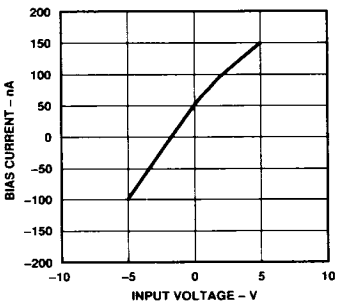
Power Supply Rejection Ratio vs. Frequency



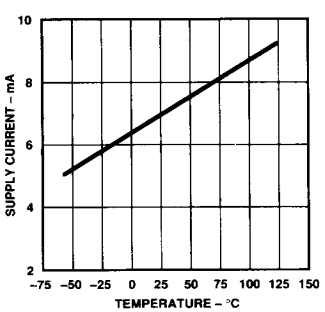
Droop Rate vs. Temperature, V_{IN} = 0 V



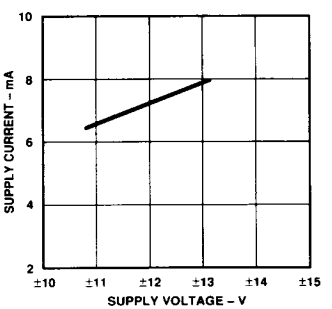
Effective Aperture Delay vs. Frequency



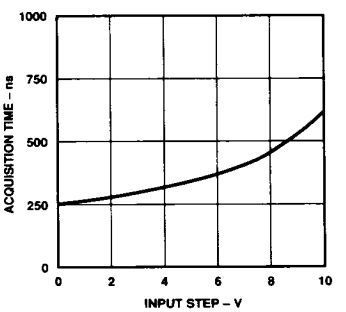
Bias Current vs. Input Voltage



Supply Current vs. Temperature



Supply Current vs. Supply Voltage



Acquisition Time (to 0.01%) vs. Input Step Size

DEFINITIONS OF SPECIFICATIONS

Acquisition Time – The length of time that the SHA must remain in the sample mode in order to acquire a full scale input step to a given level of accuracy.

Small Signal Bandwidth – The frequency at which the held output amplitude is 3 dB below the input amplitude, under an input condition of a 100 mV p–p sine wave.

Full Power Bandwidth – The frequency at which the held output amplitude is 3 dB below the input amplitude, under an input condition of a 10 V p–p sine wave.

Effective Aperture Delay – The difference between the switch delay and the analog delay of the SHA channel. A negative number indicates that the analog portion of the overall delay is greater than the switch portion. This effective delay represents the point in time, relative to the hold command, that the input signal will be sampled.

Aperture Jitter – The variations in delay for successive samples. Aperture jitter puts an upper limit on the maximum frequency that can be accurately sampled.

Hold Settling Time – The time required for the output to settle to within a specified level of accuracy of its final held value after the hold command has been given.

Droop Rate – The drift in output voltage while in the hold mode.

Feedthrough – The attenuated version of a changing input signal that appears at the output when the SHA is in the hold mode.

Hold Mode Offset – The difference between the input signal and the held output. This offset term applies only in the hold mode and includes the error caused by charge injection and all other internal offsets. It is specified for an input of 0 V.

Tracking Mode Offset – The difference between the input and output signals when the SHA is in the track mode.

Nonlinearity – The deviation from a straight line on a plot of input vs. (held) output as referenced to a straight line drawn between end points, over an input range of –5 V and +5 V.

Gain Error – Deviation from a gain of +1 on the transfer function of input vs. held output.

Interchannel Isolation – The level of crosstalk between adjacent channels while in the sample (track) mode with a full-scale 100 kHz input signal.

Interchannel Aperture Offset – The variation in aperture time between the two channels for a simultaneous hold command.

Interchannel Offset – The difference in hold mode offset between the two SHA channels.

Power Supply Rejection Ratio – A measure of change in the held output voltage for a specified change in the positive or negative supply.

Sampled DC Uncertainty – The internal rms SHA noise that is sampled onto the hold capacitor.

Hold Mode Noise – The rms noise at the output of the SHA while in the hold mode, specified over a given bandwidth.

Total Output Noise – The total rms noise that is seen at the output of the SHA while in the hold mode. It is the rms summation of the sampled dc uncertainty and the hold mode noise.

Output Drive Current – The maximum current the SHA can source (or sink) while maintaining a change in hold mode offset of less than 2.5 mV.

Signal-to-Noise and Distortion (S/N+D) Ratio – S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

Total Harmonic Distortion (THD) – THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal.

Intermodulation Distortion (IMD) – With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequency of mfa±nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa+fb) and (fa–fb), and the third order terms are (2fa+fb), (2fa–fb), (fa+2fb) and (fa–2fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude, and peak value of their sums is –0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

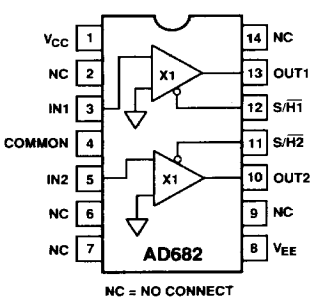
FUNCTIONAL DESCRIPTION

The AD682 is a complete dual sample-and-hold amplifier that provides high speed sampling to 12-bit accuracy in less than 700 ns.

The AD682 is completely self-contained, including on-chip hold capacitors, and requires no external components or adjustments to perform the sampling function. Each SHA channel can operate independently, having its own input, output and sample/hold command. Both inputs and outputs are treated as single-ended signals, referred to common.

The AD682 utilizes a proprietary circuit design which includes a self-correcting architecture. This sample-and-hold circuit corrects for internal errors after the hold command has been given, by compensating for amplifier gain and offset errors, and charge injection errors. Due to the nature of the design, the SHA output in the sample mode is not intended to provide an accurate representation of the input. However, in hold mode, the internal circuitry is reconfigured to produce an accurately held version of the input signal. Below is a block diagram of the AD682.

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

DYNAMIC PERFORMANCE

The AD682 is compatible with 12-bit A-to-D converters in terms of both accuracy and speed. The fast acquisition time, fast hold settling time and good output drive capability allow the AD682 to be used with high speed, high resolution A-to-D converters like the AD674B, AD774B and AD7672. The AD682's fast acquisition time provides high throughput rates for multichannel data acquisition systems. Typically, the sample and hold can acquire a 10 V step in less than 600 ns. Figure 1 shows the settling accuracy as a function of acquisition time.

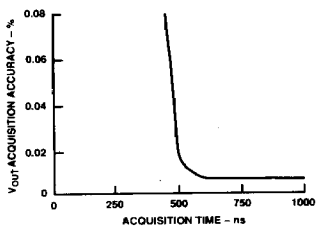


Figure 1. V_{OUT} Settling vs. Acquisition Time

The hold settling determines the required time, after the hold command is given, for the output to settle to its final specified accuracy. The typical settling behavior of the AD682 is shown in Figure 2. The settling time of the AD682 is sufficiently fast to allow the SHA, in most cases, to directly drive an A-to-D converter without the need for an added "start convert" delay.

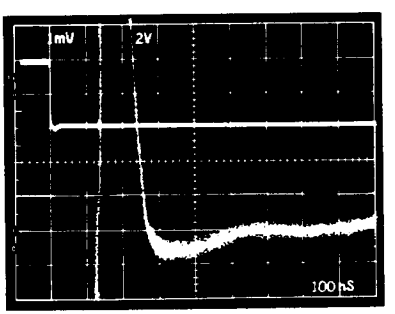


Figure 2. Typical AD682 Hold Mode

HOLD MODE OFFSET

The dc accuracy of the AD682 is determined primarily by the hold mode offset. The hold mode offset refers to the difference between the final held output voltage and the input signal at the time the hold command is given. The hold mode offset arises from a voltage error introduced onto the hold capacitor by charge injection of the internal switches. The nominal hold mode offset is specified for a 0 V input condition. Over the input range of −5 V to +5 V, the AD682 is also characterized for an effective gain error and nonlinearity of the held value, as shown in Figure 3. As indicated by the AD682 specifications, the hold mode offset is very stable over temperature.

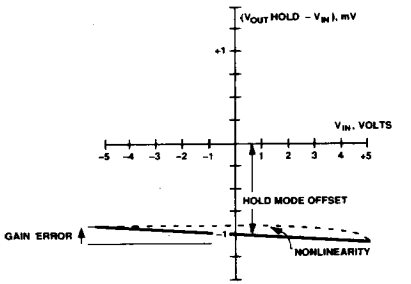


Figure 3. Hold Mode Offset, Gain Error and Nonlinearity

For applications where it is important to obtain zero offset, the hold mode offset may be nulled externally at the input to the A-to-D converter. Adjustment of the offset may be accomplished through the A-to-D itself or by an external amplifier with offset nulling capability (e.g., AD711). The offset will change less than 0.5 mV over the specified temperature range.

SUPPLY DECOUPLING AND GROUNDING CONSIDERATIONS

As with any high speed, high resolution data acquisition system, the power supplies should be well regulated and free from excessive high frequency noise (ripple). The supply connection to the AD682 should also be capable of delivering transient currents to the device. To achieve the specified accuracy and dynamic performance, decoupling capacitors must be placed directly at both the positive and negative supply pins to common. Ceramic type 0.1 μF capacitors should be connected from V_{CC} and V_{EE} to common.

The AD682 does not provide separate analog and digital ground leads as is the case with most A-to-D converters. The common pin is the single ground terminal for the device. It is the reference point for the sampled input voltage and the held output voltage and also the digital ground return path. The common pin should be connected to the reference (analog) ground of the A-to-D converter with a separate ground lead. Since the analog and digital grounds in the AD682 are connected internally, the common pin should also be connected to the digital ground, which is usually tied to analog common at the A-to-D converter. Figure 4 illustrates the recommended decoupling and grounding practice.

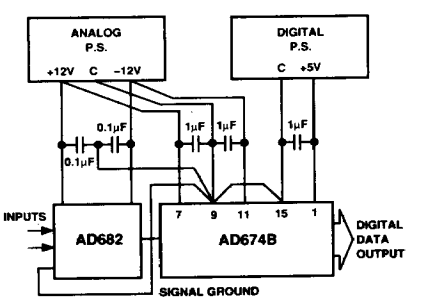


Figure 4. Basic Grounding and Decoupling Diagram

NOISE CHARACTERISTICS

Designers of data conversion circuits must also consider the effect of noise sources on the accuracy of the data acquisition system. A sample-and-hold amplifier that precedes the A-to-D converter introduces some noise and represents another source of uncertainty in the conversion process. The noise from the AD682 is specified as the total output noise, which includes both the sampled wideband noise of the SHA in addition to the band limited output noise. The total output noise is the rms sum of the sampled dc uncertainty and the hold mode noise. A plot of the total output noise vs. the equivalent input bandwidth of the converter being used is given in Figure 5.

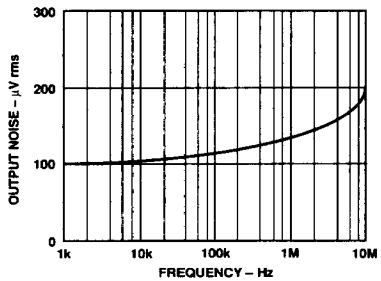


Figure 5. RMS Noise vs. Input Bandwidth of ADC

DRIVING THE ANALOG INPUTS

For best performance, it is important to drive the AD682 analog input from a low impedance signal source. This enhances the sampling accuracy by minimizing the analog and digital crosstalk. Signals which come from higher impedance sources (e.g., over 5 kΩ) will have a relatively higher level of crosstalk. For applications where signals have high source impedance, an operational amplifier buffer in front of the AD682 is required. The AD712 (precision BiFET op amp) is recommended for these applications.

HIGH FREQUENCY SAMPLING

Aperture jitter and distortion are the primary factors which limit frequency domain performance of a sample-and-hold amplifier. Aperture jitter modulates the phase of the hold command and produces an effective noise on the sampled analog input. The magnitude of the jitter induced noise is directly related to the frequency of the input signal.

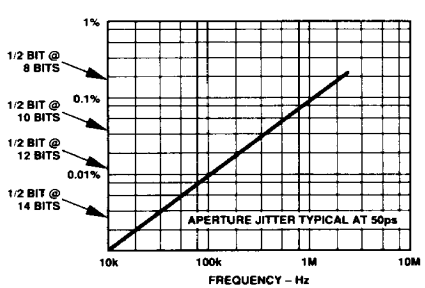


Figure 6. Error Magnitude vs. Frequency

A graph showing the magnitude of the jitter induced error vs. frequency of the input signal is given in Figure 6.

The accuracy in sampling high frequency signals is also constrained by the distortion and noise created by the sample-and-hold. The level of distortion increases with frequency and reduces the "effective number of bits" of the conversion.

Measurements of Figures 7 and 8 were made using a 14-bit A-to-D converter with V_{IN} = 10 V p–p and a sample frequency of 100 kSPS.

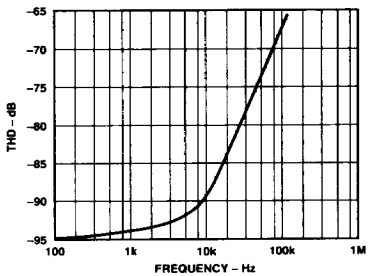


Figure 7. Total Harmonic Distortion vs. Frequency

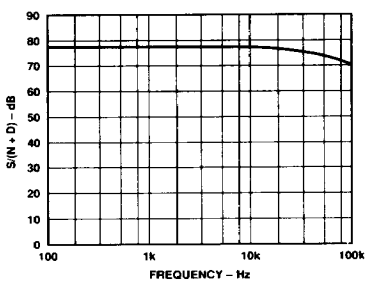


Figure 8. Signal/(Noise and Distortion) vs. Frequency

THE AD682 IN A PING-PONG ARRANGEMENT

In a ping-pong arrangement two sample-and-hold amplifiers are connected to the same analog input source. While one channel is sampling the analog input, the other is in the hold mode. Depending upon the ADC conversion time, a ping-pong circuit can increase data throughput rates by as much as 100%. The AD682's excellent interchannel aperture delay, gain and offset errors make it ideal to use in a ping-pong arrangement.

Figure 9 shows the AD682 in a ping-pong arrangement with the AD671 12-bit, 500 ns A/D converter. A high speed switch (ADG201HS) directs the appropriate AD682 output to the AD671. In this system the data throughput rate is increased by up to 80% as compared to a system using only one channel of the AD682.

THE AD682 FOR IN-PHASE (I) AND QUADRATURE (Q) DEMODULATION

The AD682 can be used to demodulate digital data that has been I and Q modulated. Using two SHAs for the signal acqui-

sition allows the use of slower and lower cost SHAs and A/D converters as compared to a system using one SHA.

Figure 10 shows the AD682 being used as a I and Q demodulator. If the carrier frequency is represented by f and w = 2 πf, the incoming signal can be represented by s(t) = I(n) × cos(wt) + Q(n) × sin(wt), where I(n) and Q(n) (the nth I− Q pair sent) only take on discrete values and must stay constant for at least one carrier period (2 π/w).

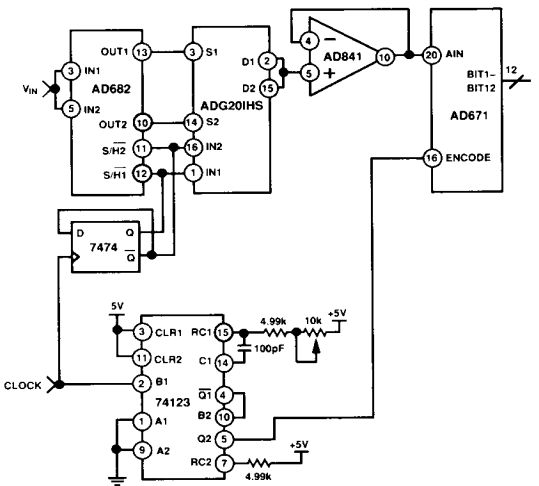


Figure 9. Ping-Ponged AD682

The clock source from which the AD682's control signals are derived must be coherent with the input signal carrier. To recover I(n), s(t) must be sampled when the in-phase carrier component is 1 and the quadrature component is 0 (when t is integer multiples of 2 π/W). Similarly to recover Q(n) s(t) must be sampled when the in-phase carrier component is 0 and the quadrature component is 1 (when t is integer multiples of 2 π/w + π/2).

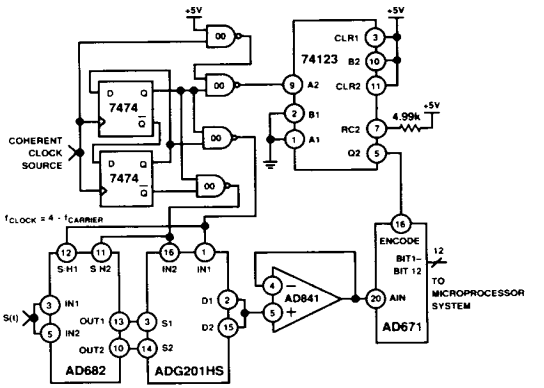


Figure 10. The AD682 Used for I and Q Demodulation