ANALOG DEVICES

Four-Channel High Speed Sample-and-Hold Amplifier

AD684

1.1 Scope.

This specification covers the detail requirements for a complete monolithic four-channel sample-and-hold amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
– 1	AD684S(Q)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Pin Cerdip

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supplies (V_{CC}, V_{EE}) . . . . . ±15 V
Logic Inputs . . . . . −0.5 V to +7 V
Analog Inputs . . . . . ±12 V
Output Short Circuit to Ground, V_{CC} or V_{EE} . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . +300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W
θ_{JA} = 120°C/W

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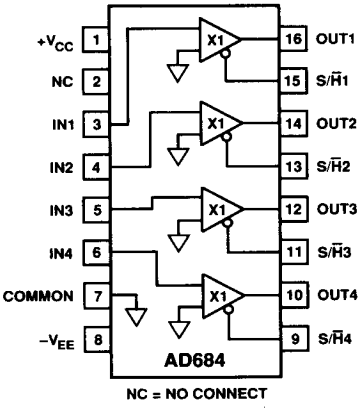
Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2	Sub Group 3	Test Condition	Unit
Hold Mode Offset	H_{OS}	−1	$-4 < H_{OS} < +3$	$-4 < H_{OS} < +3$	$-4 < H_{OS} < +3$	$-4 < H_{OS} < +3$	V_{IN} = 0 V, V_{SUP} = ±12 V	mV
Bias Current	I_B	−1	250	250	250	250	V_{IN} = 0 V, V_{SUP} = ±12 V, Sample Mode	nA max
Logic Input High Voltage	V_{IH}	−1	2.0	2.0	2.0	2.0	V_{SUP} = ±12 V[1]	V min
Logic Input Low Voltage	V_{IL}	−1	0.8	0.8	0.8	0.8	V_{SUP} = ±12 V[2]	V max
Logic Input Current	I_L	−1	10	10	10	10	V_{IN} = 0 V; V_{SUP} = ±12 V, V_{DIG} = +5 V	μA max
Supply Current	I_{SUPPLY}	−1	±26	±26	±26	±26	V_{IN} = 0 V, V_{SUP} = ±12 V, Hold Mode	mA max
Power Supply Rejection (+)	+PSRR	−1	65	65	65	65	V_{IN} = 0 V, V_{EE} = −12 V, Sweep V_{CC} +10.8 V to +13.2 V	dB min
Power Supply Rejection (−)	−PSRR	−1	60	60	60	60	V_{IN} = 0 V, V_{CC} = +12 V, Sweep V_{EE} −10.8 V to −13.2 V	dB min
Acquisition Time	I_{ACQ}	−1	1.0[3]				10 V Step to 0.01%	μs max
			0.6[3]				10 V Step to 0.1%	
Hold Settling Time	I_{SET}	−1	500[3]				To 1 mV	ns max
Droop Rate	V_{DRP}	−1	1	1	1	1	V_{IN} = (+5 V, 0, −5 V), V_{SUP} = ±12 V	μV/μs max
Sample Mode Offset	S_{OS}	−1	200	200	200	200	V_{IN} = 0 V, V_{SUP} = ±12 V	mV max
Output Drive Current[4]	I_{OUT}	−1	+5	+5	+5	+5	V_{IN} = +5 V, Output Sourcing, V_{SUP} = ±12 V	mA
			−5	−5	−5	−5	V_{IN} = −5 V, Output Sinking, V_{SUP} = ±12 V	
Interchannel Offset	$INTV_{OS}$	−1	2	2	2	2	V_{IN} = 0 V, V_{SUP} = ±12 V	mV max
Gain Error	A_E	−1	±0.05	±0.05	±0.05	±0.05	V_{IN} = −5 V to +5 V, V_{SUP} = ±12 V	% FS max

NOTES
[1]As S/Hs hold 0 V, switch V_{IN} to 5 V, sample, and measure output.
[2]As S/Hs hold 0 V, switch V_{IN} to 5 V, and measure output.
[3]Guaranteed not tested.
[4]Output sourcing/sinking ±5 mA while the H_{OS} shifts < ±2.5 mV.

3.2.1 Functional Block Diagram and Terminal Assignments.

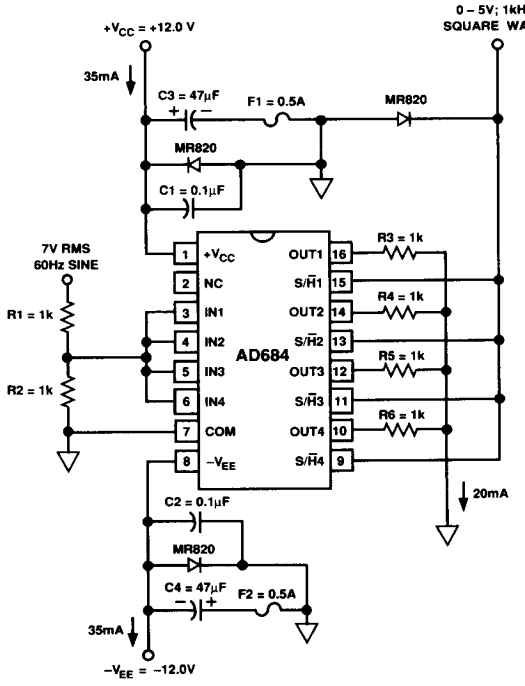


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (60).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTES
1. SUPPLY CURRENT MAX IS 35mA TYPICAL AT +125°C.
2. R1 TO R6 ARE 1kΩ ±1% TOLERANCE.
3. THE R1 & R2 RESISTOR DIVIDER CONNECTED TO THE 7V RMS SOURCE IS ONCE PER BOARD.
4. R3 TO R6 ARE ONCE PER DUT.
5. $\pm V_{SUP}$ FOR BURN-IN IS ±12.0V.
6. 16-PIN DIP: 0.300 WIDE / 0.100 PITCH.