1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS multiplying digital-to-analog converter (LOGDAC®) that can attenuate an analog signal over the range 0 to −88.5dB in 0.375dB steps.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
−1	AD7111T(X)/883B
−2	AD7111U(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
E	E-20A	20-Terminal LCC
Q	Q-16	16-Pin Cerdip

1.3 Absolute Maximum Ratings. (T_A = 25°C unless otherwise noted)

V_{DD} to GND	+7V
V_{IN} to AGND	+35V
Digital Input Voltage to DGND	−0.3V, V_{DD}
Output Voltage (Pin 1) to AGND	−0.3V, V_{DD}
V_{RFB} to AGND	±35V
AGND to DGND	0 to V_{DD}
DGND to AGND	0 to V_{DD}
Power Dissipation	
Up to +75°C	450mW
Derate above +75°C	6mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

NOTE
Pin numbers refer to DIP package ONLY.

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-16 and E-20A
θ_{JA} = 120°C/W for Q-16 and E-20A

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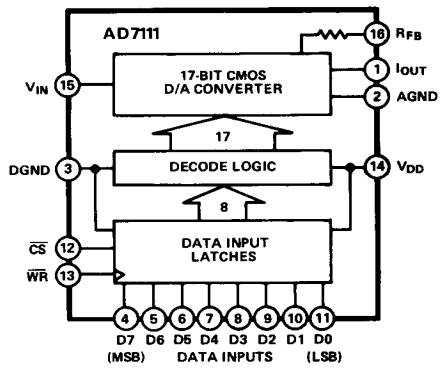
Table 1.

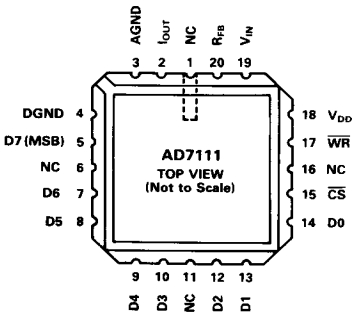
Test	Symbol	Device	Design Limit T_{min} to T_{max}	Sub Group 1	Sub Group 2,3	Sub Group 4	Test Condition[1]	Units
Gain Error	A_E	−1	0.20	0.15	0.2			± dB max
		−2	0.15	0.15	0.15	0.10		
0.375dB Steps: Accuracy = ±0.17dB[2]	RA	−1	0–30	0–30	0–30			dB min
		−2	0–36	0–30	0–36	0–36		
0.75dB Steps: Accuracy = ±0.35dB[2]	RA	−1	0–36	0–42	0–36			dB min
		−2	0–42	0–42	0–42	0–48		
1.5dB Steps: Accuracy = ±0.7dB[2]	RA	−1	0–42	0–48	0–42			dB min
		−2	0–48	0–48	0–48	0–54		
3.0dB Steps: Accuracy = ±1.4dB[2]	RA	−1	0–48	0–60	0–48			dB min
		−2	0–54	0–60	0–54	0–66		
6.0dB Steps: Accuracy = ±2.7dB[2]	RA	−1	0–60	0–60	0–60			dB min
		−2	0–60	0–60	0–60	0–72		
Nominal 0.375dB Step[3]	MR	−1	0–48	0–48	0–48			dB min
		−2	0–54	0–48	0–54	0–54		
Nominal 0.75dB Step[3]	MR	−1	0–60	0–72	0–60			dB min
		−2	0–66	0–72	0–66			
Nominal 1.5dB Step[3]	MR	−1	0–72	0–85.5	0–72			dB min
		−2	0–78	0–85.5	0–78	0–88.5		
Nominal 3.0dB Step[3]	MR	−1,2	0–88.5	0–88.5	0–88.5			dB min
Nominal 6.0dB Step[3]	MR	−1,2	0–88.5	0–88.5	0–88.5			dB min
DC Supply Rejection	PSR	−1,2	0.005				ΔV_{DD} = ± 10% Input Data Latch Loaded with 0000 0000	± dB per % max
Propagation Delay	t_{PD}	−1,2	4.5				R_{OUT1} = 100Ω, C_{OUT1} = 13pF; Time required for the output current to reach 90% of its final value for a Full Scale Change. Measured from $\overline{WR}$ going high, $\overline{CS}$ = 0V.	µs max
Feedthrough[4]	FT	−1	68				Full scale Change. Measured from $\overline{WR}$ going high, $\overline{CS}$ = 0V. V_{IN} = 6V rms, 1kHz sinewave. Input Data loaded with 1111 1111.	− dB max
		−2	72					
Output Capacitance	C_{OUT}	−1,2	185					pF max
V_{IN} Input Resistance	R_{IN}	−1	7	7	7			kΩ min
		−2	9	9	9			
		−1	18	18	18			kΩ max
		−2	15	15	15			
R_{FB} Input Resistance	R_{FB}	−1	7.3	7.3	7.3			kΩ min
		−2	9.3	9.3	9.3			
		−1	18.8	18.8	18.8			kΩ max
		−2	15.7	15.7	15.7			
Input High Voltage	V_{IH}	−1,2	2.4	2.4	2.4			V min
Input Low Voltage	V_{IL}	−1,2	0.8	0.8	0.8			V max
Input Leakage Current	I_{IN}	−1,2	10	1	10		Digital Inputs = V_{DD} or 0V	± µA max
Input Capacitance	C_{IN}	−1,2	7					pF max
Supply Current	I_{DD}	−1,2	4	1	4		Digital Inputs = V_{IH} or V_{IL}	mA max
			1	0.5	1		Digital Inputs = 0V or V_{DD}	mA max
Chip-Select-to-Write Setup Time[5]	t_{CS}	−1,2	0					ns min
Chip-Select-to-Write Hold Time[5]	t_{CH}	−1,2	0					ns min
Write Pulse Width[5]	t_{WR}	−1,2	500					ns min
Data Valid to Write Setup Time[5]	t_{DS}	−1,2	250					ns min
Data Valid to Hold Time[5]	t_{DH}	−1,2	10					ns min
Refresh Time[5]	t_{RFSH}	−1,2	4.5					ns min

NOTES
[1] V_{DD} = +5V; V_{PIN1} = V_{PIN2} = 0V; V_{IN} = −10V.
[2] Accuracy is measured using the internal R_{FB} and includes effects of leakage current and gain TC.
[3] Monotonic range for specified step.
[4] Feedthrough can be further reduced by connecting the metal lid to ground.
[5] Timing per Figure 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



E Package (LCC)

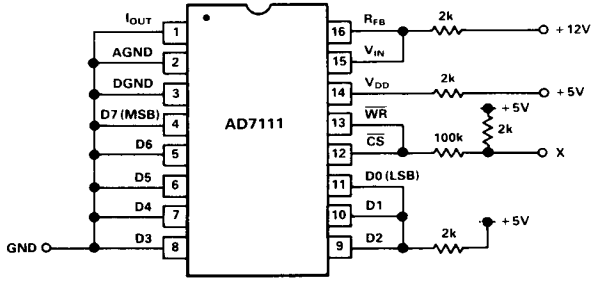


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTE
ON POWER UP APPLY 0V TO POINT X TO LOAD THE INPUT DATA INTO THE DAC.

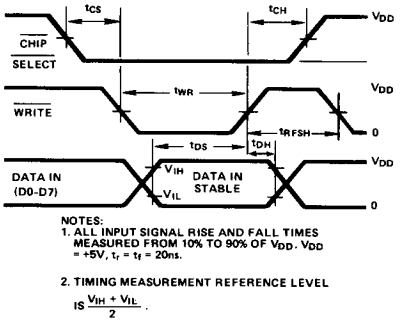


Figure 1. Write Cycle Timing Diagram

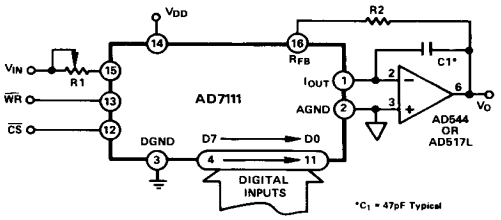


Figure 2. Typical Circuit Configuration

Table 2. Ideal Attenuation in dB vs. Input Code

D7-D4 \ D3-D0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	0.0	0.375	0.75	1.125	1.5	1.875	2.25	2.625	3.0	3.375	3.75	4.125	4.5	4.875	5.25	5.625
0001	6.0	6.375	6.75	7.125	7.5	7.875	8.25	8.625	9.0	9.375	9.75	10.125	10.5	10.875	11.25	11.625
0010	12.0	12.375	12.75	13.125	13.5	13.875	14.25	14.625	15.0	15.375	15.75	16.125	16.5	16.875	17.25	17.625
0011	18.0	18.375	18.75	19.125	19.5	19.875	20.25	20.625	21.0	21.375	21.75	22.125	22.5	22.875	23.25	23.625
0100	24.0	24.375	24.75	25.125	25.5	25.875	26.25	26.625	27.0	27.375	27.75	28.125	28.5	28.875	29.75	29.625
0101	30.0	30.375	30.75	31.125	31.5	31.875	32.25	32.625	33.0	33.375	33.75	34.125	34.5	34.875	35.25	35.625
0110	36.0	36.375	36.75	37.125	37.5	37.875	38.25	38.625	39.0	39.375	39.75	40.125	40.5	40.875	41.25	41.625
0111	42.0	42.375	42.75	43.125	43.5	43.875	44.25	44.625	45.0	45.375	45.75	46.125	46.5	46.875	47.25	47.625
1000	48.0	48.375	48.75	49.125	49.5	49.875	50.25	50.625	51.0	51.375	51.75	52.125	52.5	52.875	53.25	53.625
1001	54.0	54.375	54.75	55.125	55.5	55.875	56.25	56.625	57.0	57.375	57.75	58.125	58.5	58.875	59.25	59.625
1010	60.0	60.375	60.75	61.125	61.5	61.875	62.25	62.625	63.0	63.375	63.75	64.125	64.5	64.875	65.25	65.625
1011	66.0	66.375	66.75	67.125	67.5	67.875	68.25	68.625	69.0	69.375	69.75	70.125	70.5	70.875	71.25	71.625
1100	72.0	72.375	72.75	73.125	73.5	73.875	74.25	74.625	75.0	75.375	75.75	76.125	76.5	76.875	77.25	77.625
1101	78.0	78.375	78.75	79.125	79.5	79.875	80.25	80.625	81.0	81.375	81.75	82.125	82.5	82.875	83.25	83.625
1110	84.0	84.375	84.75	85.125	85.5	85.875	86.25	86.625	87.0	87.375	87.75	88.125	88.5	88.875	89.25	89.625
1111	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE