AMI SEMICONDUCTORS

PEEL™ 18CV8

February 1993

CMOS Programmable Electrically Erasable Logic Device

Features

Advanced CMOS EEPROM™ Technology

Low Power Consumption

- 30mA Standby + 0.5mA/MHz Max (for 25ns)
- 90mA Standby + 0.5mA/MHz Max (for all other speeds)

High Performance

- tPD = 5ns, 7.5ns, 10ns, 15ns, 25ns Max

Reprogrammability

- 100% factory tested
- Cost effective "windowless" package
- Erases and programs in seconds
- Adds convenience, reduces field retrofit and development cost

Foolproof Design Security

- Prevents unauthorized reading or copying of design

Architectural Flexibility

- 74 Product Term X 36 Input array
- Up to 18 Inputs and 8 I/O pins
- Independently configurable I/O macrocells: polarity, register, combinational, bi-directional
- Synchronous preset, asynchronous clear
- Independent output enables

Application Versatility

- Replaces SSI/MSI logic
- Emulates bipolar PAL®, GAL®, and EPLDs
- Simplifies inventory control
- Allows new design possibilities

Development/Programmer Support

- PC-based development tools from AMI
- Third-party development tools and programmer support

General Description

The AMI PEEL18CV8 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally flexible alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the performance of the PEEL18CV8 rivals speed parameters of standard bipolar PLDs with a dramatic improvement in power consumption. The electrically erasable reprogrammable technology of the PEEL18CV8 not only reduces development and field retrofit costs, but also enhances testability, enabling AMI to ensure 100% field programmability and function.

Packaged in a cost effective "windowless" 20-pin DIP, the flexible architecture of the PEEL18CV8 allows for replacement of standard SSI/MSI logic circuitry or pin-out compatible emulation of 20-pin bipolar PAL® devices, GAL® devices, and EPLDs. In addition, over a hundred new logic configurations, not possible with earlier generation PLDs, can be implemented. Development and programming support of the PEEL18CV8 is provided by popular third-party PC-based development tools and stand alone programmers. AMI also offers development tools specifically for the PEEL18CV8 and other PEEL devices.

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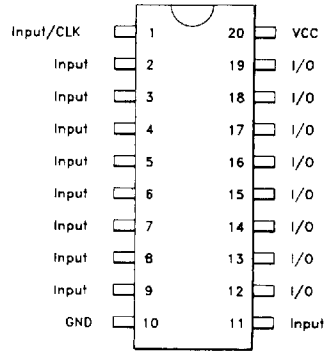
Figure 5: PEEL18CV8 Pin and Block Diagram

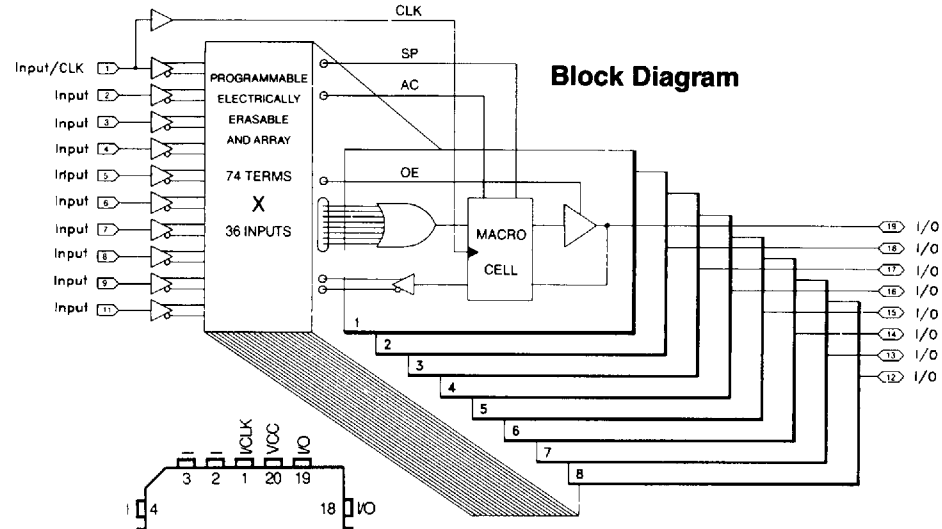
Pin Diagram

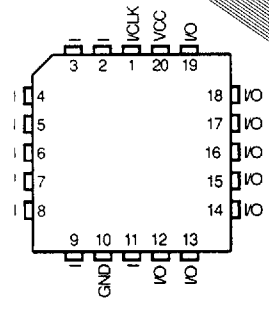


Pin Names

INPUT/CLK	Input and/or Clock
INPUT	Input
GND	Ground
I/O	Bi-Directional Input/Output
V_{CC}	Power Supply (+5V)

Block Diagram

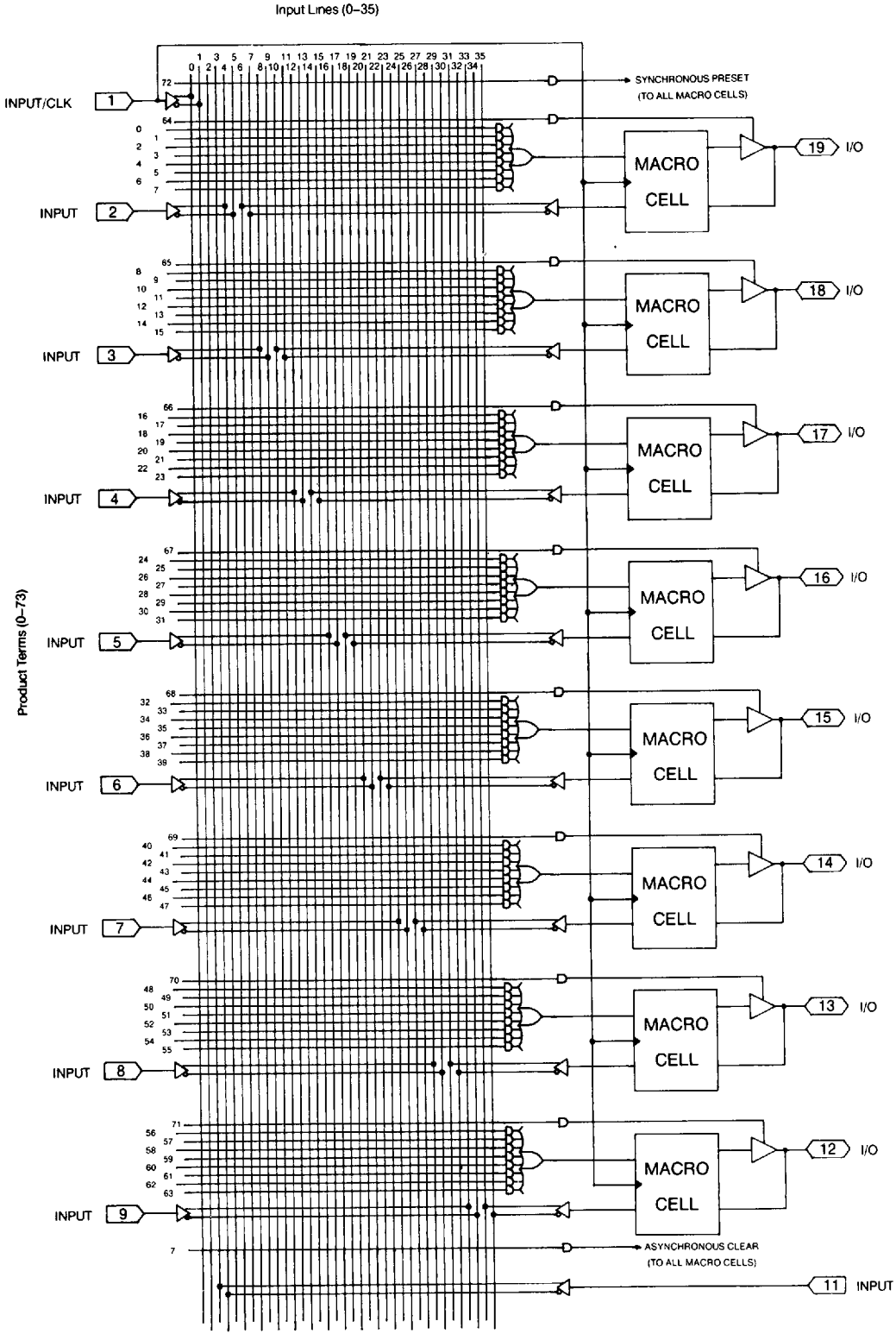




PLCC

SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

Figure 6: PEEL18CV8 Logic Array Diagram



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Architectural Overview

The basic architecture of the PEEL18CV8 is similar to that of earlier generation PLDs to the extent that it utilizes a sum-of-products logic array in a programmable-AND, fixed-OR structure. This familiar logic arrangement allows user-defined output functions to be created by programming the connection of input signals into the array. What makes the architecture of the PEEL18CV8 different, however, is the increased capability and flexibility it provides, resulting in a higher level of equivalent gate integration and a simplification of design.

The block diagram in figure 5 illustrates the key elements of the PEEL18CV8 architecture. Externally, the PEEL18CV8 provides up to 18 inputs and 8 outputs for use. At the core is a programmable electrically erasable "AND array" of 36 input lines by 74 product terms. The 36 input lines are derived from the true and complements of the 18 possible input pins. The 74 product terms are made up of 1 synchronous preset term, 1 asynchronous clear term, 8 output enable terms, and 64 terms divided into groups of 8, each feeding into an OR function.

Each OR function is directly associated with one of eight macrocells and I/O pins. An individual macrocell can be programmed into one of twelve different configurations. Depending on the configuration, the output of the macrocell can be fed back into the array or output via its associated I/O pin. The configurations include various arrangements for bi-directional I/O, registered or combinatorial feedback, registered or combinatorial output, and output polarity control. The output enable term of each I/O pin can be used to force a high impedance state for bi-directional I/O operations or for dedicated input usage. The synchronous preset term, asynchronous clear term, and clock (pin 1, I/CLK) are globally routed to all macrocells.

Logic Array Operation

A more detailed view of the overall architecture, specifically the logic array, is illustrated by the PEEL18CV8 logic array diagram in figure 6. As referred to previously, the logic array of the PEEL18CV8 consists of:

36 Input Lines:

10 true and complement inputs

8 true and complement inputs/feedbacks

74 Product Terms:

64 product terms (8x8 sum-of-products form)

8 output enable product terms

1 synchronous preset term

1 asynchronous clear term

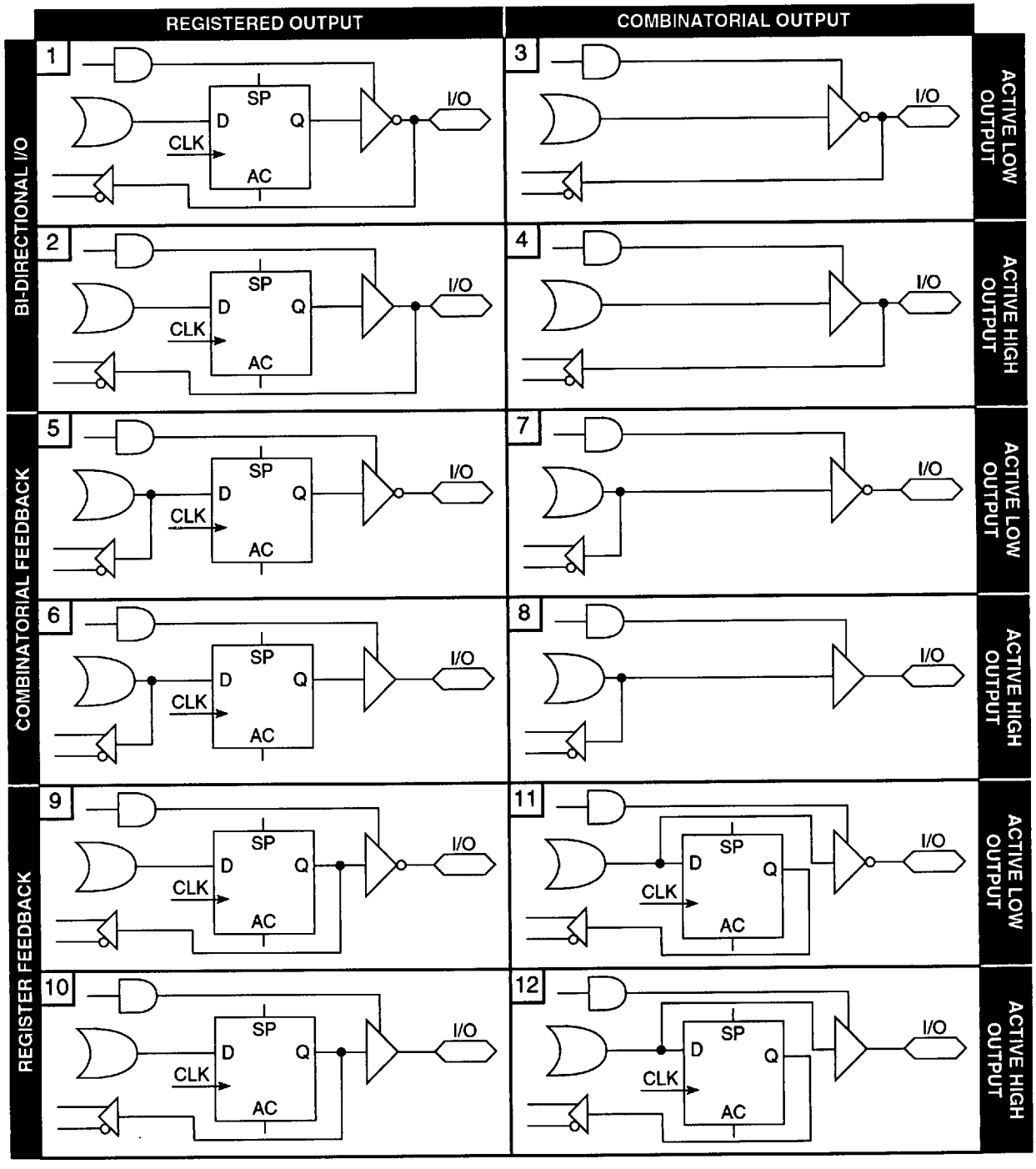
On the logic array diagram, the 36 input lines (0-35) run vertically and the 74 product terms (0-73) run horizontally. Each input line and product term intersection in the array has an associated programmable EEPROM memory cell that determines whether the intersection is connected or open. A connection allows an input line to become a logical input of the intersected product term (AND gate). Thus, each product term, although unlikely in a real application, truly equals a 36 input AND gate.

In figure 6, the logic array has 64 product terms that are divided into groups of 8, each feeding into a sum (OR gate). By connecting specific inputs or I/O macrocell feedbacks to the product terms, complex sum-of-products logic functions can be created. Each sum feeds into its associated I/O macrocell, where the logic function can be further controlled for output to an I/O pin or feedback into the array.

In addition to the 64 product terms of the 8 sum-of-product groups, there are 8 output enable product terms, 1 synchronous preset product term, and 1 asynchronous clear product term. These additional terms are used to directly control specific I/O functions, which are covered in the following section.

Each of the 8 output enable terms can enable or disable the output of its associated I/O macrocell. When the output enable product term is a logical true (HIGH), the output signal is enabled to the I/O pin. When it is a logical false (LOW), the I/O pin is in a high impedance state. The output-enable product terms allow individual I/O pins to be input only or bi-direction I/O.

Figure 7: PEEL18CV8 Macrocell Configuration Equivalent Circuits



I/O Macrocell and Output Enable Operation

A great amount of architectural flexibility is provided by the PEEL18CV8's reconfigurable I/O macrocells and independently controlled output enables. A closer look at the I/O macrocell, figure 9, shows that it consists of a D-type flip-flop and two signal select multiplexers.

The D-type flip-flop operates similarly to standard TTL D flip- flops to the extent that the D input is latched on the rising edge (LOW to HIGH transition) of the CLK input and Q or $\overline{Q}$ output signals can be used. Two additional inputs are controlled by the asynchronous clear and synchronous preset terms.

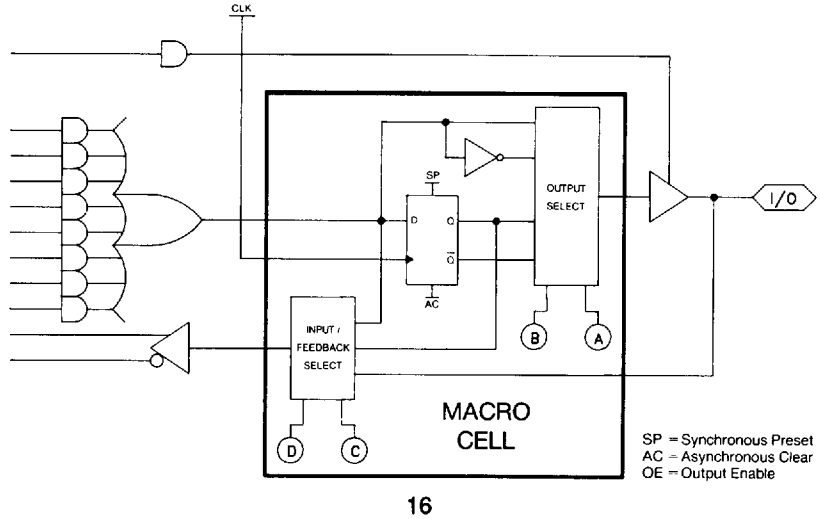
When the asynchronous clear product term is asserted (HIGH), the Q output will immediately be set to a LOW, regardless of the clock state. When the synchronous preset term is asserted (HIGH), the Q output will be set to a HIGH on the following rising edge (LOW to HIGH transition) of the CLK input. Priority is given to the asynchronous clear signal if both asynchronous clear and synchronous preset have been asserted. Upon power-up, the asynchronous clear function is automatically performed, setting the Q outputs of all macrocell flip-flops to a LOW.

The two signal select multiplexers of each macrocell are controlled by four EEPROM programmable bits (A,B,C, and D) that determine which of the twelve possible configurations the macrocell will assume. This independent flexibility allows a single PEEL18CV8 to implement a combination of configurations among its eight macrocells. The configurations include various arrangements for bi-directional I/O, registered or combinatorial feedback, registered or combinatorial output, and output polarity control. The twelve possible I/O macrocell configurations are listed in figure 8. Their equivalent circuits are illustrated in figure 7.

Figure 8: PEEL18CV8 Macrocell Configuration Bits

Configuration					Input/ Feedback Select	Output Select	
#	A	B	C	D			
1	1	1	1	1	Bi-Directional I/O	Register	Active Low
2	0	1	1	1			Active High
3	1	0	1	1		Combinatorial	Active Low
4	0	0	1	1			Active High
5	1	1	1	0	Combinatorial Feedback	Register	Active Low
6	0	1	1	0			Active High
7	1	0	1	0		Combinatorial	Active Low
8	0	0	1	0			Active High
9	1	1	0	0	Register Feedback	Register	Active Low
10	0	1	0	0			Active High
11	1	0	0	0		Combinatorial	Active Low
12	0	0	0	0			Active High

Figure 9: PEEL18CV8 Macrocell Diagram



Application of the PEEL18CV8

The versatility of the PEEL makes it an effective alternative to conventional methods of logic design over a broad range of applications.

As an SSI/MSI logic replacement, the PEEL enhances the design process with increased flexibility, higher performance, faster development time, and design security. Manufacturing benefits are also realized by requiring fewer components and interconnects, resulting in more efficient use of space, simplified inventory control, and high reliability.

As a bipolar PAL® replacement, the PEEL has comparable speed, yet offers several advantages, including enhanced design flexibility, simplified inventory control, reduced power consumption, reprogrammability, and 100% factory testability for function and programming.

Design flexibility is of particular importance since the PEEL18CV8 not only emulates the majority of the 20 pin PAL® devices (see figure 10), but also allows functions found among several PAL® device types to be combined, i.e. combinatorial and registered outputs on a single PEEL device. In addition, completely new functions, not supported by the standard PAL® devices, can be implemented. This flexibility means a designer can focus on the design, rather than on the restrictions of a fixed architecture. Reprogrammability is also a key benefit over one-time-programmable PALs®. This feature adds convenience and cost savings in development prototyping and field retrofitting of systems. Converting existing PAL® designs to the PEEL18CV8 for plug-in replacement is easily accomplished using the PEEL development tools, which are described later in this data book.

As a design alternative to low-density gate arrays, one or more PEEL18CV8s offers a cost-effective and low-risk option. With its architectural flexibility and equivalent gate density of approximately 300 gates, designs traditionally employing low-density gate arrays can be implemented quickly at no factory development (NRE) cost. Unlike the lead times encountered with gate arrays, the PEEL18CV8 is off-the-shelf available. Furthermore, if a design error is made or an upgrade is necessary, the changes can simply be reprogrammed.

Similar to SSI/MSI logic, PALs® and low density gate arrays, applications of the PEEL18CV8 cover all the primary areas of system design, including data processing, communications, industrial, consumer, military, and transportation. Specific functions implemented using the PEEL18CV8 range from basic logic and system support circuitry to stand-alone controllers. Some of the applications' possibilities include:

SSI/MSI Logic Replacement/Customization

- Random logic
- Decoders/encoders
- Comparators
- Multiplexers
- Counters
- Shift registers

Processor System Support

- Address decoding
- Wait-state generation
- Memory protection
- Memory refresh
- DMA control
- Interrupt control
- Timer/Counter functions
- Bus arbitration and interface
- Error detection and correction

I/O Interface and Support

- Intelligent I/O port
- Data Comm interface
- Display interface
- Keyboard scanning
- Disk and tape drive control
- Front panel interface

Stand-Alone Non μP Based Controllers

- Motor control
- Sensor monitoring
- Security access control
- Display Control

Figure 10: PLD Devices that can be emulated by the PEEL18CV8

20-pin PAL®

Output Type	Part Number and I/O Capacity								
Combinatorial-High	10H8	12H6	14H4	16H2			16H8	16HD8	
Combinatorial-Low	10L8	12L6	14L4	16L2			16L8	16LD8	
Combinatorial-Polarity							16P8		18P8
Registered-Low					16R4	16R6	16R8		
Registered-Polarity					16RP4	16RP6	16RP8		

ALTERA

EP 300/310

Absolute Values

Absolute Maximum Ratings[8]

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
Vcc	Supply Voltage	Relative to GND	-0.5	7.0	V
Vi	Voltage applied to Input[4,10]	Relative to GND[1,2]	-0.5	Vcc +0.6	V
Vo	Voltage applied to Output	Relative to GND[1,2]	-0.5	Vcc +0.6	V
Io	Output Current	Per pin (Iol, Ioh)		+25	mA
Tst	Storage Temperature		-65	+150	C
Tlt	Lead Temperature	(soldering 10 seconds)		+300	C

Operating Ranges

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
Vcc	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	V
Ta	Operating Temperature	Commerical	0	+70	C
		Industrial	-40	+85	C
Tr	Clock Rise Time[5]	Test points at 10% and 90% levels		250	ns
Tf	Clock Fall Time[5]	Test points at 10% and 90% levels		250	ns
Trvcc	Vcc Rise Time[5]	Test points at 10% and 90% levels		250	ms

DC Characteristics (Over Operating Range Specifications)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Iil	Input Leakage	Vin = GND to Vcc			±10	µA
Ioz	Output Leakage	I/O = High Impedance Vo = GND to Vcc			±10	µA
Vil	Input Low Voltage		-0.3		0.8	V
Vih	Input High Voltage		2.0		Vcc+0.3	V
Vol	Output Low Voltage TTL	Iol = +12.0mA[12]			0.45	V
Volc	Output Low Voltage CMOS	Iol = 10µA[12]			0.1	V
Voh	Output High Voltage TTL	Ioh = -4.0mA[12]	2.4			V
Vohc	Output High Voltage CMOS	Ioh = -10µA[12]	Vcc -0.1			v

Capacitance

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Cin	Input Capacitance[3]	Frequency = 1MHz		4	6	pF
Cout	Output Capacitance[3]	Frequency = 1MHz		8	12	pF
Cclk	Clk Pin Capacitance[3]	Frequency = 1MHz		8	13	pF

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Electrical Characteristics (Over Operating Range Specifications)

PREVIEW			18CV8-5**		18CV8-7**		18CV8-10		18CV8-15		18CV8-25	
SYMBOL	PARAMETER	UNITS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
Iccs	Vcc Current Standby[9]	mA		120		90		90		90		30
Icca	Vcc Current Active[9]	mA		Iccs + 0.5 mA/MHz		Iccs + 0.5 mA/MHz		Iccs + 0.5 mA/MHz		Iccs + 0.5 mA/MHz		Iccs + 0.5 mA/MHz
tPD	Input[4] to combinatorial output	ns		5		7.5		10		15		25
tOD	Input[4] to output disable[6]	ns		5		7.5		10		15		25
tOE	Input[4] to output enable[6]	ns		5		7.5		10		15		25
tSC	Input[4] set-up to clock	ns	4		6		7		12		23	
tHC	Input[4] hold after clock	ns	0		0		0		0		0	
tCH	Clock high time[5]	ns	4		6		7		10		15	
tCL	Clock low time[5]	ns	4		6		7		10		15	
tCO1	Clock to output	ns		4		6		7		12		15
tCO2	Clock to combinatorial output delay via registered feedback[3]	ns		8		9		12		25		35
tCP	Minimum clock period tSC+tCO1	ns	8		12		14		24		35	
fmax1	Max clock freq (1/tSC+tCL)[3]	MHz	125		83.3		71.4		45		28.5	
fmax2	Max clock freq (1/tCP)[3]	MHz	125		83.3		71.4		41.6		28.5	
fmax3	Max clock freq (1/tCL+tCH)[3]	MHz	125		83.3		71.4		50		33.3	
tAW	Async clear pulse width[11]	ns	5		7.5		10		15		25	
tAP	Input to async clear TYPICAL	ns		8		12		15		20		30
tAR	Async reset recovery TYPICAL	ns		6		10		10		10		20
tRESET	Register power-on-reset[5]	µs		3		5		5		5		5

NOTES:

** No industrial versions.

1. Minimum DC input is -0.5V; however, inputs may undershoot to -2.0V for periods less than 20ns.
2. Voltage applied to input or output must not exceed Vcc+1.0V.
3. These measurements are periodically sample tested.
4. "Input" refers to an Input signal.
5. Test points for Clock and Vcc in Tr, Tf, Trvcc, tCH, tCL, and tRESET are referenced at 10% and 90% levels.
6. See AC test point/load circuit table for tOE and tOD testing.
7. Typical values and capacitance are measured at Vcc = 5.0V and Ta = 25°C.
8. Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.
9. I/O pins are open (no load).
10. Vin specified is not for program/verify operation. Contact AMI for information regarding PEEL program/verify specifications.
11. Minimum width required to ensure proper asynchronous clear operation and does not imply rejection of signal less than this value.
12. Contact factory for increased Iol requirements.

Figure 11: PEEL18CV8 AC Switching Waveforms

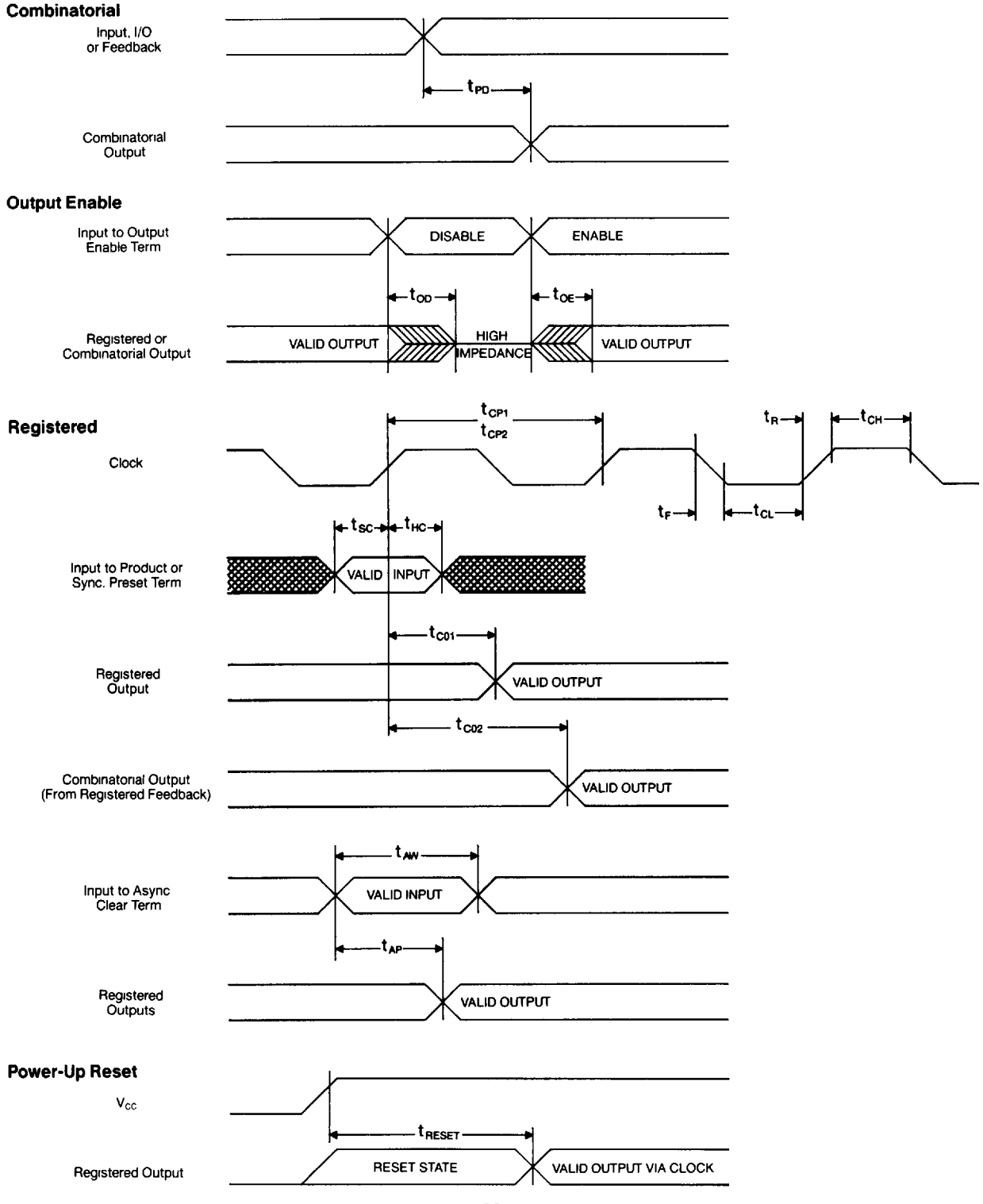
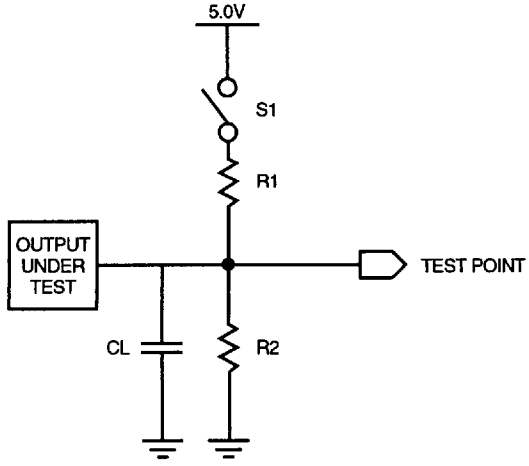


Figure 12: PEEL18CV8 AC Test Loads/Waveforms

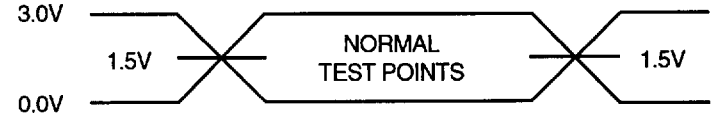
AC Equivalent Load Circuit



TTL Levels
R1 = 464Ω
R2 = 250Ω

CMOS Levels
R1 = 480KΩ
R2 = 480KΩ

AC Testing Input/Output Waveform



AC Test Point/Load Circuit Table

AC Test	Test Point	CL	S1
NORMAL	1.5V	50pF	closed
tOE(Z→0)	VOH	50pF	open
tOE(Z→0)	VOL	50pF	closed
tOD(1→Z)	VOH−.5V	5pF	open
tOD(0→Z)	VOL+.5V	5pF	closed

Z=High Impedance