PEEL™ 18LV8Z-25 / I-35

CMOS Programmable Electrically Erasable Logic Device

Features

- **Low Voltage, Ultra Low Power Operation**
  - Vcc = 2.7 to 3.6 V
  - Icc = 5 µA (typical) at standby
  - Icc = 1.5 mA (typical) at 1 MHz
  - Meets JEDEC LV Interface Spec (JEDSD8-A)
  - 5 Volts tolerant inputs and I/O's
- **CMOS Electrically Erasable Technology**
  - Superior factory testing
  - Reprogrammable in plastic package
  - Reduces retrofit and development costs
- **Application Versatility**
  - Replaces random logic
  - Super set of standard PLDs
  - Pin and JEDEC compatible with 16V8
  - Ideal for battery powered systems
  - Replaces expensive oscillators
- **Architectural Flexibility**
  - Enhanced architecture fits in more logic
  - 113 product terms x 36 input AND array
  - 10 inputs and 8 I/O pins
  - 12 possible macrocell configurations
  - Asynchronous clear, Synchronous preset
  - Independent output enables
  - Programmable clock; pin 1 or p-term
  - Programmable clock polarity
  - 20 Pin DIP/SOIC/TSSOP and PLCC
  - Schmitt triggers on clock and data inputs
- **Schmitt Trigger Inputs**
  - Eliminates external Schmitt trigger devices
  - Ideal for encoder designs

General Description

The PEEL18LV8Z is a Programmable Electrically Erasable Logic (PEEL) SPLD (Simple Programmable Logic Device) that operates over the supply voltage range of 2.7V-3.6V and features ultra-low, automatic "zero" power-down operation. The PEEL18LV8Z is logically and functionally similar to ICT's 5V PEEL18CV8 and PEEL18CV8Z. The "zero power" (25 µA max. Icc) power-down mode makes the PEEL18LV8Z ideal for a broad range of battery-powered portable equipment applications, from hand-held meters to PCMCIA modems. EE-reprogrammability provides both the convenience of fast reprogramming for product development and quick product personalization in manufacturing, including Engineering Change Orders.

The differences between the PEEL18LV8Z and PEEL18CV8 include the addition of programmable clock polarity, p-term clock, and Schmitt trigger input buffers on all inputs, including the clock. Schmitt trigger inputs allow direct input of slow or noisy signals.

Like the PEEL18CV8, the PEEL18LV8Z is a logical superset of the industry standard PAL16V8 SPLD. The PEEL18LV8Z provides additional architectural features that allow more logic to be incorporated into the design. ICT's JEDEC file translator allows easy conversion of existing 20 pin PLD designs to the PEEL18LV8Z architecture without the need for redesign. The PEEL18LV8Z architecture allows it to replace over twenty standard 20-pin DIP, SOIC, TSSOP and PLCC packages Pin Configuration.

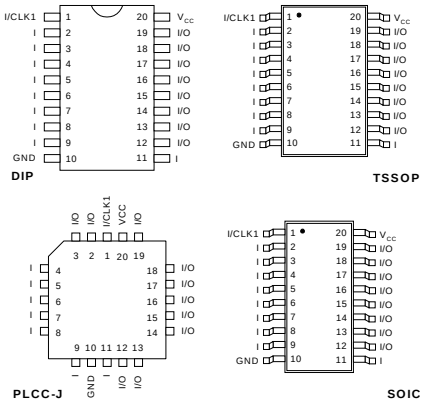


Figure 1 - Pin Configuration

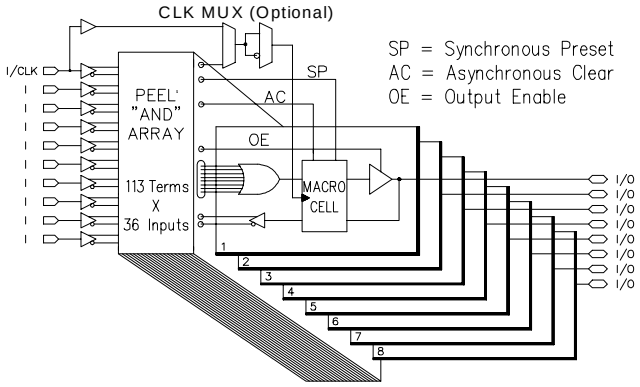


Figure 2 - Block Diagram

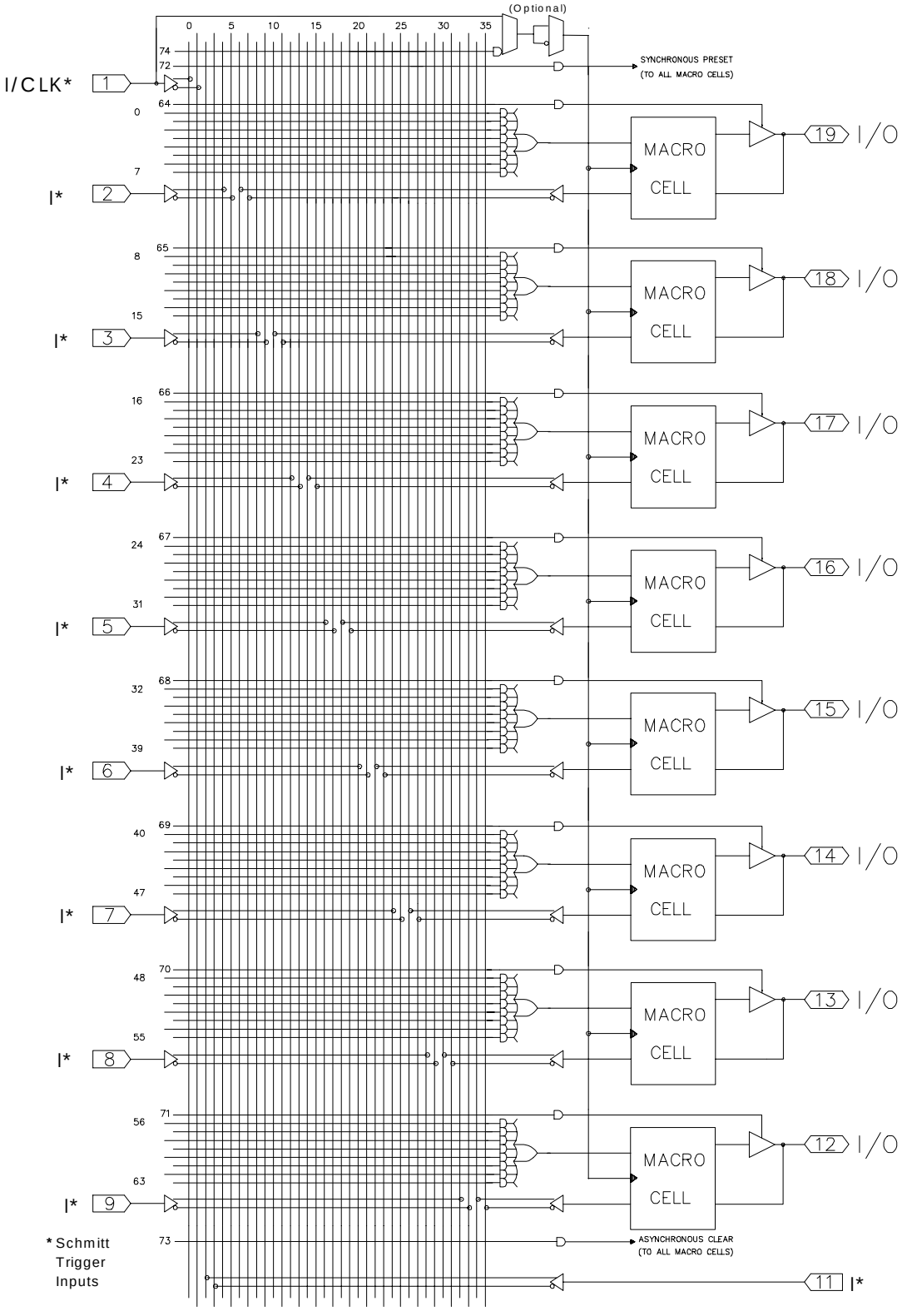


Figure 3 - PEEL18LV8Z Logic Array Diagram

Function Description

The PEEL18LV8Z implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. Programming the connections of input signals into the array creates user-defined functions. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL18LV8Z architecture is illustrated in the block diagram of Figure 14. Ten dedicated inputs and 8 I/Os provide up to 18 inputs and 8 outputs for creation of logic functions. At the core of the device is a programmable electrically erasable AND array that drives a fixed OR array. With this structure, the PEEL18LV8Z can implement up to 8 sum-of-products logic expressions.

Associated with each of the 8 OR functions is an I/O macrocell that can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to be used to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL18LV8Z (shown in Figure 15) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

- **36 Input Lines:**
  - 20 input lines carry the true and complement of the signals applied to the 10 input pins
  - 16 additional lines carry the true and complement values of feedback or input signals from the 8 I/Os
- **113 product terms:**
  - 102 product terms are used to form sum of product functions
  - 8 output enable terms (one for each I/O)
  - 1 global synchronous preset term
  - 1 global asynchronous clear term
  - 1 programmable clock term

At each input-line/product-term intersection, there is an EEPROM memory cell that determines whether or not there is a logical connection at that intersection. Each product term is essentially a 36-input AND gate. A product term that is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a "don't care" state exists and that term will always be TRUE.

When programming the PEEL18LV8Z, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function).

Variable Product Term Distribution

The PEEL18LV8Z provides 113 product terms to drive the 8 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see Figure 15). This distribution allows optimum use of the device resources.

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently lets you to tailor the configuration of the PEEL18LV8Z to the precise requirements of your design.

Macrocell Architecture

Each I/O macrocell, as shown in Figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The four EEPROM bits controlling these multiplexers determine the configuration of each macrocell. These bits determine output polarity, output type (registered or non-registered) and input-feedback path (bidirectional I/O, combinatorial feedback). Refer to Table 1 for details.

Equivalent circuits for the twelve macrocell configurations are illustrated in Figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10), the macrocell provides eight additional configurations. When creating a PEEL device design, the desired macrocell configuration is generally specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register is set HIGH at the next rising edge of the clock input. Satisfying

the asynchronous clear sets Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is switched into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

The PEEL18LV8Z macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell can be obtained from three different locations; from the I/O input pin, from the Q output of the flip-flop (registered feedback), or directly from the OR gate (combinatorial feedback).

Bi-directional I/O

The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with a bi-directional I/O, refer to Figure 4).

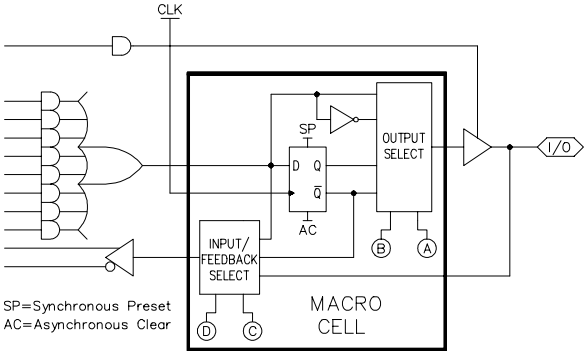


Figure 4 - PEEL18LV8Z I/O Macro cell

Combinatorial Feedback

The signal-select multiplexer gives the macrocell the ability to feedback the output of the OR gate, bypassing the output buffer, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in Figure 5.)

Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is programmed to be combinatorial or registered. When implementing a combinatorial output function, registered feedback allows for the internal latching of states without giving up the use of the external output.

Programmable Clock Options

A unique feature of the PEEL18LV8Z is a programmable clock multiplexer that allows the user to select true or complement forms of either input pin or product-term clock sources.

Operates in both 3 Volt and 3.3 Volt Systems

The PEEL18LV8Z is designed to operate with a V_{CC} range of 2.7 to 3.6 Volts D.C. This allows operation in both 3 Volt 10% (battery operated) and 3.3 Volt 10% (power supply operated) systems. The propagation delay t_{PD} is 5 ns slower at the lower voltage, but this is typically not an issue in battery-operated systems (see - A.C. Electrical CharacteristicsTable 1 - Absolute Maximum Ratings- A.C. Electrical Characteristics).

Schmitt Trigger Inputs

The PEEL18LV8Z has Schmitt trigger input buffers on all inputs, including the clock. Schmitt trigger inputs allow direct input of slow signals such as biomedical and sine waves or clocks. They are also useful in cleaning up noisy signals. This makes the PEEL18LV8Z especially desirable in portable applications where the environment is less predictable.

Zero Power Feature

The CMOS PEEL18LV8Z features "Zero-Power" standby operation for ultra-low power consumption. With the "Zero-Power" feature, transition-detection circuitry monitors the inputs, I/Os (including CLK) and feedbacks. If these signals do not change for a period of time greater than approximately three t_{PD} 's, the outputs are latched in their current state and the device automatically powers down. When the next signal transition is detected, the device will

"wake up" for active operation until the signals stop switching long enough to trigger the next power-down. (Note that the tPD is approximately 5 ns. slower on the first transition from sleep mode.)

As a result of the "Zero-Power" feature, significant power savings can be realized for combinatorial or sequential operations when the inputs or clock change at a modest rate. See Figure 6.

When the PEEL18LV8Z is powered up, a built-in feature holds the outputs in tri-state until Vcc reaches 2.2V. This prevents output transitions during power-up.

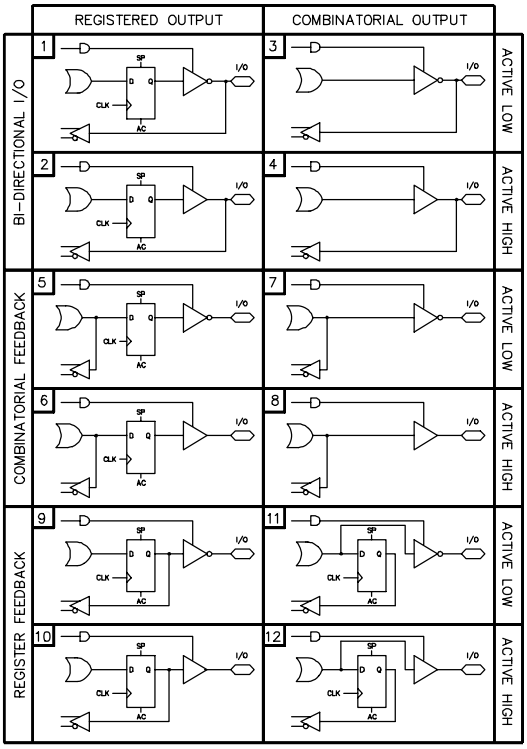


Figure 5 - Equivalent Circuits for the twelve configurations of the PEEL18LV8Z I/O Macrocell

Configuration					Input/Feedback Select	Output Select	
#	A	B	C	D			
1	0	0	1	0	Bi-directional I/O	Register	Active Low
2	1	0	1	0			Active High
3	0	1	0	0		Combinatorial	Active Low
4	1	1	0	0			Active High
5	0	0	1	1	Combinatorial Feedback	Register	Active Low
6	1	0	1	1			Active High
7	0	1	1	1		Combinatorial	Active Low
8	1	1	1	1			Active High
9	0	0	0	0	Register Feedback	Register	Active Low
10	1	0	0	0			Active High
11	0	1	1	0		Combinatorial	Active Low
12	1	1	1	0			Active High

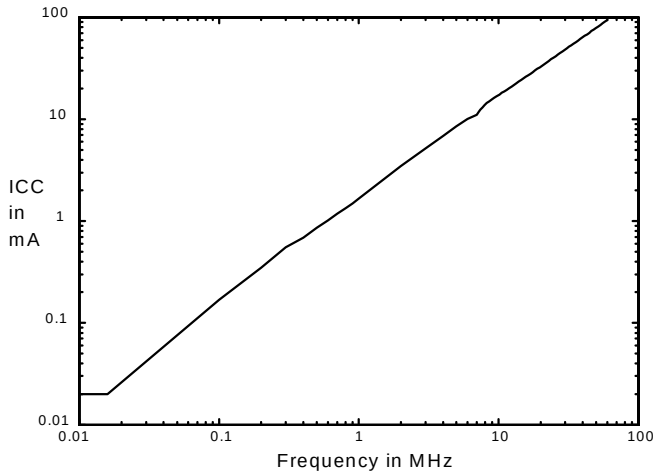


Figure 6 - Typical ICC vs. Input Clock Frequency for the 18LV8Z

Design Security

The PEEL18LV8Z provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The PLD programmer sets the security bit, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 64-bit code to be programmed into the PEEL18LV8Z if the software option is used. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

Programming Support

ICT's JEDEC file translator allows easy conversion of existing 20 pin PLD designs to the PEEL18LV8Z, without the need for redesign. ICT supports a broad range of popular third party design entry systems, including Data I/O Synario and Abel, Logical Devices CUPL and others. ICT also offers (for free) its proprietary PLACE software, an easy-to-use entry level PC-based software development system.

Programming support includes all the popular third party programmers; Data I/O, Logical Devices, and numerous others.

This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Table 1 - Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to Ground	-0.5 to + 6.0	V
V_I, V_O	Voltage Applied to Any Pin[2]	Relative to Ground[1]	-0.5 to 5.5	V
I_O	Output Current	Per Pin (I_{OL} , I_{OH})	± 25	mA
T_{ST}	Storage Temperature		-65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 Seconds	+300	°C

Table 2 - Operating Range

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc	Supply Voltage[3]	Commercial / Industrial	2.7	3.6	V
TA	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
T_{RVCC}	V_{CC} Rise Time	See Note 4		250	ms

Table 3 - D. C. Electrical Characteristics Over the operating range (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = -2.0 mA	V_{CC} - 0.5		V
V_{OHC}	Output HIGH Voltage - CMOS	V_{CC} = Min, I_{OH} = -10 A	V_{CC} - 0.3		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 8.0 mA		0.4	V
V_{OLC}	Output LOW Voltage - CMOS	V_{CC} = Min, I_{OL} = 10 A		0.15	V
V_{IH}	Input HIGH Voltage	V_{CC} = 3.3 V	2.0	5.5	V
V_{IL}	Input LOW Voltage	V_{CC} = 3.3 V	-0.3	0.8	V
V_H	Input Voltage Hysteresis		0.2		V
I_{IN}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}, I/O = High Z		+/- 1	µA
		V_{CC} = Min, GND ≤ V_{IN} ≤ 5.5V, I/O = High Z		25	µA
	I/O Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}, I/O = High Z		+/- 1	µA
		V_{CC} = Min, GND ≤ V_{IN} ≤ 5.5V, I/O = High Z		500	µA
I_{CCS}	V_{CC} Current, Standby	VIN = 0V or V_{CC}, All Outputs disabled[5]	5 (typ)	25	µA
I_{CC}[11]	V_{CC} Current, f=1MHz	VIN = 0V or V_{CC}, All Outputs disabled[5]	1.5 (typ)	3	mA
C_{IN}[8]	Input Capacitance	TA = 25°C, VCC = Max @ f = 1 MHz		6	pF
C_{OUT}[8]	Output Capacitance			12	pF

Table 4 - A.C. Electrical Characteristics

Over the operating range[9]

Symbol	Parameter	-25				I-35				Units
		3V±10%		3.3V±10%		3V±10%		3.3V±10%		
		Min	Max	Min	Max	Min	Max	Min	Max	
tPD	Input[6] to non-registered output in continuous mode[13]		30		25		40		35	ns
tOE	Input[6] to output enable[7]		30		25		40		35	ns
tOD	Input[6] to output disable[7]		30		25		40		35	ns
tCO1	Clock to Output		20		15		28		25	ns
tCO2	Clock to comb output delay via internal registered feedback		40		35		56		49	ns
tCF	Clock to Feedback		14		9		20		13	ns
tSC	Input[6] or feedback setup to clock	20		15		28		21		ns
tHC	Input[6] hold after clock	0		0		0		0		ns
tCL, tCH	Clock low time, clock high time[9]	20		13		28		18		ns
tCP	Min clock period Ext (tSC + tCO1)	40		30		56		39		ns
fMAX1	Internal feedback 1/ (tSC + tCF) [12]	29.4		41.6		20.8		29.4		MHz
fMAX2	External Feedback (1/ tCP) [12]	25		33.3		17.9		25.6		MHz
fMAX3	No Feedback 1/ (tCL + tCH) [12]	25		38.4		17.9		27.7		MHz
tAW	Asynchronous Reset Pulse Width	30		25		40		35		ns
tAP	Input to Asynchronous Reset		30		25		40		35	ns
tAR	Asynchronous Reset recovery time		30		25		40		35	ns
tRESET	Power-on reset time for registers in clear state[14]		5		5		5		5	µs

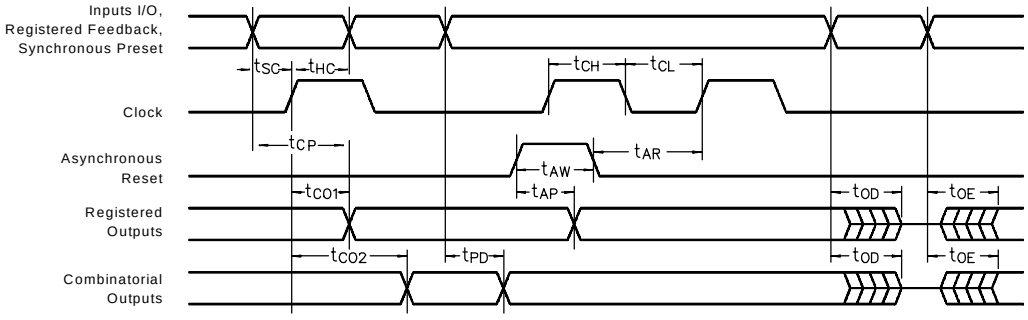


Figure 7 - Switching Waveforms

Notes:

1. Minimum DC input is -0.5V, however, inputs may undershoot to -2.0V for periods less than 20 ns.
2. V*I* and V*O* are not specified for program / verify operation.
3. The Supply Voltage range of 2.7 to 3.6V was chosen to allow this part to be used in both 3V ±10% and 3.3V ±10% applications.
4. Test Points for Clock and VCC in tR and tF are referenced at the 10% and 90% levels.
5. I/O pins are 0V and V*CC* .
6. "Input" refers to an input pin signal.
7. t*OE* is measured from input transition to V *REF*± 0.1V, T*OD* is measured from input transition to V*OH* -0.1V or V*OL* +0.1V; V*REF* =V*L*.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (Unless otherwise specified).
10. Test one output at a time for duration of less than 1 second.
11. I*CC* for a typical application: This parameter is tested with the device programmed as an 8-bit Counter.
12. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design process modification that might affect operational frequency.
13. tPD , tOE , tOD , tCO , tSC , and tAP are approximately 5 ns. slower on the first transaction from sleep mode.
14. All inputs at GND.

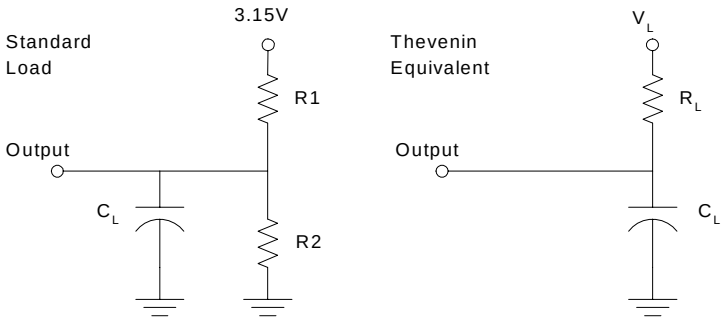


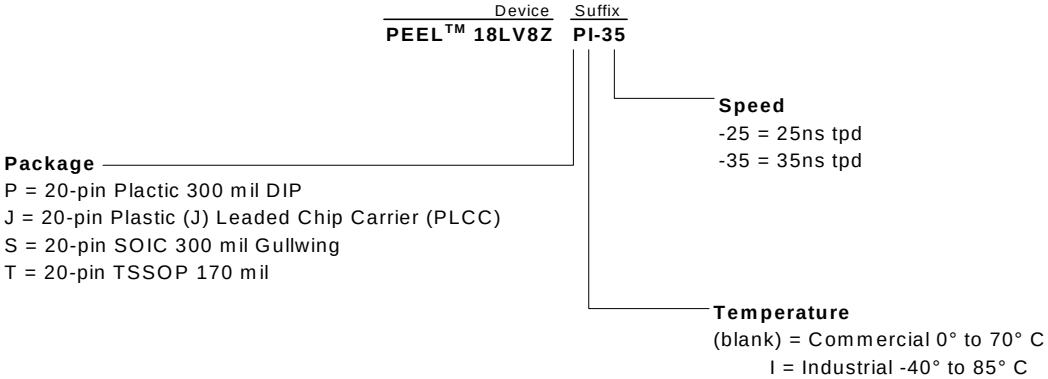
Figure 8 - PEEL™ Device and Array Test Loads

Technology	R1	R2	RL	VL	CL
CMOS	284 kΩ	258 kΩ	113 kΩ	1.275V	33 pF
TTL	308 Ω	433 Ω	180 Ω	1.840V	33 pF

Ordering Information

Part Number	Speed	Temperature	Package
PEEL18LV8ZP-25	25ns	Commercial	20-pin Plastic DIP
PEEL18LV8ZPI-35	35ns	Industrial	20-pin Plastic DIP
PEEL18LV8ZJ-25	25ns	Commercial	20-pin PLCC
PEEL18LV8ZJI-35	35ns	Industrial	20-pin PLCC
PEEL18LV8ZS-25	25ns	Commercial	20-pin SOIC
PEEL18LV8ZSI-35	35ns	Industrial	20-pin SOIC
PEEL18LV8ZT-25	25ns	Commercial	20-pin TSSOP
PEEL18LV8ZTI-35	35ns	Industrial	20-pin TSSOP

Part Number



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