PEEL™20CG10A -5/-7/-10/-15/L-15/-25
CMOS Programmable Electrically Erasable Logic

3

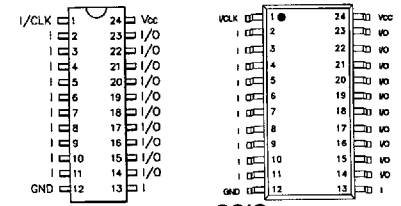
Features

- **High Speed/Low Power**
  - — Speeds ranging from 5ns to 25ns
  - — Power as low as 67mA at 25MHz
- **Electrically Erasable Technology**
  - — Superior factory testing
  - — Reprogrammable in plastic package
  - — Reduces retrofit and development costs
- **Development/Programmer Support**
  - — Third party software and programmers
  - — ICT Place Development Software and PDS-3 programmer
  - — PLD-to-PEEL JEDEC file translator
- **Architectural Flexibility**
  - — 92 product term X 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Up to 12 configurations per macrocell
  - — Synchronous preset, asynchronous clear
  - — Independent output enables
  - — 24-pin DIP, SOIC and 28-pin PLCC packages
- **Application Versatility**
  - — Replaces random logic
  - — Super-sets standard PLDs (PAL, GAL, EPLD)
  - — Enhanced Architecture fits more logic than ordinary PLDs

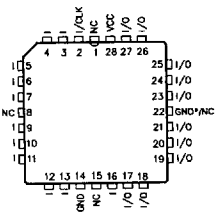
General Description

The PEEL20CG10A is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL20CG10A offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL20CG10A is available in 24-pin DIP, SOIC and 28-pin PLCC packages with speeds ranging from 5ns to 25ns with power consumption as low as 67mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability thus, ensuring the highest quality possible. The PEEL20CG10A architecture allows it to replace over 20 standard 24-pin PLDs (PAL, GAL, EPLD etc.). It also provides additional architecture features so more logic can be put into every design. ICT's JEDEC file translator instantly converts existing 24-pin PLDs to the PEEL20CG10A without the need to rework the existing design. Development and programming support for the PEEL20CG10A is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

Pin Configuration (Figure 1)



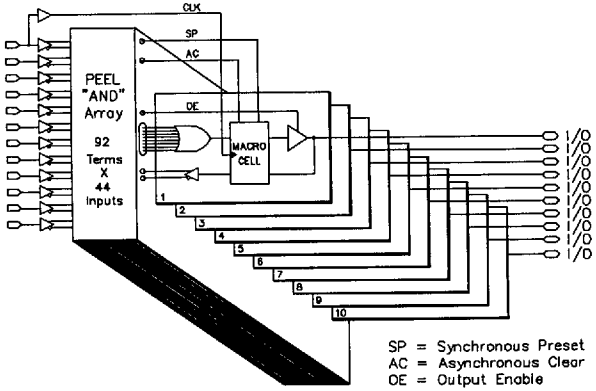
DIP SOIC



*Optional extra ground pin for -5 speed grade.

PLCC

Block Diagram (Figure 2)



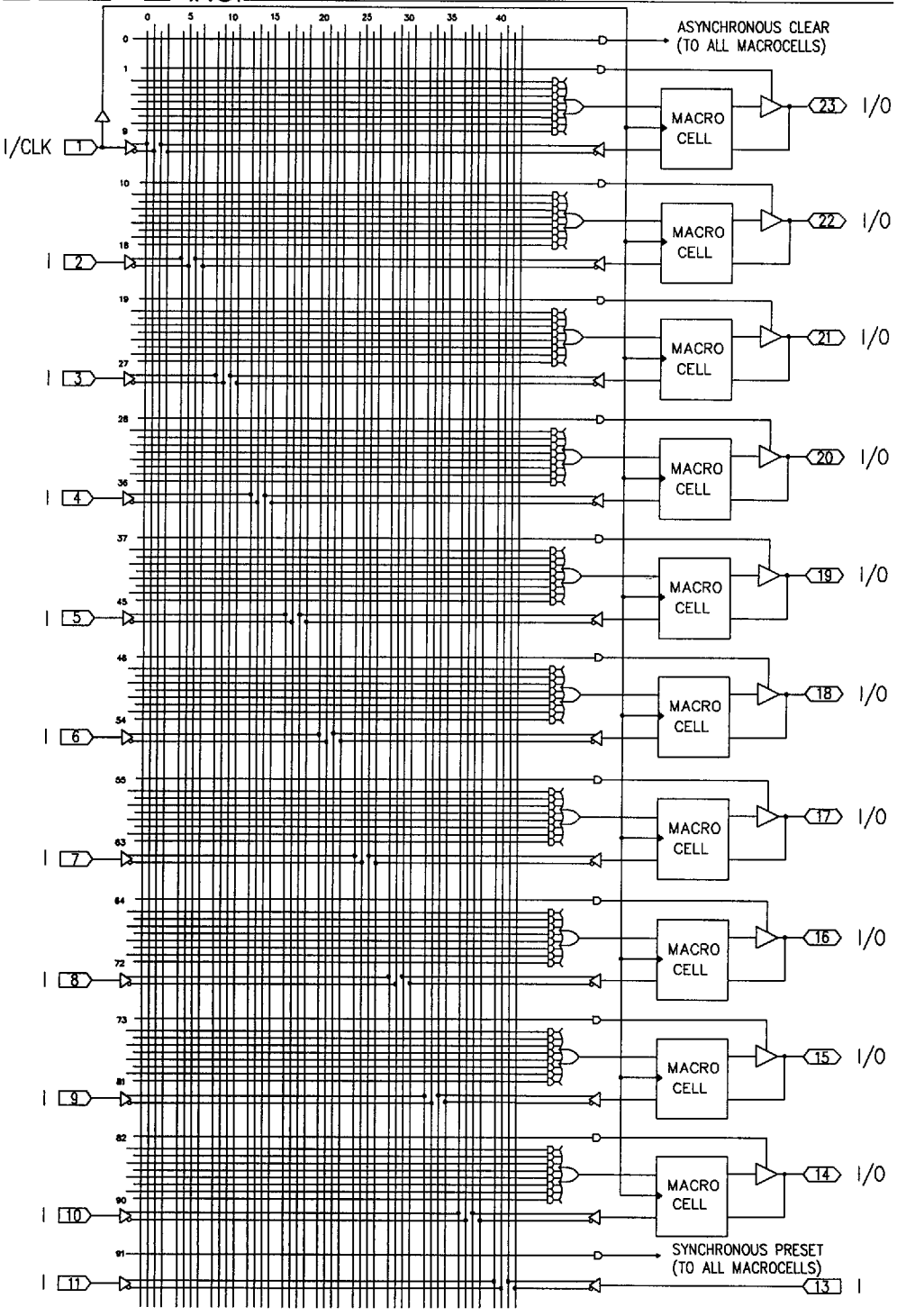


Figure 3. PEEL20CG10A Logic Array Diagram

Function Description

The PEEL20CG10A implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL20CG10A architecture is illustrated in the block diagram of Figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL20CG10A can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL20CG10A (shown in Figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

92 product terms:

- 80 product terms (8 per I/O)
- 10 output enable terms (one for each I/O)
- 1 global synchronous present term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a "don't care" state exists and that term will always be TRUE.

When programming the PEEL20CG10A, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program the connections on unused product terms so that they will have no effect on the output function).

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL20CG10A to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in Figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine: output polarity; output type (registered or non-registered); and input/feedback path (bi-directional I/O, combinatorial feedback, or register feedback). Table 1 shows the bit settings for each of the twelve macro-cell configurations.

Equivalent circuits for the twelve macrocell configurations are illustrated in Figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10) the macrocell provides eight configurations that are unavailable in any PAL device.

Output Type

The signal from the OR array can be fed directly to the output pin or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

The PEEL20CG10A macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O); directly from the Q output of the flip-flop (registered feedback); or directly from the OR gate (combinatorial feedback).

Bi-directional I/O

The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback

The signal-select multiplexer gives the macrocell the ability to feedback the output directly from the OR gate, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7 and 8 in Figure 5.)

Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is to be combinatorial or registered. When implementing configurations 11 and 12 in Figure 5, the register can be used for internal latching of data while leaving the external output free for combinatorial functions.

Design Security

The PEEL20CG10A provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

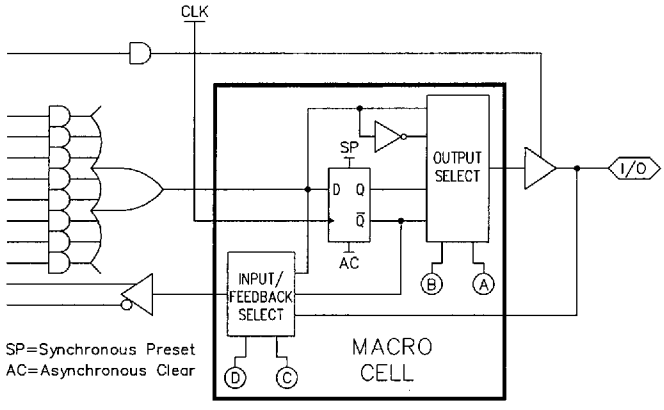


Figure 4. Block Diagram of the PEEL20CG10A I/O Macrocell

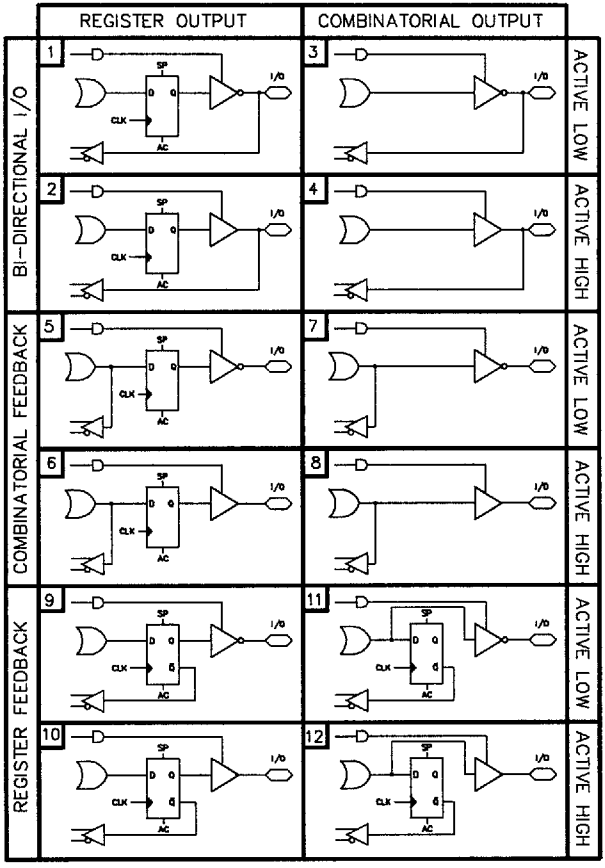


Figure 5. Equivalent Circuits for the Twelve Configurations of the PEEL20CG10A I/0 Macrocell.

Configuration #	A	B	C	D	Input/Feedback Select	Output Select	
1	0	0	1	0	Bi-Directional I/O	Register	Active Low
2	1	0	1	0	"	"	Active High
3	0	1	0	0	"	Combinatorial	Active Low
4	1	1	0	0	"	"	Active High
5	0	0	1	1	Combinatorial Feedback	Register	Active Low
6	1	0	1	1	"	"	Active High
7	0	1	1	1	"	Combinatorial	Active Low
8	1	1	1	1	"	"	Active High
9	0	0	0	0	Register Feedback	Register	Active Low
10	1	0	0	0	"	"	Active High
11	0	1	1	0	"	Combinatorial	Active Low
12	1	1	1	0	"	"	Active High

Table 1. PEEL20CG10A Macrocell Configuration Bits

Absolute Maximum Ratings

This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin[2]	Relative to Ground[1]	-0.5 to VCC + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	±25	mA
T_{ST}	Storage Temperature		-65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	
T_A	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
T_R	Clock Rise Time	See Note 3		20	ns
T_F	Clock Fall Time	See Note 3		20	ns
T_{RVCC}	V_{CC} Rise Time	See Note 3		250	ms

D.C. Electrical Characteristics Over the operating range

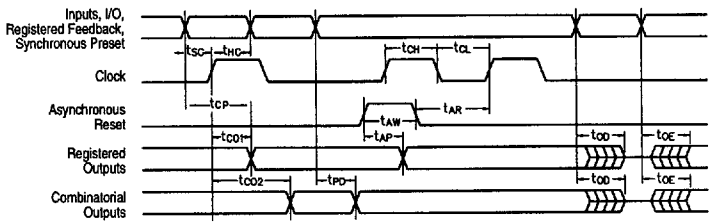
Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = -4.0mA		2.4		V
V_{OHC}	Output HIGH Voltage - CMOS[13]	V_{CC} = Min, I_{OH} = -10µA		V_{CC} - 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA			0.5	V
V_{OLC}	Output LOW Voltage - CMOS[13]	V_{CC} = Min, I_{OL} = 10µA			0.1	V
V_{IH}	Input HIGH Level			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level			-0.3	0.8	V
I_{IL}	Input and I/O Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}			±10	µA
I_{SC}	Output Short Circuit Current	V_{CC} = 5V, V_O = 0.5V[9], T_A = 25°C		-30	-135	mA
I_{CC}[10]	VCC Current, f=1MHz	V_{IN} = 0V or 3V All outputs disabled[4]	-5		140	mA
			-7		155	
			-10/I-10		135/145	
			-15/I-15		135/145	
			L-15		75	
			-25/I-25		67/75	
C_{IN}[7]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz			6	pF
C_{OUT}[7]	Output Capacitance				12	pF

A.C. Electrical Characteristics

Over the Operating Range [8, 11]

Symbol	Parameter	-5		-7		-10 / I-10		-15 / I-15		L-15		-25 / I-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input[5] to non-registered output		5		7.5		10		15		15		25	ns
t_{OE}	Input[5] to output enable[6]		5		7.5		10		15		15		25	ns
t_{OD}	Input[5] to output disable[6]		5		7.5		10		15		15		25	ns
t_{CO1}	Clock to output		4		5.5		6		8		10		15	ns
t_{CO2}	Clock to comb. output delay via int. registered feedback		7.5		10		12		17		19		35	ns
t_{CF}	Clock to Feedback		2.5		3.5		4		5		6		9	ns
t_{SC}	Input[5] or feedback setup to clk	3		3		4/5		8		10		15		ns
t_{HC}	Input[5] hold after clock	0		0		0		0		0		0		ns
t_{CL}, t_{CH}	Clk low time, clock high time[8]	2.5		3		5		6		7.5		13		ns
t_{CP}	Min Clk period Ext (t_{SC} + t_{CO1})	7		8.5		11		18		20		30		ns
f_{MAX1}	Int. Feedback ($1/t_{SC}+t_{CF}$)[12]	181.8		142		111		76.9		62.5		41.6		MHz
f_{MAX2}	External Feedback ($1/t_{CP}$)[12]	142.8		117		90.9		62.5		50		33.3		MHz
f_{MAX3}	No Feedback ($1/t_{CL}+t_{CH}$)[12]	200		166		125		83.3		66.7		38.4		MHz
t_{AW}	Asynch. Reset pulse width	5		7.5		10		15		15		25		ns
t_{AP}	Input[5] to Asynchronous Reset		5		7.5		10		15		18		25	ns
t_{AR}	Asynch. Reset recovery time		5		7.5		10		15		18		25	ns
t_{RESET}	Power-on reset time for registers in clear state		5		5		5		5		5		5	µs

Switching Waveforms



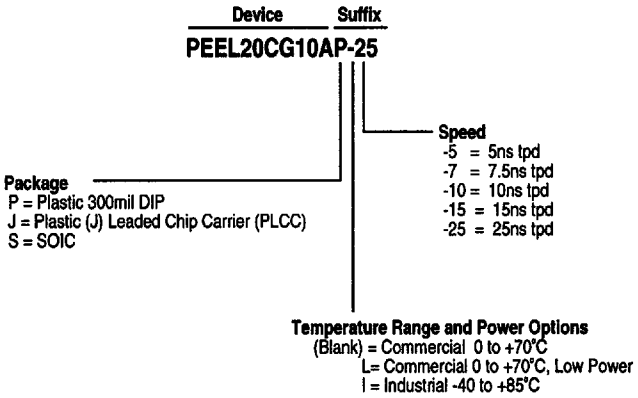
Notes

1. Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
2. V_I and V_O are not specified for program/verify operation.
3. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
4. I/O pins are 0V or Vcc.
5. "Input" refers to an Input pin signal.
6. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to V_{OH} - 0.1V or V_{OL} + 0.1V; $V_{REF} = V_L$ see test loads in Section 6 of this Data Book.
7. Capacitances are tested on a sample basis.
8. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
9. Test one output at a time for a duration of less than 1 sec.
10. ICC for a typical application: This parameter is tested with the device programmed as an 10-bit Counter.
11. PEEL Device test loads are specified in Section 6 of this Data Book.
12. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.
13. Available only for 20CG10A-15/I-15/L-15/25/I-25 grades.

Ordering Information

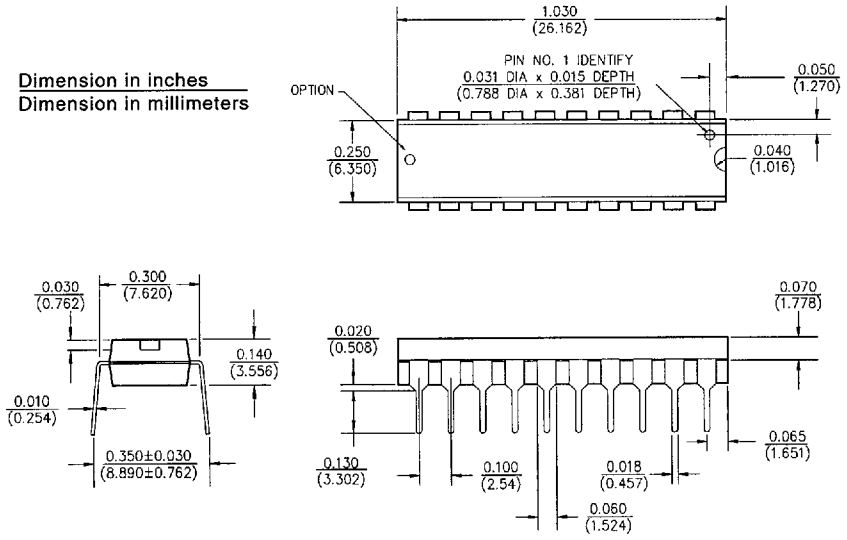
PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PEEL20CG10AJ-5	5ns	C	J28
PEEL20CG10AP-7	7.5ns	C	P24
PEEL20CG10API-7	7.5ns	I	P24
PEEL20CG10AJ-7	7.5ns	C	J28
PEEL20CG10AJI-7	7.5ns	I	J28
PEEL20CG10AS-7	7.5ns	C	S24
PEEL20CG10ASI-7	7.5ns	I	S24
PEEL20CG10AP-10	10ns	C	P24
PEEL20CG10API-10		I	P24
PEEL20CG10AJ-10	10ns	C	J28
PEEL20CG10AJI-10		I	J28
PEEL20CG10AS-10	10ns	C	S24
PEEL20CG10ASI-10		I	S24
PEEL20CG10AP-15	15ns	C	P24
PEEL20CG10API-15		I	P24
PEEL20CG10AJ-15	15ns	C	J28
PEEL20CG10AJI-15		I	J28
PEEL20CG10AS-15	15ns	C	S24
PEEL20CG10ASI-15		I	S24
PEEL20CG10APL-15	15ns	C	P24
PEEL20CG10AJL-15	15ns	C	J28
PEEL20CG10ASL-15	15ns	C	S24
PEEL20CG10AP-25	25ns	C	P24
PEEL20CG10API-25		I	P24
PEEL20CG10AJ-25	25ns	C	J28
PEEL20CG10AJI-25		I	J28
PEEL20CG10AS-25	25ns	C	S24
PEEL20CG10ASI-25		I	S24

Part Number

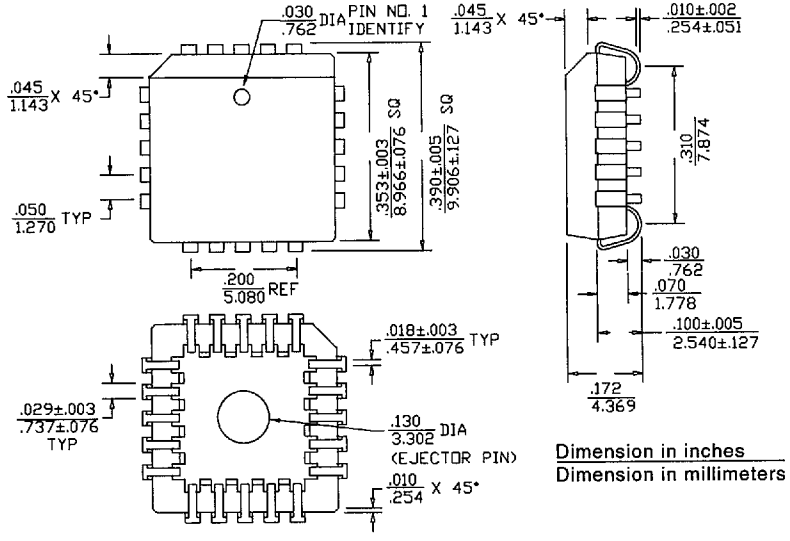


Package Diagrams (Drawings are not necessarily to scale.)

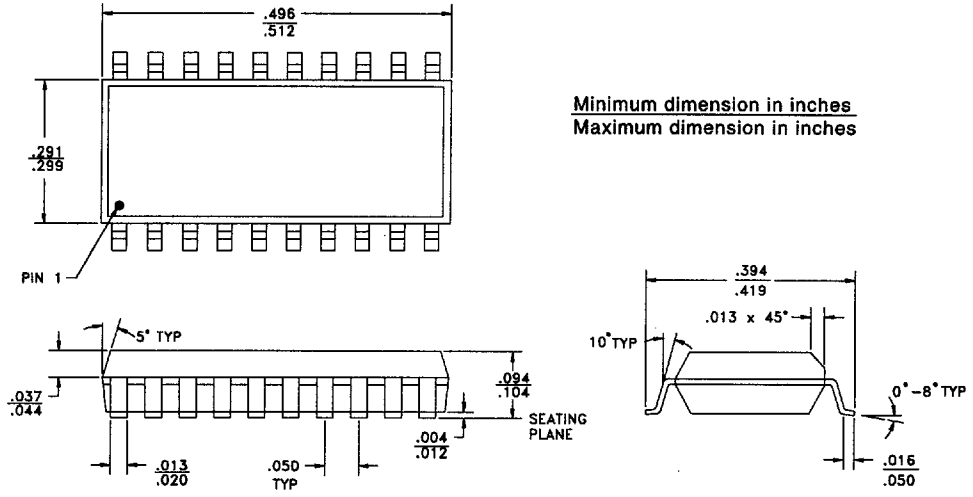
Dimension in inches
Dimension in millimeters



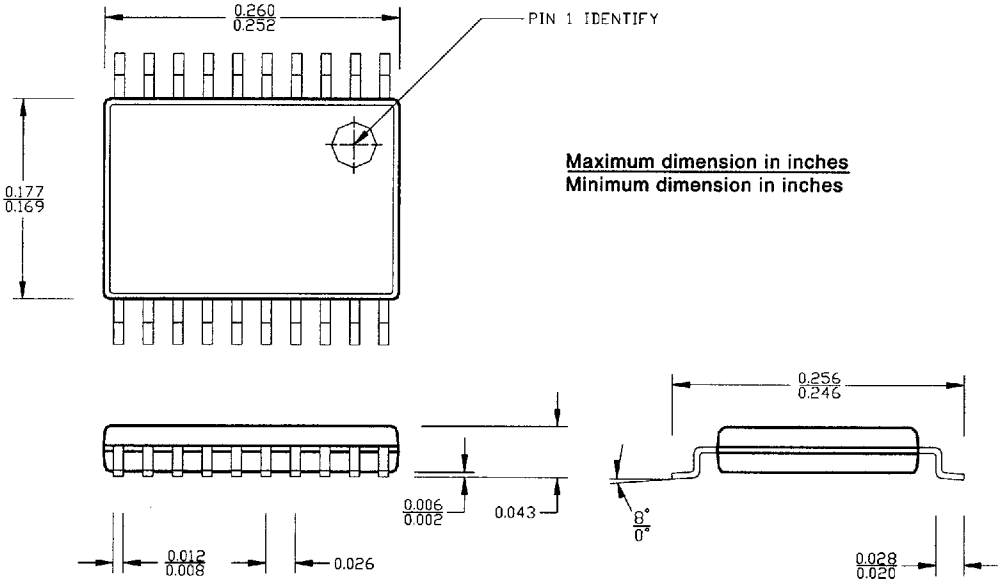
20-Pin Plastic DIP (P20)



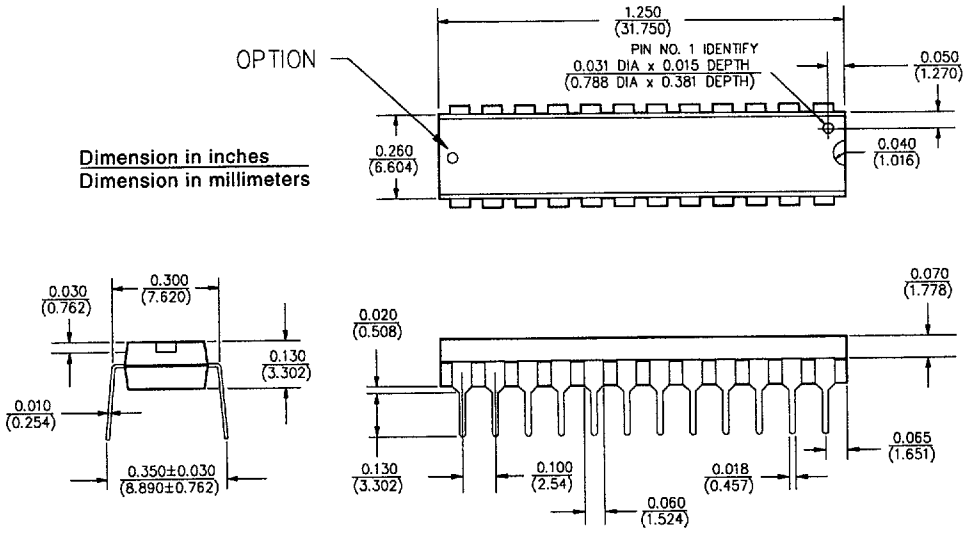
20-Pin PLCC (J20)



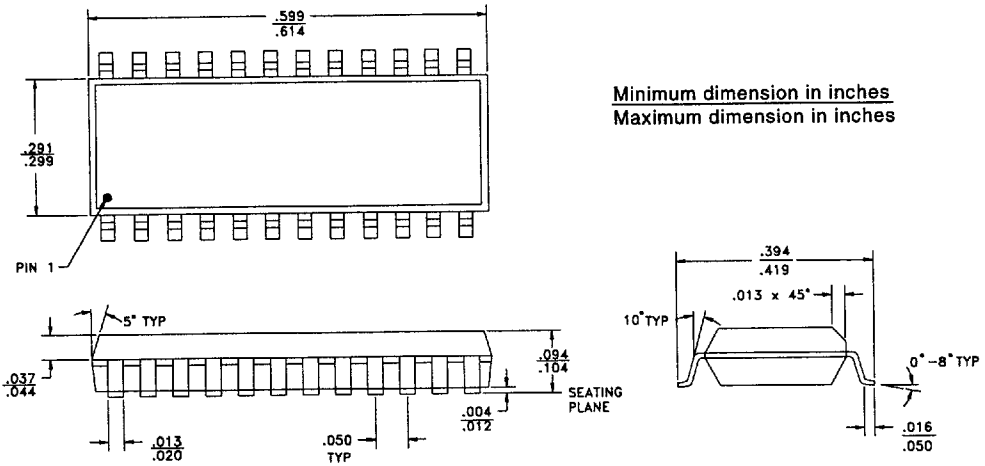
20-Pin SOIC (S20)



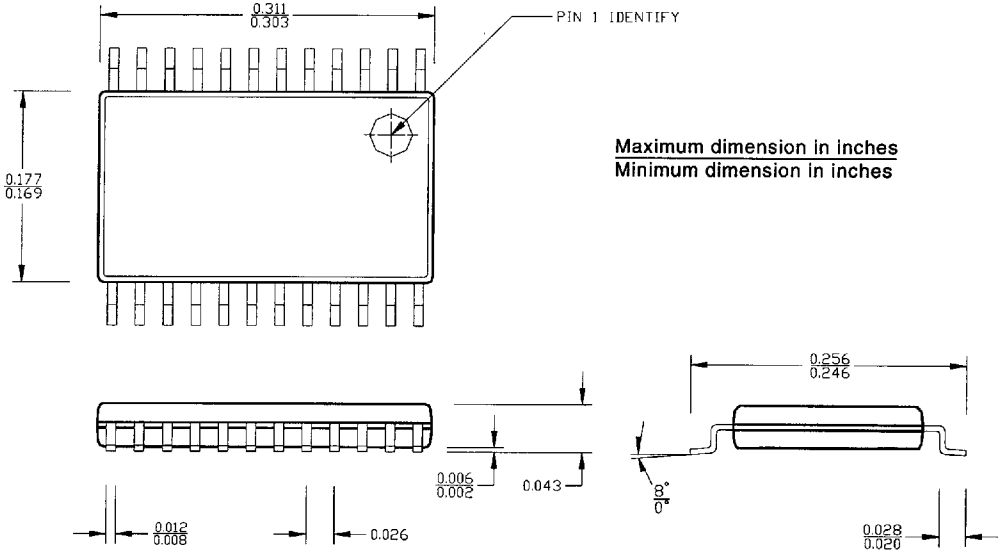
20-Pin TSSOP (T20)



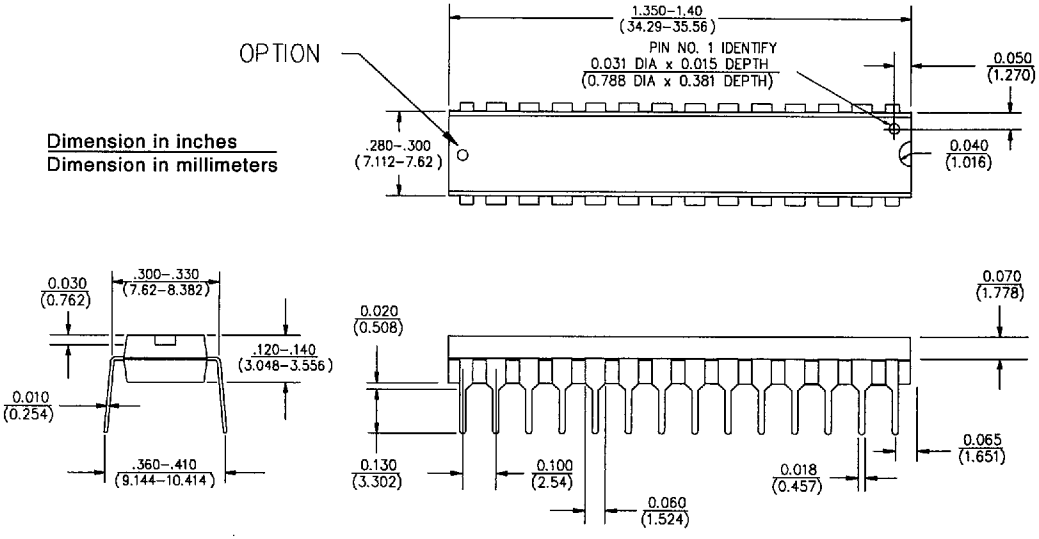
24-Pin Plastic DIP (P24)



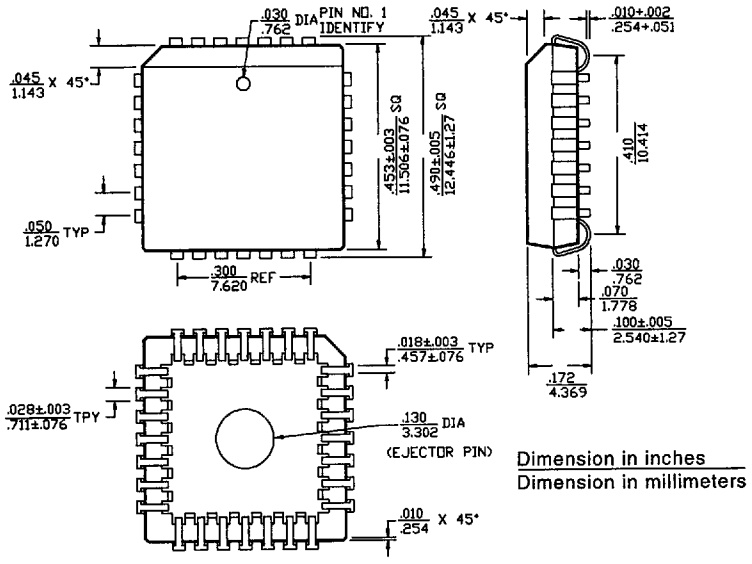
24-Pin SOIC (S24)



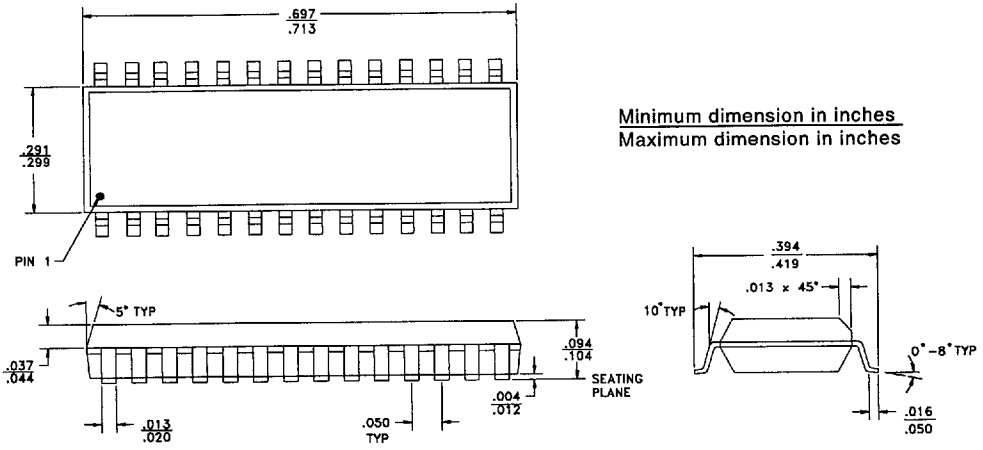
24-Pin TSSOP (T24)



28-Pin Plastic Dip (P28)

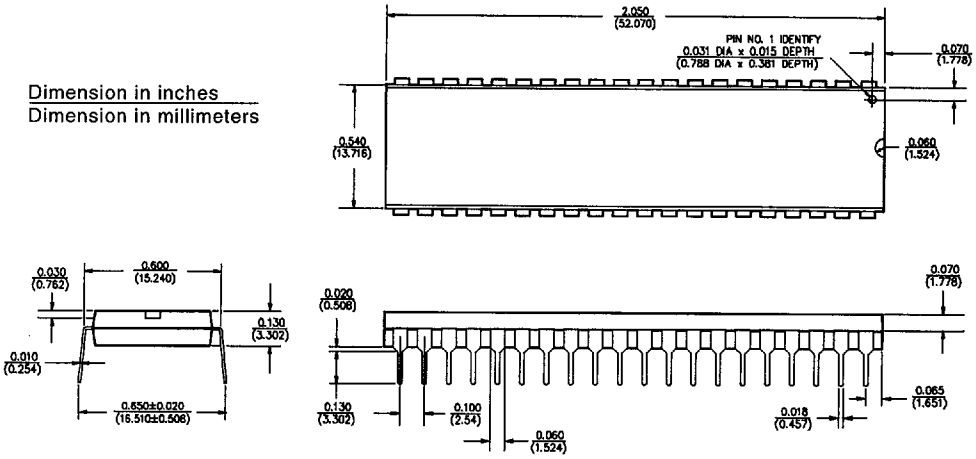


28-Pin PLCC (J28)

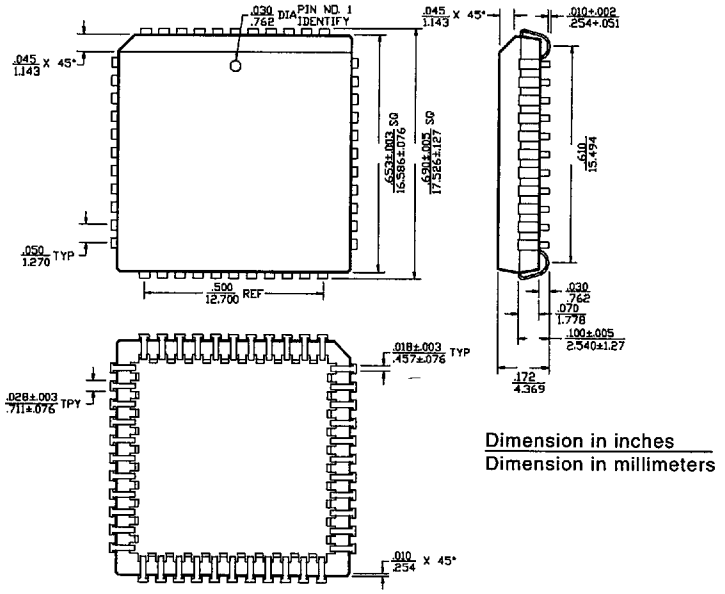


28-Pin SOIC (S28)

Dimension in inches
Dimension in millimeters



40-Pin Plastic DIP (T40)



Dimension in inches
Dimension in millimeters

44-Pin PLCC (J44)