MAXIM

CMOS 8-Bit DAC with Output Amplifier

General Description

The AD7224 is a precision voltage-output CMOS digital-to-analog converter (DAC) which includes an output amplifier on chip. Only an external reference source is required for operation and the fully specified accuracy is achieved with no external trims.

Double buffered interface logic is included to allow simultaneous updating in systems which have several DAC channels in operation. Control is provided by $\overline{CS}$, $\overline{WR}$, and $\overline{LDAC}$ (Load DAC) inputs. A $\overline{RESET}$ input is provided which acts as a zero override. All logic inputs are compatible with TTL and 5V CMOS logic levels.

Specified Performance is guaranteed for reference inputs ranging from +2V to +12.5V when using dual supplies. With a +10V reference the performance is also specified for single supply operation. The DAC output can drive +10V into a 2kΩ load.

Applications

Automatic Calibration

Motion Control

Digital Attenuators

Function Generators

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Features

- Voltage Output
- Complete DAC with Output Amplifier
- Single or Dual Supply Operation
- 1 LSB Unadjusted Error
- Double Buffered Logic Inputs

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7224KN	0°C to +70°C	Plastic DIP	±2 LSB
AD7224LN	0°C to +70°C	Plastic DIP	±1 LSB
AD7224C/D	0°C to +70°C	Dice	±2 LSB
AD7224KCWN	0°C to +70°C	Wide S.O.	±2 LSB
AD7224LCWN	0°C to +70°C	Wide S.O.	±1 LSB
AD7224BQ	-25°C to +85°C	CERDIP**	±2 LSB
AD7224CQ	-25°C to +85°C	CERDIP**	±1 LSB
AD7224TD	-55°C to +125°C	Ceramic	±2 LSB
AD7224UD	-55°C to +125°C	Ceramic	±1 LSB
AD7224TQ	-55°C to +125°C	CERDIP**	±2 LSB
AD7224UQ	-55°C to +125°C	CERDIP**	±1 LSB

* *All devices—18 lead packages*

** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

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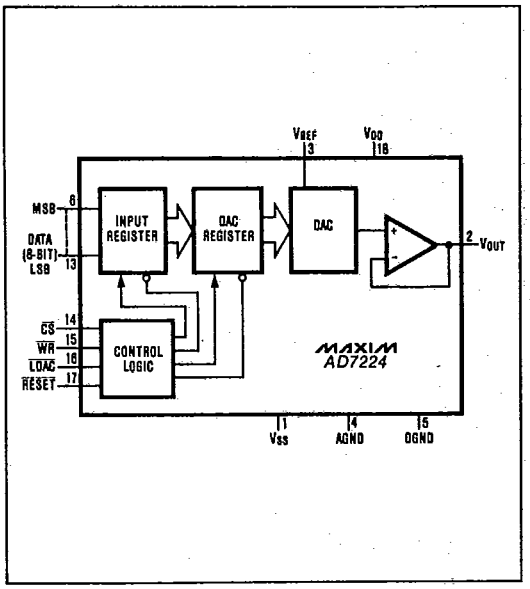
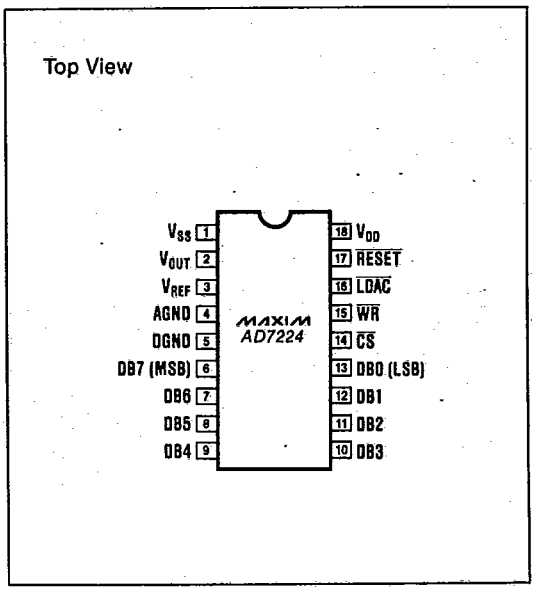
Functional Diagram



Pin Configuration



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CMOS 8-Bit DAC with Output Amplifier

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +17V
V_{DD} to DGND ..... -0.3V, +17V
AGND to DGND ..... -0.3V, V_{DD}
V_{SS} to DGND ..... -7V, V_{DD} + 0.3V
V_{DD} to V_{SS} ..... -0.3V, +24V
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
V_{REF} to AGND ..... -0.3V, V_{DD}
V_{OUT} to DGND ..... V_{SS}, V_{DD}

Power Dissipation (Any Package) to +75°C 450mW
Derating above +75°C ..... 6mW/°C
Operating Temperature
AD7224K/L ..... 0°C to +70°C
AD7224A/B ..... -25°C to +85°C
AD7224T/U ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering 10 secs) ..... +300°C

The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typical short circuit current to AGND is 25mA.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—AD7224, Dual Supply Operation

(V_{DD} = +11.4V to +16.5V, V_{SS} = -5V ±10%, AGND = DGND = 0V, V_{REF} = +2V to (V_{DD} - 4V) (Note 1), Over Temperature unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution				8			Bits
Total Unadjusted Error		V_{REF} = +10V V_{DD} = +15V ± 5%	AD7224L/C/U AD7224K/B/T			±1 ±2	LSB
Relative Accuracy		AD7224L/C/U AD7224K/B/T				±½ ±1	LSB
Differential Nonlinearity		Guaranteed Monotonic				±1	LSB
Full Scale Error		AD7224L/C/U AD7224K/B/T				±1 ±1½	LSB
Full Scale Temperature Coefficient		V_{REF} = +10V			±5		ppm/°C
Zero Code Error		AD7224L/C/U AD7224K/B/T				±20 ±30	mV
Zero Code Temperature Coefficient		AD7224L/C/U AD7224K/B/T			±30 ±50		μV/°C
REFERENCE INPUT							
Reference Input Voltage Range	V_{REF}			2		V_{DD} - 4	V
Reference Input Resistance	V_{REF}			8			kΩ
Reference Input Capacitance (Code Dependent, Note 2)	C_{REF}	DAC at full scale code.				100	pF
DIGITAL INPUTS							
Digital Input High Voltage	V_{INH}			2.4			V
Digital Input Low Voltage	V_{INL}					0.8	V
Digital Input Leakage Current		V_{IN} = 0V or V_{DD}				±1	μA
Digital Input Capacitance (Note 2)						8	pF

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CMOS 8-Bit DAC with Output Amplifier

ELECTRICAL CHARACTERISTICS—AD7224, Dual Supply Operation (Continued)

(V_{DD} = +11.4V to +16.5V, V_{SS} = -5V ±10%, AGND = DGND = 0V, V_{REF} = +2V to (V_{DD} - 4V) (Note 1), Over Temperature unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate (Note 2)			2.5	10		V/µs
Voltage Output Settling Time (Note 5)		To 1/2 LSB, V_{REF} = +10V		2	5	µs
Digital Feedthrough (Notes 3, 4)		All 0's to all 1's code change, V_{REF} = 0V		50		nV-s
Output Load Resistance		V_{OUT} = +10V	2			kΩ
POWER SUPPLIES						
V_{DD} Range		For Specified Performance	+11.4		+16.5	V
V_{SS} Range		For Specified Performance	-4.5		-5.5	V
Positive Supply Current	I_{DD}	Outputs unloaded, at V_{INL}/V_{INH} T_A = 25°C Over Temp			4 6	mA
Negative Supply Current	I_{SS}	Outputs unloaded, at V_{INL}/V_{INH} T_A = 25°C Over Temp			3 5	mA
SWITCHING CHARACTERISTICS (Note 2)						
Chip Select to Write Setup Time	t_{CS}		0			ns
Load DAC to Write Setup Time	t_{LS}		0			ns
Chip select to Write Hold Time	t_{CH}		0			ns
Load DAC to Write Setup Time	t_{LH}		0			ns
Data Valid to Write Setup Time	t_{DS}	T_A = 25°C Over Temp	90 100			ns
Data Valid to Write Hold Time	t_{DH}		10			ns
Write Pulse Width	t_{WR}	T_A = 25°C Over Temp	150 200			ns
Chip Select Pulse Width	t_{CW}	T_A = 25°C Over Temp	150 200			ns
Reset Pulse Width	t_{RS}	T_A = 25°C Over Temp	150 200			ns
Load DAC ($\overline{LDAC}$) Pulse Width	t_{LD}	T_A = 25°C Over Temp	150 200			ns

Note 1: Maximum possible reference voltage.
Note 2: Sample tested at 25°C to ensure compliance.
Note 3: Guaranteed, but not 100% production tested.
Note 4: Feedthrough is reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.
Note 5: Positive or negative full scale change.

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CMOS 8-Bit DAC with Output Amplifier

ELECTRICAL CHARACTERISTICS—AD7224, Single Supply Operation

(V_{DD} = +15V ± 5%, V_{SS} = AGND = DGND = 0V, V_{REF} = +10V (Note 1), Over Temperature unless otherwise stated.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution			8			Bits
Total Unadjusted Error					±2	LSB
Differential Nonlinearity		Guaranteed Monotonic			±1	LSB
REFERENCE INPUT						
Reference Input Resistance	R_{REF}		8			kΩ
Reference Input Capacitance (Code Dependent)(Note 2)	C_{REF}	DAC at full scale code			100	pF
DIGITAL INPUTS						
Digital Input High Voltage	V_{INH}		2.4			V
Digital Input Low Voltage	V_{INL}				0.8	V
Digital Input Leakage Current		V_{IN} = 0V to V_{DD}			±1	μA
Digital Input Capacitance (Note 2)					8	pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate (Note 2)			2.5	10		V/μs
Output Settling Time (Note 2)		To 1/2 LSB, Positive FS Chg Negative FS Chg		2 3	5 8	μs
Digital Feedthrough (Notes 3, 4)		All 0's to all 1's code change, V_{REF} = 0V		50		nV-s
Output Load Resistance		V_{OUT} = +10V	2			kΩ
POWER SUPPLIES						
V_{DD} Range		For Specified Performance	+14.25		+15.75	V
Positive Supply Current	I_{DD}	Outputs unloaded, at V_{INL}/V_{INH}; T_A = 25°C Over Temp			4 6	mA
SWITCHING CHARACTERISTICS (Note 2)						
Chip Select to Write Setup Time	t_{CS}		0			ns
Load DAC to Write Setup Time	t_{LS}		0			ns
Chip select to Write Hold Time	t_{CH}		0			ns
Load DAC to Write Setup Time	t_{LH}		0			ns
Data Valid to Write Setup Time	t_{DS}	T_A = 25°C Over Temp	90 100			ns
Data Valid to Write Hold Time	t_{DH}		10			ns
Write Pulse Width	t_{WR}	T_A = 25°C Over Temp	150 200			ns
Chip Select Pulse Width	t_{CW}	T_A = 25°C Over Temp	150 200			ns
Reset Pulse Width	t_{RS}	T_A = 25°C Over Temp	150 200			ns
Load DAC ($\overline{LDAC}$) Pulse Width	t_{LD}	T_A = 25°C Over Temp	150 200			ns

Note 1: Maximum possible reference voltage.
Note 2: Sample tested at 25°C to ensure compliance.
Note 3: Guaranteed, but not 100% production tested.
Note 4: Feedthrough is reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

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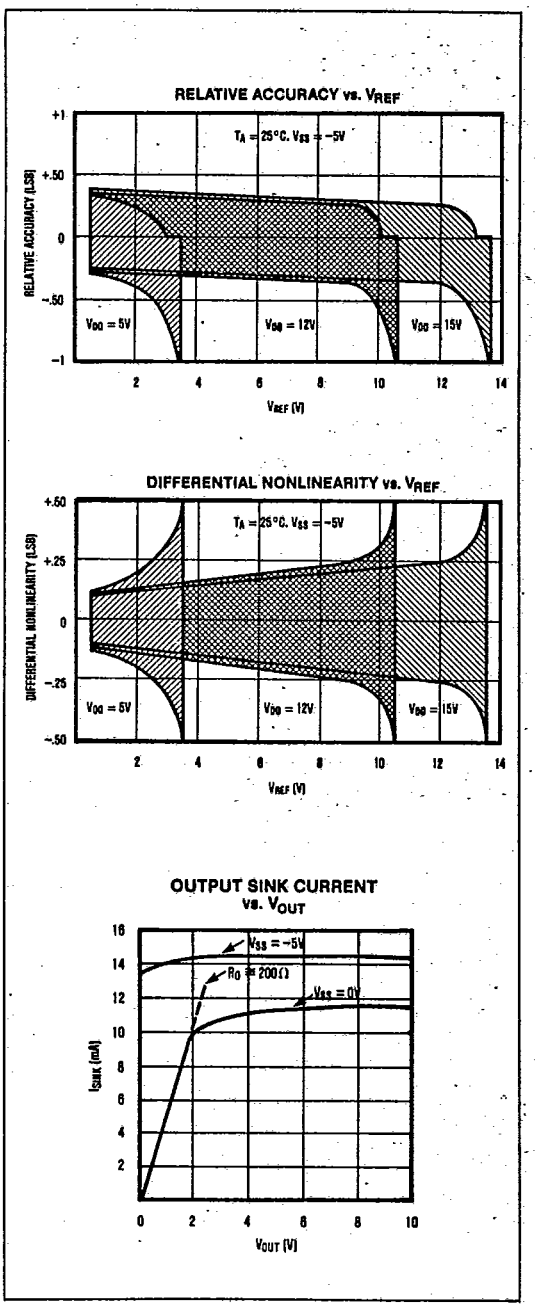
CMOS 8-Bit DAC with Output Amplifier

Typical Operating Characteristics



Detailed Description

D/A Section

The AD7224 contains an 8-bit digital-to-analog converter that operates in the voltage output mode. The output voltage is of the same polarity as the external reference voltage thus allowing single supply operation. A DAC switch pair arrangement on the AD7224 allows a reference voltage range from +2V to +12.5V.

The DAC consists of a stable thin-film resistor R-2R ladder and eight NMOS single pole, double-throw switches. A simplified circuit diagram is shown in Figure 1.

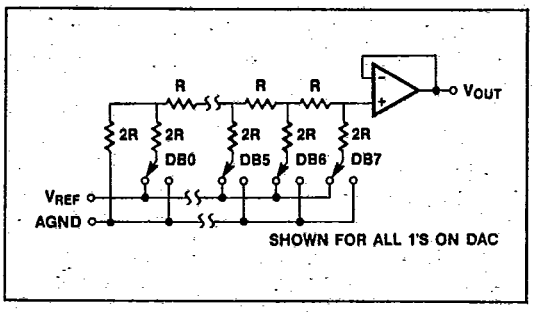


Figure 1. D/A Simplified Circuit Diagram

The input impedance at the V_{REF} pin is code dependent and varies from 8kΩ minimum to infinity. The lowest input impedance occurs when the DAC is loaded with the digital code 01010101. Therefore, it is important that the reference presents a low impedance under changing load conditions. Capacitance at the reference terminal is also code dependent and typically varies from 25pF to 50pF.

The V_{OUT} pin can be considered as a digitally-programmable voltage source with the output defined by:

$$V_{OUT} = D \cdot V_{REF}$$

where D is a fractional representation of the digital input code and can vary from 0 to 255/256.

Output Buffer Amplifier

The DAC's voltage output is buffered by a unity-gain CMOS voltage follower that slews at greater than 2.5V/μs. This amplifier is capable of driving a 2kΩ load to +10V. When driving a 2kΩ load in parallel with 100pF with full-scale transitions (0V to +10V or +10V to 0V), the output settles to 1/2LSB in less than 5μs. Typical dynamic response and settling performance of the AD7224 is shown in Figures 2 through 7.

The AD7224 can be operated single or dual supply. In single supply operation, Maxim's AD7224 can sink and source up to 5mA.

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CMOS 8-Bit DAC with Output Amplifier

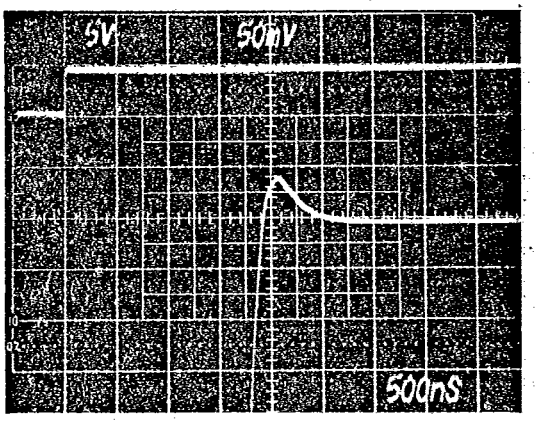

Figure 2. Positive Settling Time with V_{DD} = +15V, V_{SS} = -5V.

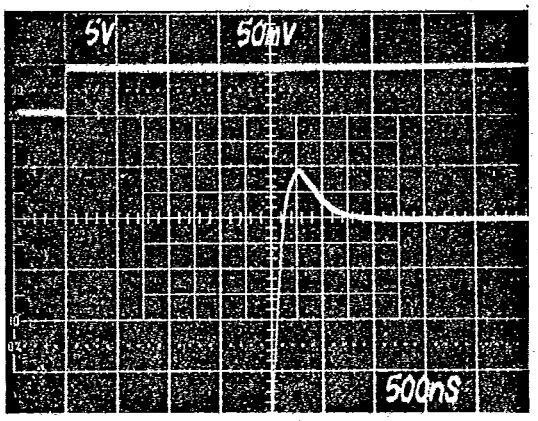

Figure 3. Positive Settling Time with V_{DD} = +15V, V_{SS} = 0V.

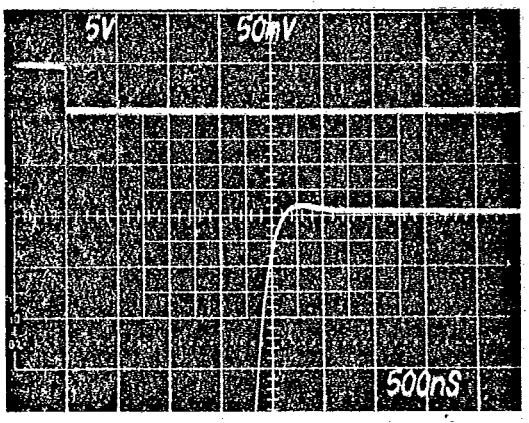

Figure 4. Negative Settling Time with V_{DD} = +15V, V_{SS} = -5V.

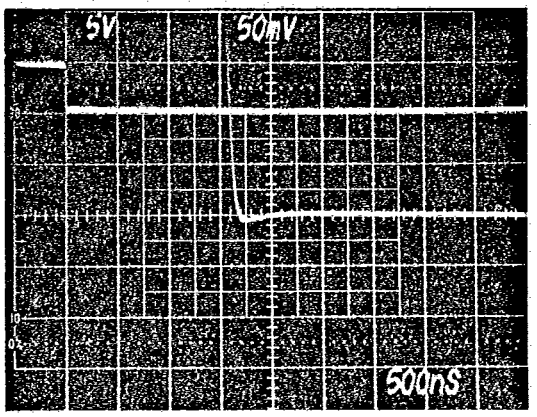

Figure 5. Negative Settling Time with V_{DD} = +15V, V_{SS} = 0V.

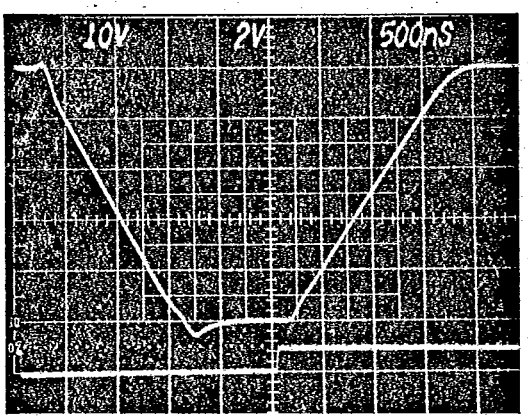

Figure 6. Dynamic Response with V_{DD} = +15V, V_{SS} = -5V.

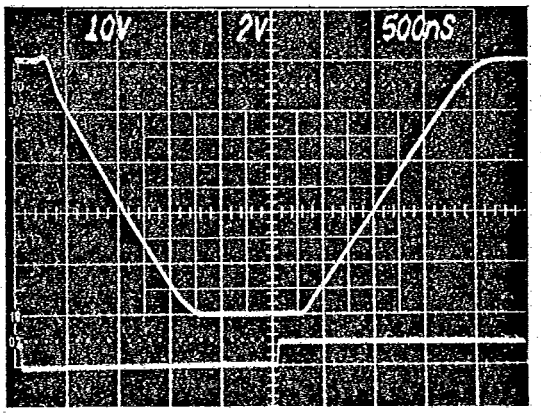

Figure 7. Dynamic Response with V_{DD} = +15V, V_{SS} = 0V.

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CMOS 8-Bit DAC with Output Amplifier

A simplified circuit diagram of the output buffer is shown is Figure 8. Input common-mode range to V_{SS} is provided by a PMOS input structure. The improved output circuitry incorporates a Maxim proprietary pull-down circuit to actively drive V_{OUT} to within typically +15mV of the negative supply (V_{SS}). Maxim's improved buffer circuitry allows the output to sink and source up to 5mA. This is especially important in single supply applications, where V_{SS} is connected to GND, so that zero error is kept at or under 1/2LSB (V_{REF} = +10V). A plot of output sink current versus output voltage is shown in the Typical Operating Characteristics section.

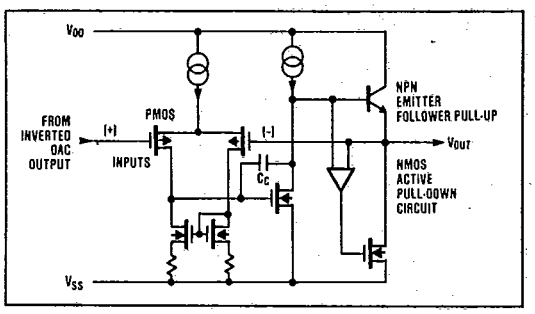

Figure 8. Simplified Output Buffer Circuit

Digital Inputs and Interface Logic

The digital inputs are compatible with both TTL and 5V CMOS logic. Power supply current, I_{DD} and I_{SS}, are specified for TTL input levels. The supply currents are somewhat dependent on input logic level and are highest when the AD7224 is driven from TTL, however, they can be significantly reduced if the inputs are driven as close to +5V as possible.

Table 1 shows the truth table for AD7224 operation. The part contains two registers, an input register and a DAC register. $\overline{CS}$ and $\overline{WR}$ control the loading of the input register while $\overline{LDAC}$ and $\overline{WR}$ control the transfer of information from the input to the DAC register. Only the data held in the DAC register will determine the converter's analog output.

All control signals are level-triggered and therefore either or both registers may be made transparent; the input register by keeping $\overline{CS}$ and $\overline{WR}$ "LOW," the DAC register by keeping $\overline{LDAC}$ and $\overline{WR}$ "LOW." The rising edge of the $\overline{WR}$ input latches input data.

The contents of both registers are reset by a low level on the $\overline{RESET}$ line. With both registers transparent, the $\overline{RESET}$ line overrides input data for the duration of the $\overline{RESET}$ pulse. If both registers are latched, a "LOW" pulse on the $\overline{RESET}$ will latch all 0's into the registers, with the output remaining at 0V after the reset pulse has been removed. The $\overline{RESET}$ line can be used to force 0V on the output at power-up, and is also useful as a zero override in system calibration cycles. Figure 9 shows the input control logic for the AD7224.

Table 1. AD7224 Truth Table

$\overline{RESET}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	Function
H	L	L	L	Both Registers are Transparent
H	X	H	X	Both Registers are Latched
H	H	X	H	Both Registers are Latched
H	H	L	L	Input Register Transparent
H	H	↓	L	Input Register Latched
H	L	L	H	DAC Register Transparent
H	L	↓	H	DAC Register Latched
L	X	X	X	Both Registers Loaded with all Zeros
↓	H	H	H	Both Registers Latched with all Zeros and Output Remains at Zero
↓	L	L	L	Both Registers are Transparent and Output Follows Input Data

H = High State, L = Low State, X = Don't Care

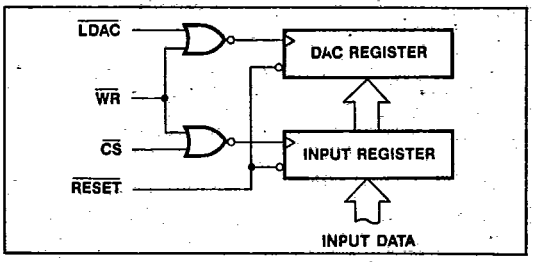

Figure 9. Input Control Logic

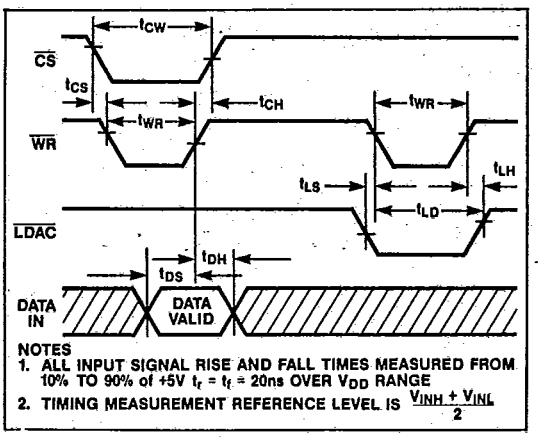

Figure 10. Write Cycle Timing Diagram

CMOS 8-Bit DAC with Output Amplifier

Applications Information

Power Supply and Reference Operating Ranges

The AD7224 is fully specified to operate with V_{DD} between +12V ± 5% and +15V ± 10% (+11.4V to +16.5V), and with V_{SS} from 0V to -5.5V. Eight bit performance is also guaranteed for single supply operation (V_{SS} = 0V), however zero code error is reduced when V_{SS} is -5V (see Output Buffer Amplifier section).

For adequate DAC and buffer operating range, the V_{REF} voltage must always be at least 4V below V_{DD}. The AD7224 is specified to operate with a reference input range of +2V to V_{DD} - 4V.

Ground Management

Digital or AC transient signals between AGND and DGND will create noise at the analog outputs. It is recommended that AGND and DGND be tied together at the DAC and that this point be tied to the highest quality ground that is available. If separate ground busses are used, then two clamp diodes (1N914 or equivalent) should be connected between AGND and DGND to keep the two ground busses within one diode drop of each other. To avoid parasitic device turn-on, AGND must not be allowed to be more negative than DGND. DGND should be used as supply ground for bypassing purposes.

Careful PCB ground layout techniques should be used to minimize crosstalk between the DAC output, the reference input, and the digital inputs. This is particularly important if the reference is driven from an AC source.

Unipolar Output

In unipolar operation, the output voltage and the reference input are the same polarity. The unipolar circuit configuration is shown in Figure 11. A slight increase in zero error occurs when the AD7224 is operated from a single supply (see Output Buffer Amplifier section). To avoid parasitic device turn-on, the voltage at V_{REF} must always be positive with respect to DGND. The unipolar code table is given in Table 2.

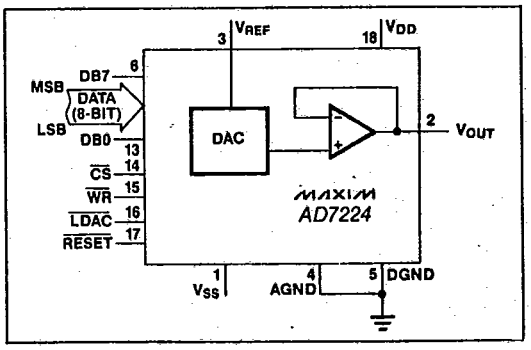

Figure 11. Unipolar Output Circuit

Table 2. Unipolar Code Table

DAC CONTENTS MSB	LSB	ANALOG OUTPUT
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0	0 0 0 0	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{256}\right)$
0 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0	0 0 0 0	0V

Note: $1LSB = (V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

Bipolar Output

The DAC output may be configured for bipolar operation using the circuit in Figure 12. Only one op-amp and two resistors are required. With R1 = R2:

$$V_{OUT} = V_{REF} \cdot (2D - 1)$$

where D is a fractional representation of the digital word in the DAC regiser.

Table 3 shows the digital code versus output voltage for the circuit in Figure 12.

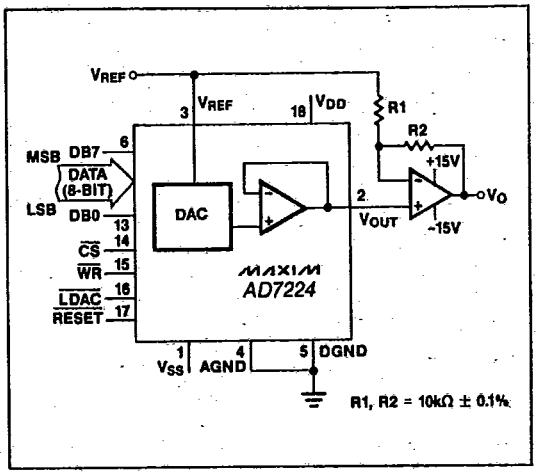

Figure 12. Bipolar Output Circuit

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Table 3. Bipolar (Offset Binary) Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0V
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Offsetting AGND

AGND can be biased above DGND to provide an arbitrary non-zero output voltage for a "zero" input code. This is shown in Figure 13. The output voltage at V_{OUT} is:

$$V_{OUT} = V_{BIAS} + (D \cdot V_{IN})$$

where D is a fractional representation of the digital input word and can vary from 0 to 255/256. For a given V_{IN}, increasing AGND above system GND will reduce the effective V_{DD}-V_{REF} which must be at least 4V to ensure specified operation. Note that V_{DD} and V_{SS} for the AD7224 must be referenced to DGND.

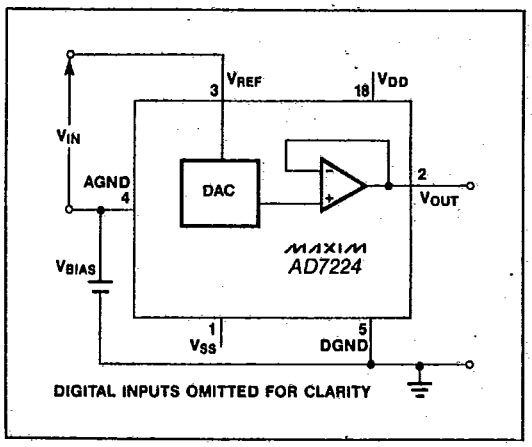

Figure 13. AGND Bias Circuit

Using an AC Reference

In applications where V_{REF} has AC signal components, the AD7224 has multiplying capability within the limits of the V_{REF} input range specifications. Figure 14 shows a technique for applying a sinewave signal to the reference input where the AC signal is biased up before being applied to V_{REF}. Output distortion is typically less than 0.1% with input frequencies up to 50kHz, and the typical -3dB frequency is 700kHz. Note that V_{REF} must never be more negative than AGND.

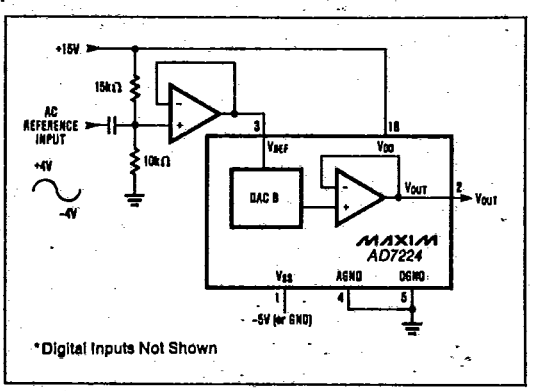

Figure 14. AC Reference Input Circuit

Generating V_{SS}

The performance of the AD7224 is specified for both dual and single supply (V_{SS} = 0V) operation. When the improved performance of dual supply operation is desired, but only a single supply is available, a -5V V_{SS} supply can be generated using an ICL7660 in one of the circuits of Figure 15.

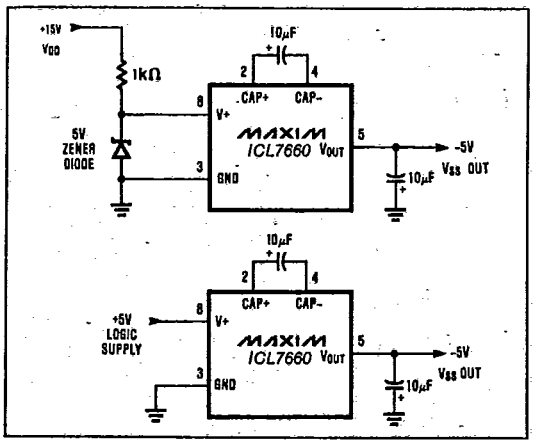

Figure 15. Generating -5V for V_{SS}

CMOS 8-Bit DAC with Output Amplifier

Microprocessor Interfacing

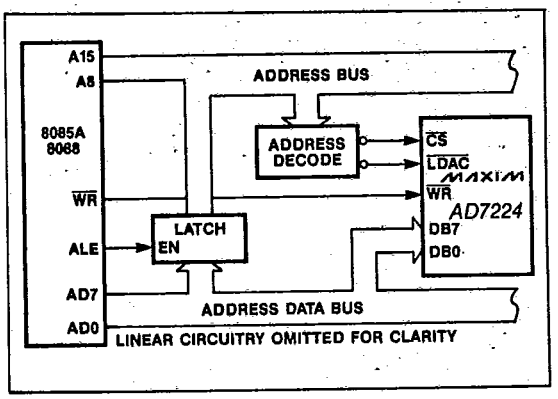

Figure 16. AD7224 to 8085A/8088 Interface

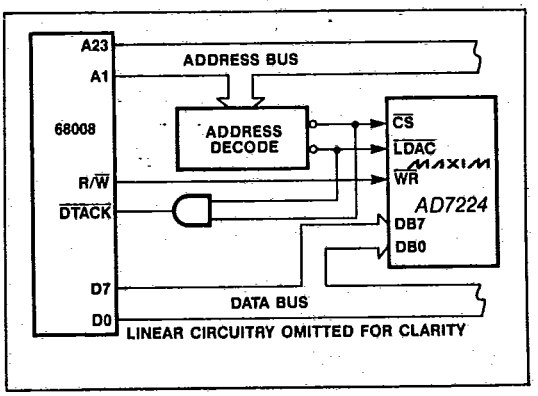

Figure 19. AD7224 to 68008 Interface

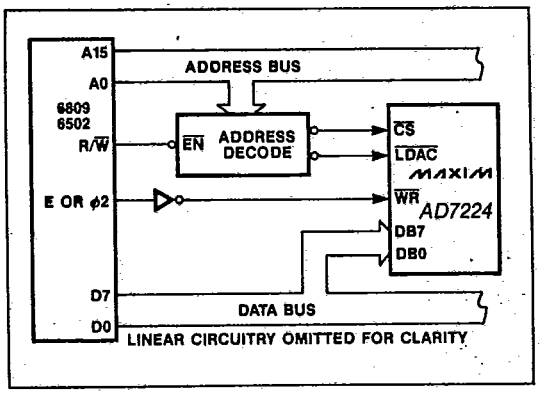

Figure 17. AD7224 to 6809/6502 Interface

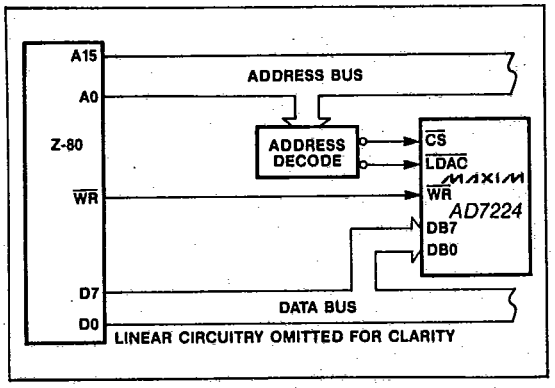

Figure 18. AD7224 to Z-80 Interface

Chip Topography