PEEL™ 20V8 -5/-7/-10/-15/-25
CMOS Programmable Electrically Erasable Logic

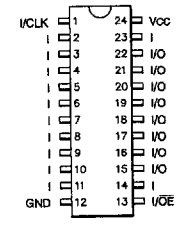
Features

- **Compatible with Popular 20V8 Devices**
  - 20V8 socket and function compatible
  - Programs with standard 20V8 JEDEC file
  - 24-pin DIP/SOIC, 28-pin PLCC packages
- **CMOS Electrically Erasable Technology**
  - Superior factory testing
  - Reprogrammable in plastic package
  - Reduces retrofit and development costs
- **Application Versatility**
  - Replaces random logic
  - Super-sets standard 24-pin PLDs (PALs)
- **Low Power and Quarter Power Versions**
  - Low Power: 75mA typical Icc
  - Quarter Power: 45mA typical Icc
- **Development/Programmer Support**
  - Third party software and programmers
  - ICT PLACE Development Software and PDS-3 programmer
  - Automatic programmer translation and JEDEC file translation software available for the most popular PAL devices

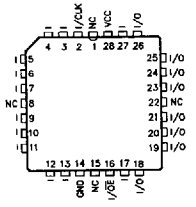
General Description

The PEEL20V8 is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL20V8 offers the performance, flexibility, ease-of-design and production practicality needed by logic designers today. The PEEL20V8 is available in 24-pin DIP, PLCC and SOIC packages (see Figure 1) with speeds ranging from 5ns to 25ns and power consumption as low as 45mA. EE-reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-reprogrammability also improves factory testability, thus ensuring the highest quality possible. The PEEL20V8 is socket and function compatible with other 20V8 devices. Its architecture allows it to replace many standard 24-pin PALs. See Figure 2. ICT's PEEL20V8 can be programmed with any existing 20V8 JEDEC file. Some programmers also allow the PEEL20V8 to be programmed directly from PAL 20L8, 20R4, 20R6 and 20R8 JEDEC files. Additional development and programming support for the PEEL20V8 is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

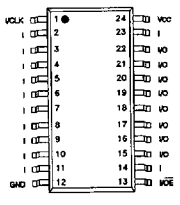
Pin Configuration (Figure 1)



DIP

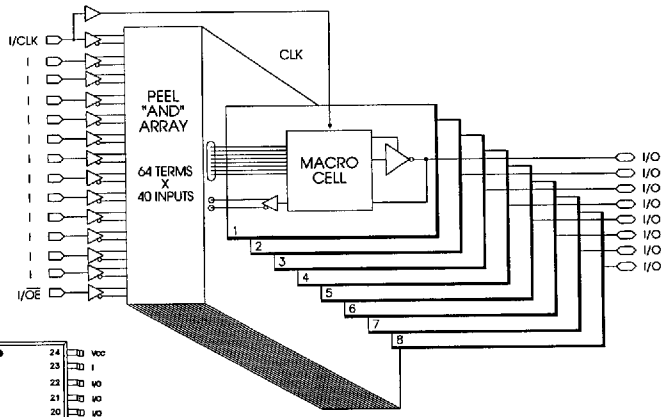


PLCC



SOIC

Block Diagram (Figure 2)



Functional Description

The PEEL20V8 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of macrocells further increase logic flexibility.

Architecture Overview

The PEEL20V8 features fourteen dedicated input pins and eight I/O pins, which allow a total of up to 20 inputs and 8 outputs for creating logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL20V8 can implement up to 8 sum-of-products logic expressions.

Associated with each of the eight OR functions is a macrocell which can be independently programmed to one of up to four different basic configurations: active-high or active-low registered logic output (with registered feedback) or active-high or active-low combinatorial logic output (with I/O pin feedback).

Three different device modes, Simple, Complex and Registered, support various user configurations. In Simple mode a macrocell can be configured for combinatorial function with the output buffer permanently enabled, or the output buffer can be disabled and the I/O pin used as a dedicated input. In Complex mode a macrocell is configured for combinatorial function with the output buffer enable controlled by a product term. In Registered mode, a macrocell can be configured for registered operation with the register clock and output buffer enable controlled directly from pins, or can be configured for combinatorial function with the output buffer enable controlled by a product term. In most cases the device mode is set automatically by the development software, based on the features specified in the design.

The three device modes support designs created explicitly for the PEEL20V8, as well as designs created originally for popular PAL devices such as the 20R4, 20R8 and 20L8. Table 1 shows the device mode used to emulate the various PALs. Design conversion into the 20V8 is accommodated by several programmers which can read the original PAL JEDEC file and automatically program the 20V8 to perform the same function.

AND/OR Logic Array

The programmable AND array of the PEEL20V8 is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

40 input lines:

24 input lines carry the true and complement of the signals applied to the 12 dedicated input pins

16 additional lines carry the true and complement of 8 macrocell feedback signals or inputs from I/O pins or the clock/OE pins

64 product terms:

56 product terms (arranged in 8 groups of 7) form sum-of-product functions for macrocell combinatorial or registered logic

8 product terms (arranged 1 per macrocell) add an additional product term for macrocell sum-of-products functions or I/O pin output enable control

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 32-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, that term will always be TRUE.

When programming the PEEL20V8, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program at least one pair of complementary inputs on unused product terms so that they will have no effect on the output function.)

Table 1. PEEL20V8/PAL Device Compatibility

PAL Architecture Compatibility	PEEL20V8 Device Mode
14H8	Simple
14L8	Simple
14P8	Simple
16H6	Simple
16L6	Simple
16P6	Simple
18H4	Simple
18L4	Simple
18P4	Simple
20H2	Simple
20L2	Simple
20P2	Simple
20H8	Complex
20L8	Complex
20P8	Complex
20R4	Registered
20R6	Registered
20R8	Registered
20RP4	Registered
20RP6	Registered
20RP8	Registered

Programmable Macrocell

The macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL20V8 to the precise requirements of their designs.

Macrocell Architecture

Each macrocell consists of an OR function, a D-type flip-flop, an output polarity selector, and a programmable feedback path. Four EEPROM architecture bits MS0, MS1, OP and RC control the configuration of each macrocell. Bits MS0 and MS1 are global, and select between Simple, Complex, and Registered mode for the whole device. Bits OP and RC are local for each macrocell; bit OP controls the output polarity and bit RC selects between registered and combinatorial operation and also specifies the feedback path. Table 2 shows the architecture bit settings for each possible configuration.

Equivalent circuits for the possible macrocell configurations are illustrated in Figures 3, 4 and 5. When creating a PEEL device design, the desired macrocell configuration generally is specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Simple Mode

In Simple mode, all eight product terms feed the OR array which can generate a purely combinatorial function for the output pin. The programmable output polarity selector allows active-high or active-low logic, eliminating the need for external inverters. For output functions, the buffer can be permanently enabled. Feedback into the array is available on all macrocell I/O pins, except for DIP/SOIC pins 18 and 19 (PLCC pins 21 and 23). Figure 6 shows the logic array of the PEEL20V8 configured in Simple mode.

Simple mode also provides the option of configuring an I/O pin as a dedicated input. In this case the output buffer is permanently disabled, and the I/O pin feedback is used to bring the input signal from the pin into the logic array. This option is available for all I/O pins except pins 18 and 19 (PLCC pins 21 and 23).

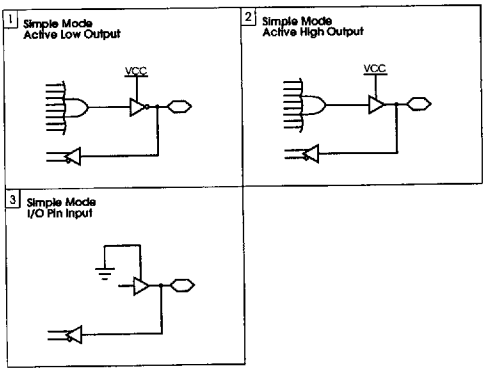


Figure 3. Macrocell Configurations for the Simple Mode of the PEEL20V8

Table 2. PEEL20V8 Device Mode/Macrocell Configuration Bits

Config. #	Mode	Architecture Bits				Function	Polarity	Feedback
		MS0	MS1	OP	RC			
1	Simple	1	0	0	0	Combinatorial	Active Low	I/O Pin
2	Simple	1	0	1	0	Combinatorial	Active High	I/O Pin
3	Simple	1	0	X	1	None	None	I/O Pin
1	Complex	1	1	0	1	Combinatorial	Active Low	I/O Pin
2	Complex	1	1	1	1	Combinatorial	Active High	I/O Pin
1	Registered	0	1	0	0	Registered	Active Low	Registered
2	Registered	0	1	1	0	Registered	Active High	Registered
3	Registered	0	1	0	1	Combinatorial	Active Low	I/O Pin
4	Registered	0	1	1	1	Combinatorial	Active High	I/O Pin

Complex Mode

In Complex mode, seven product terms feed the OR array which can generate a purely combinatorial function for the output pin. The programmable output polarity selector provides active-high or active-low logic, eliminating the need for external inverters. The output buffer is controlled by the eighth product term, allowing the macrocell to be configured for input, output, or bidirectional functions. Feedback into the array for input or bidirectional functions is available on all pins except DIP/SOIC pins 15 and 22 (PLCC pins 18 and 26). Figure 7 shows the logic array of the PEEL20V8 configured in Complex mode.

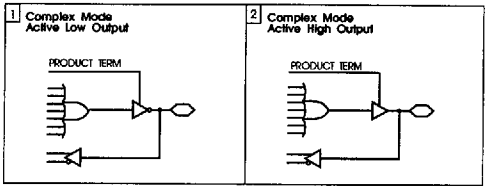


Figure 4. Macrocell Configurations for the Complex Mode of the PEEL20V8

Registered Mode

Registered mode provides eight product terms to the OR array for registered functions. The programmable output polarity selector provides active-high or active-low logic, eliminating the need for external inverters. (Note, however, that PEEL20V8 registers power-up reset and so before the first clock arrives the output at the pin will be low if the user has selected active-high logic and high if the user has selected active-low logic.) For registered functions, the output buffer enable is controlled directly from the /OE control pin. Feedback into the array comes from the macrocell register. In Registered mode, DIP/SOIC input pins 1 and 13 (PLCC pins 2 and 16) are permanently allocated as CLK and /OE, respectively. Figure 8 shows the logic array of the PEEL20V8 configured in Registered mode.

Registered mode also provides the option of configuring a macrocell for combinatorial operation, with seven product terms feeding the OR function.

Again the programmable output polarity selector provides active-high or active-low logic. The output buffer enable is controlled by the eighth product term, allowing the macrocell to be configured for input, output, or bidirectional functions. Feedback into the array for input or bidirectional functions is available on all I/O pins.

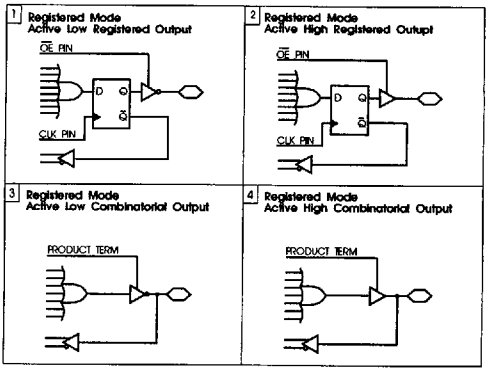


Figure 5. Macrocell Configurations for the Registered Mode of the PEEL20V8

Input and I/O Pin Pull-ups

The input and I/O pins on this device feature pull-up circuitry. The pull-ups cause input and I/O pins to be pulled high through nominally 100k ohms.

Design Security

The PEEL20V8 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit has been set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 64-bit code to be programmed into the PEEL20V8. The code cannot be read back after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

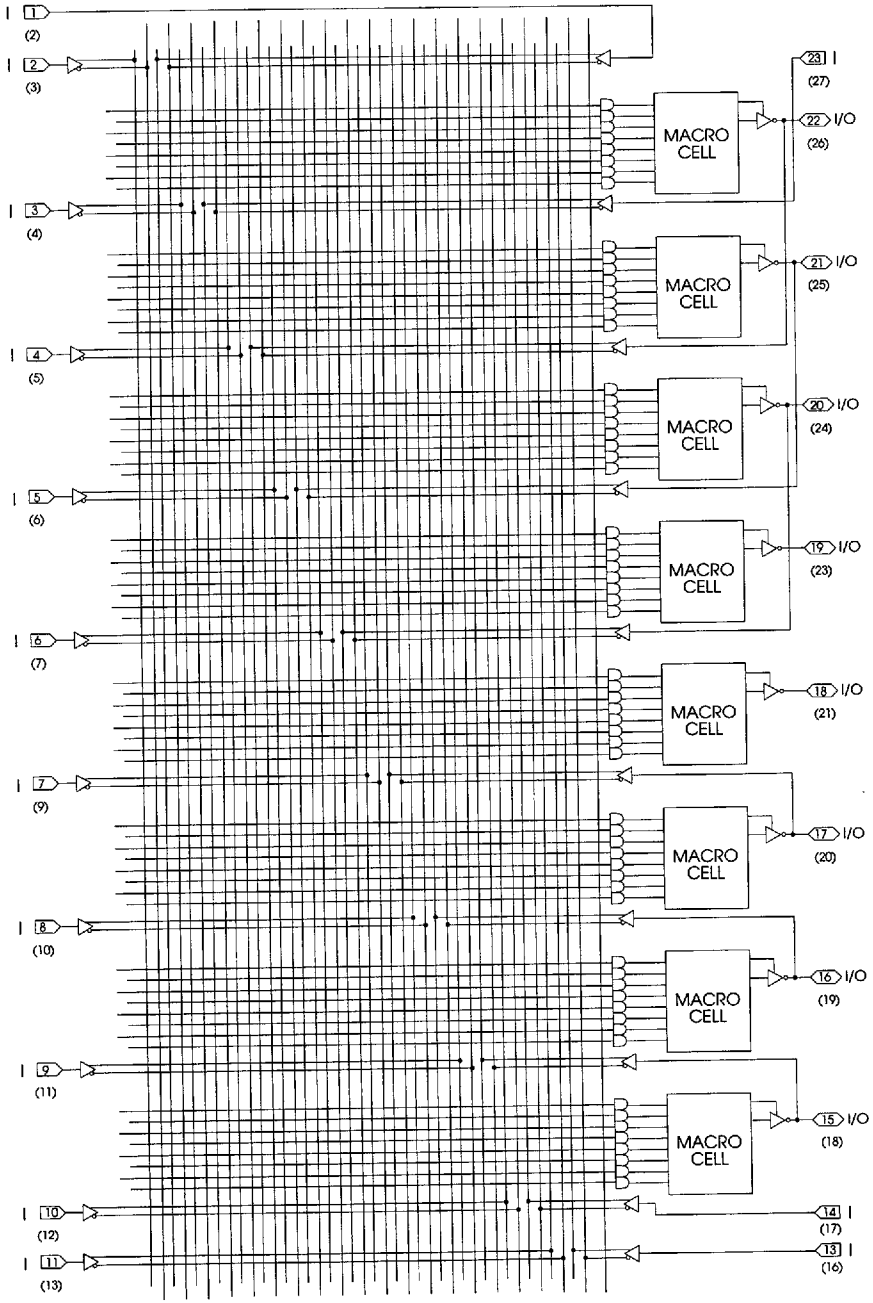


Figure 6. PEEL20V8 Logic Array - Simple Mode
(Pin numbers are for DIP and SOIC packages, PLCC pin numbers shown in parentheses.)

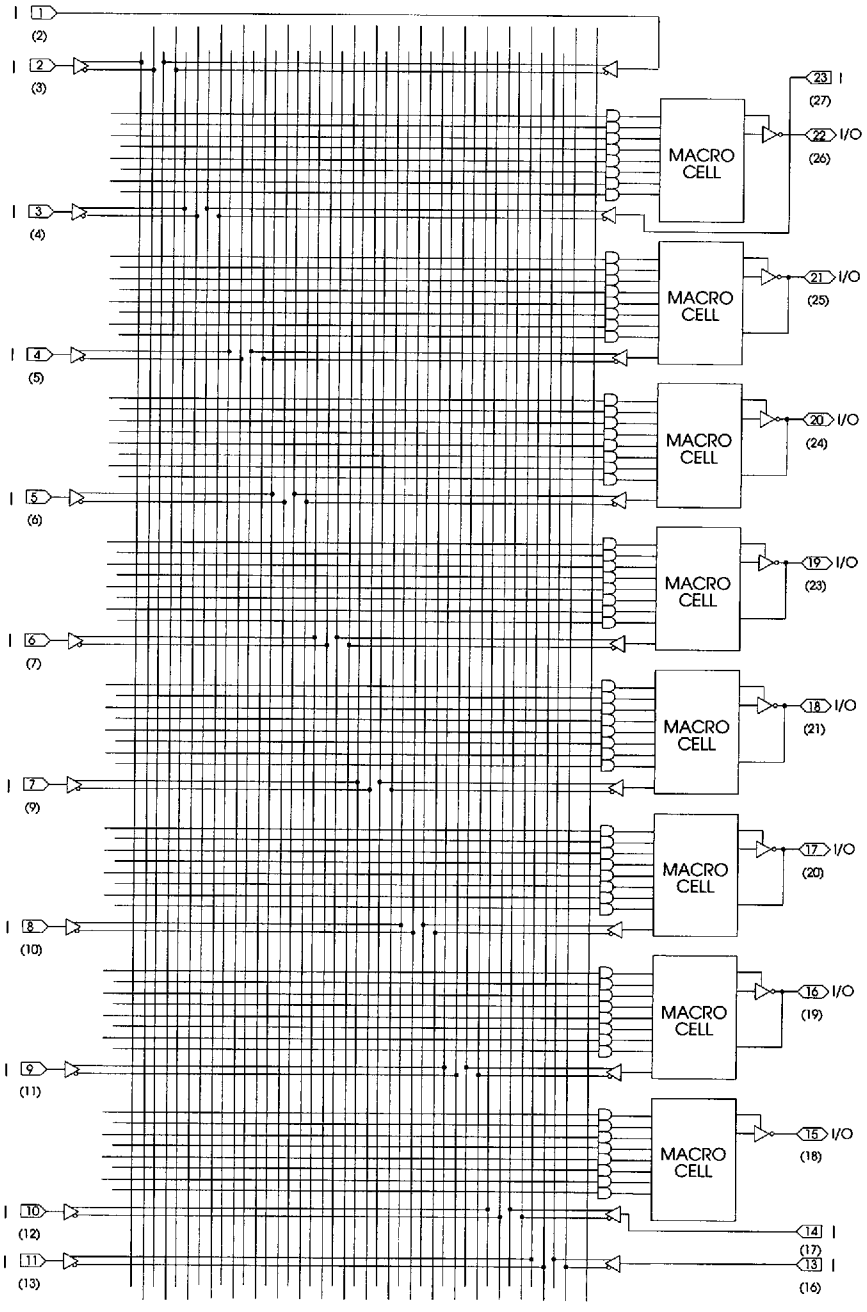


Figure 7. PEEL20V8 Logic Array - Complex Mode
(Pin numbers are for DIP and SOIC packages, PLCC pin numbers shown in parentheses.)

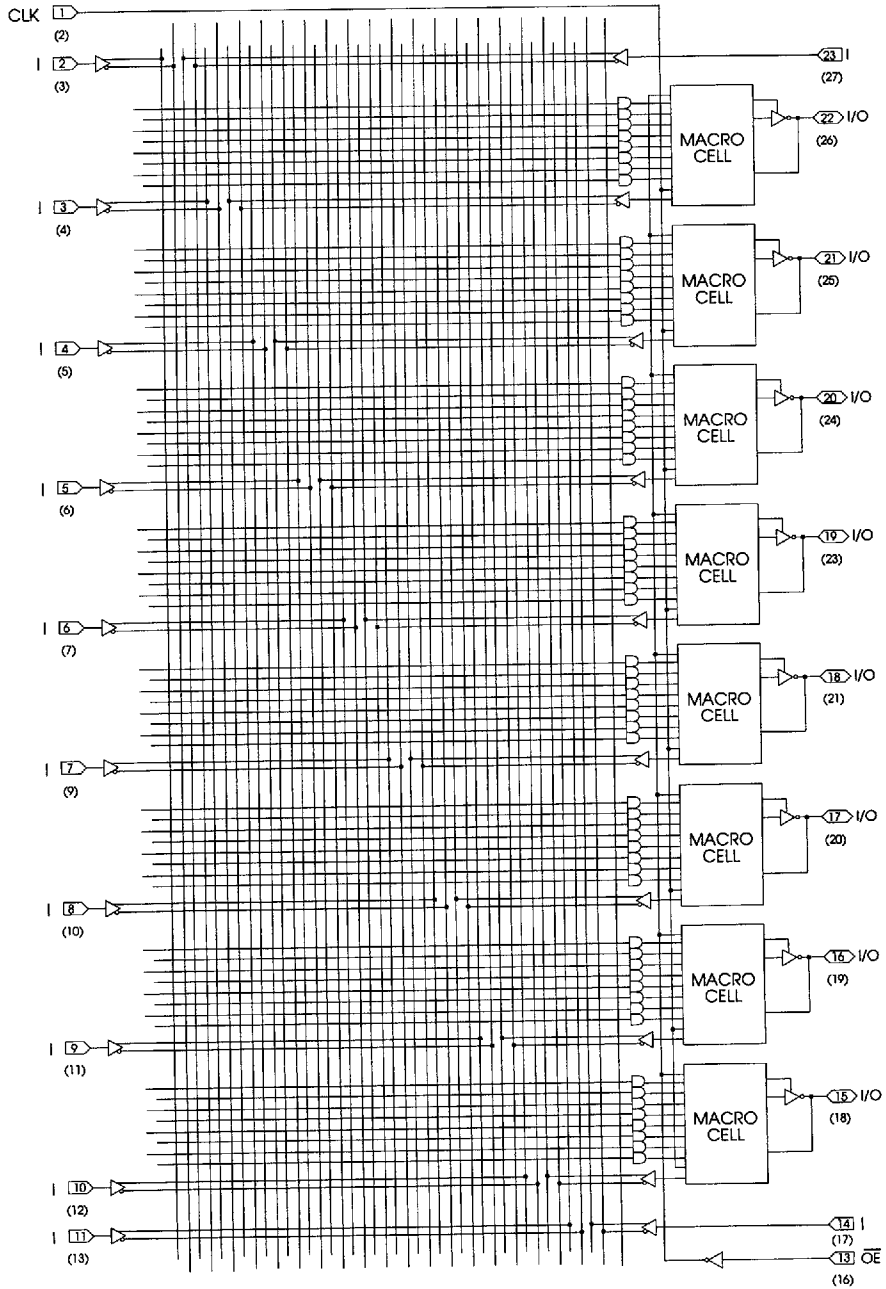


Figure 8. PEEL20V8 Logic Array - Registered Mode
(Pin numbers are for DIP and SOIC packages, PLCC pin numbers shown in parentheses.)

Absolute Maximum Ratings

This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin[2]	Relative to Ground[1]	-0.5 to VCC + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	±25	mA
T_{ST}	Storage Temperature		-65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	+70	°C
T_R	Clock Rise Time	See Note 3		20	ns
T_F	Clock Fall Time	See Note 3		20	ns
T_{RVCC}	V_{CC} Rise Time	See Note 3		250	ms

D.C. Electrical Characteristics Over the operating range

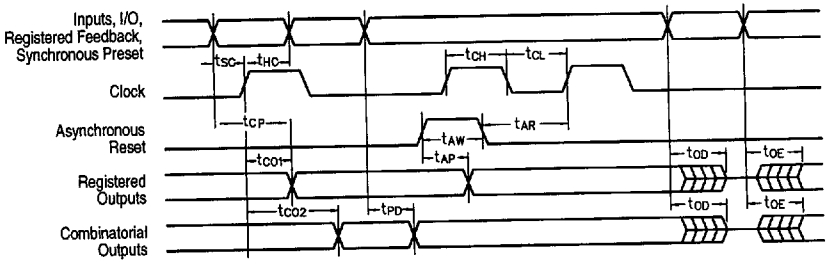
Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -4.0mA		2.4		V
V_{OL}	Output LOW Level	V_{CC} = Min, I_{OL} = 16mA			0.5	V
V_{IH}	Input HIGH Level			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level			-0.3	0.8	V
I_{IL}	Input and I/O Leakage Current LOW	V_{CC} = Max, V_{IN} = GND, I/O = High Z			-100	µA
I_{IH}	Input and I/O Leakage Current HIGH	V_{CC} = Max, V_{IN} = V_{CC}, I/O = High Z			10	µA
I_{SC}	Output Short Circuit Current	V_{CC} = 5V, V_O = 0.5V[9], T_A = 25°C		-30	-150	mA
I_{CC}[10]	V_{CC} Current	V_{IN} = 0V or 3V f = 25MHz All outputs disabled[4]	L -5	75 (typ)	115	mA
			L -7	75 (typ)	115	
			L -10	75 (typ)	115	
			Q/L -15	45/75 (Typ)	55/90	
			Q/L -25	45/75 (Typ)	55/90	
C_{IN}[7]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz			6	pF
C_{OUT}[7]	Output Capacitance				12	pF

A.C. Electrical Characteristics

Over the Operating Range [8, 11]

Symbol	Parameter	L-5		L-7		L-10		Q/L-15		Q/L-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input[5] to non-registered output	1	5	3	7.5	3	10	3	15	3	25	ns
t_{OE}	Input[5] to output enable[6]	1	5	3	7.5		10		15		20	ns
t_{OD}	Input[5] to output disable[6]	1	5	3	7.5		10		15		20	ns
t_{CO1}	Clock to output	1	4		7	2	7	2	10	2	12	ns
t_{CO2}	Clock to comb. output delay via internal registered feedback		7.5		10		12		25		35	ns
t_{CF}	Clock to Feedback		3		3.5		4		8		10	ns
t_{SC}	Input[5] or feedback setup to clock	3		5		5		12		15		ns
t_{HC}	Input[5] hold after clock	0		0		0		0		0		ns
t_{CL}, t_{CH}	Clock low time, clock high time[8]	3		3.5		5		8		12		ns
t_{CP}	Min clock period Ext (t_{SC} + t_{CO1})	7		12		12		22		27		ns
f_{MAX1}	Internal Feedback ($1/t_{SC}+t_{CF}$)[12]	166.6		117.6		111.1		50		40		MHz
f_{MAX2}	External Feedback ($1/t_{CP}$)[12]	142.8		83.3		83.3		45.5		37		MHz
f_{MAX3}	No Feedback ($1/t_{CL}+t_{CH}$)[12]	166.6		142.8		100		62.5		41.6		MHz
t_{AW}	Asynchronous Reset pulse width	5		7.5		10		15		25		ns
t_{AP}	Input[5] to Asynchronous Reset		5		7.5		10		15		25	ns
t_{AR}	Asynchronous Reset recovery time		5		7.5		10		15		25	ns
t_{RESET}	Power-on reset time for registers in clear state						5		5		5	µs

Switching Waveforms



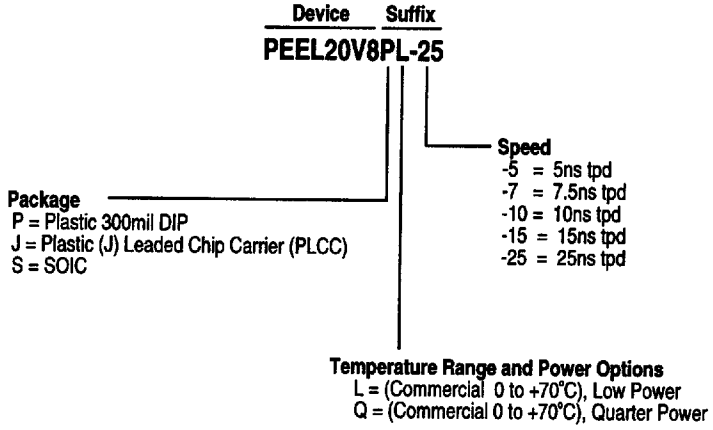
Notes

1. Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
2. V_I and V_O are not specified for program/verify operation.
3. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
4. I/O pins are 0V or 3V.
5. "Input" refers to an Input pin signal.
6. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to V_{OH} - 0.1V or V_{OL} + 0.1V; $V_{REF} = V_L$ see test loads in Section 6 of this Data Book.
7. Capacitances are tested on a sample basis.
8. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
9. Test one output at a time for a duration of less than 1 sec.
10. ICC for a typical application: This parameter is tested with the device programmed as an 8-bit Counter.
11. PEEL Device test loads are specified in Section 6 of this Data Book.
12. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

Ordering Information

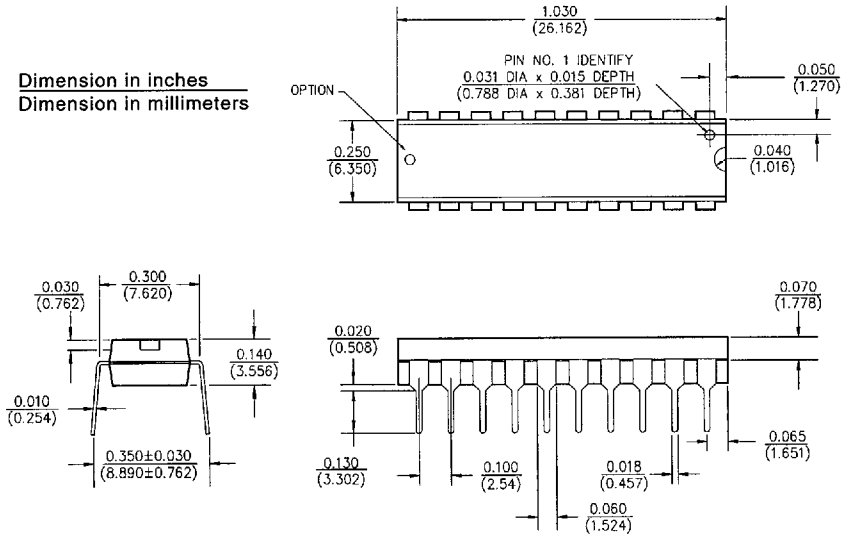
PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PEEL20V8JL-5*	5ns	C	J28
PEEL20V8PL-7*	7.5ns	C	P24
PEEL20V8JL-7*	7.5ns	C	J28
PEEL20V8SL-7*	7.5ns	C	S24
PEEL20V8PL-10*	10ns	C	P24
PEEL20V8JL-10*	10ns	C	J28
PEEL20V8SL-10*	10ns	C	S24
PEEL20V8PL-15	15ns	C	P24
PEEL20V8PQ-15		C	
PEEL20V8JL-15	15ns	C	J28
PEEL20V8JQ-15		C	
PEEL20V8SL-15	15ns	C	S24
PEEL20V8SQ-15		C	
PEEL20V8PL-25	25ns	C	P24
PEEL20V8PQ-25		C	
PEEL20V8JL-25	25ns	C	J28
PEEL20V8JQ-25		C	
PEEL20V8SL-25	25ns	C	S24
PEEL20V8SQ-25		C	

* Contact ICT for availability of the -5, -7 and -10 speed grades.

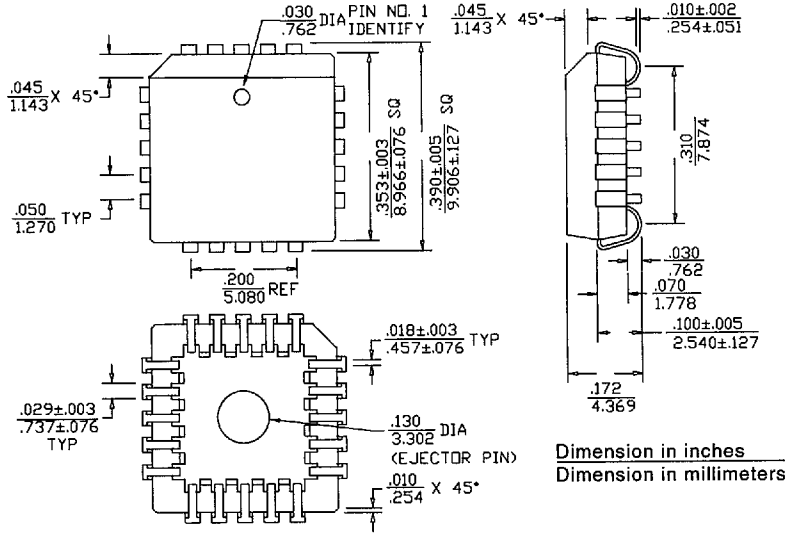


Package Diagrams (Drawings are not necessarily to scale.)

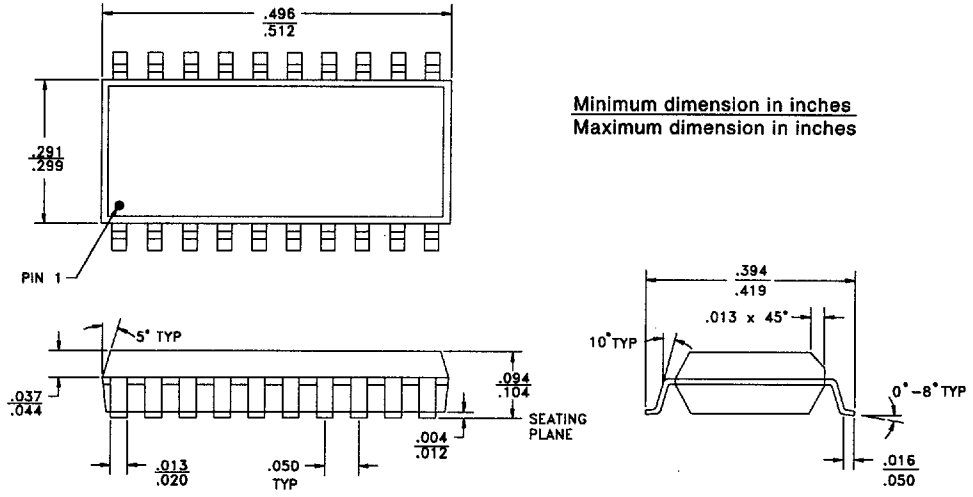
Dimension in inches
Dimension in millimeters



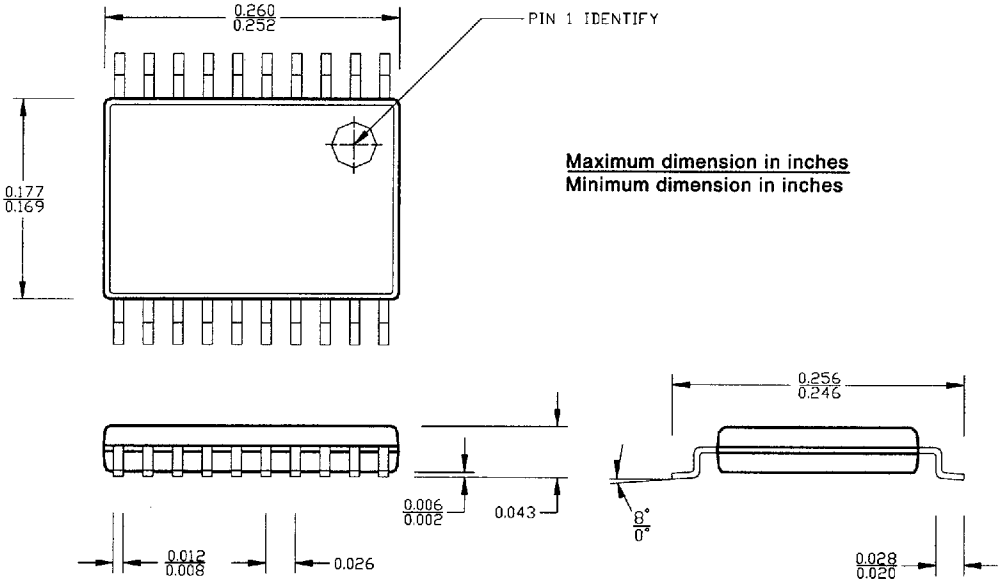
20-Pin Plastic DIP (P20)



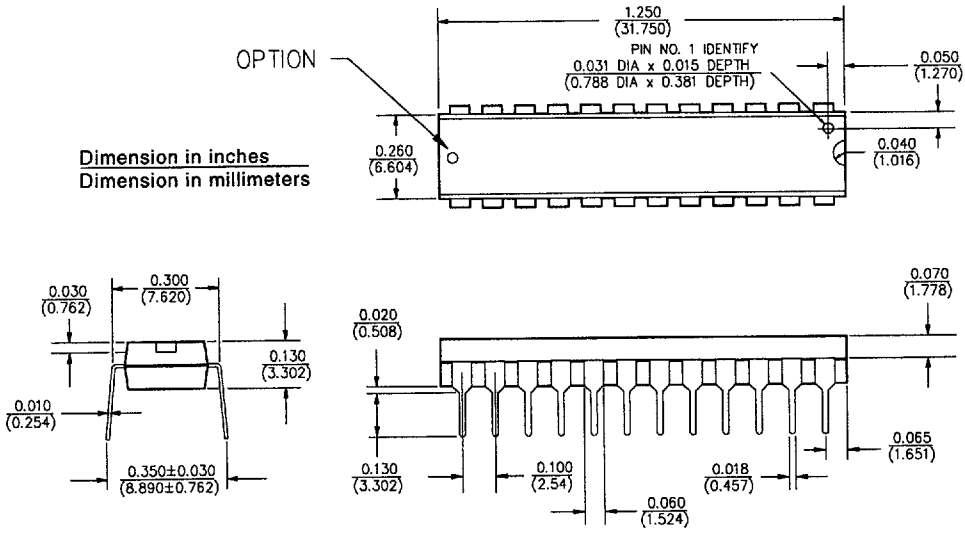
20-Pin PLCC (J20)



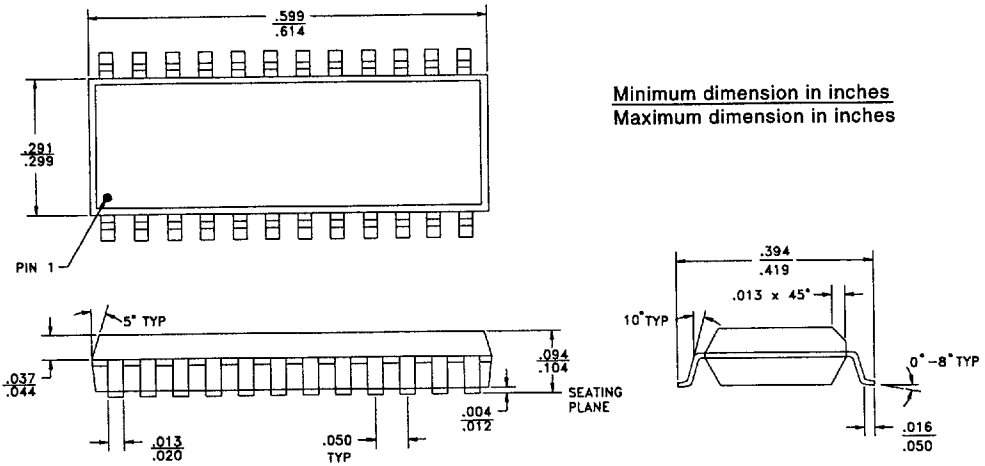
20-Pin SOIC (S20)



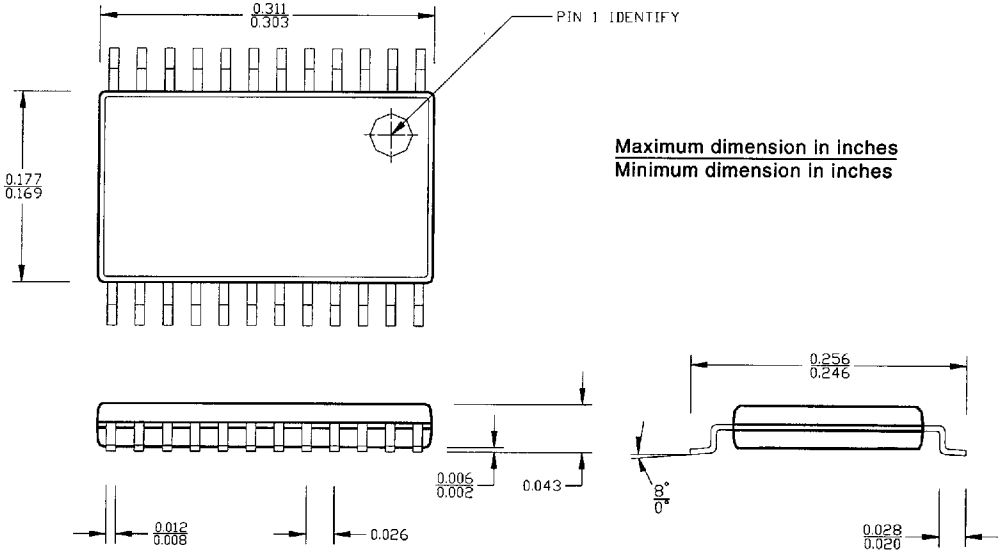
20-Pin TSSOP (T20)



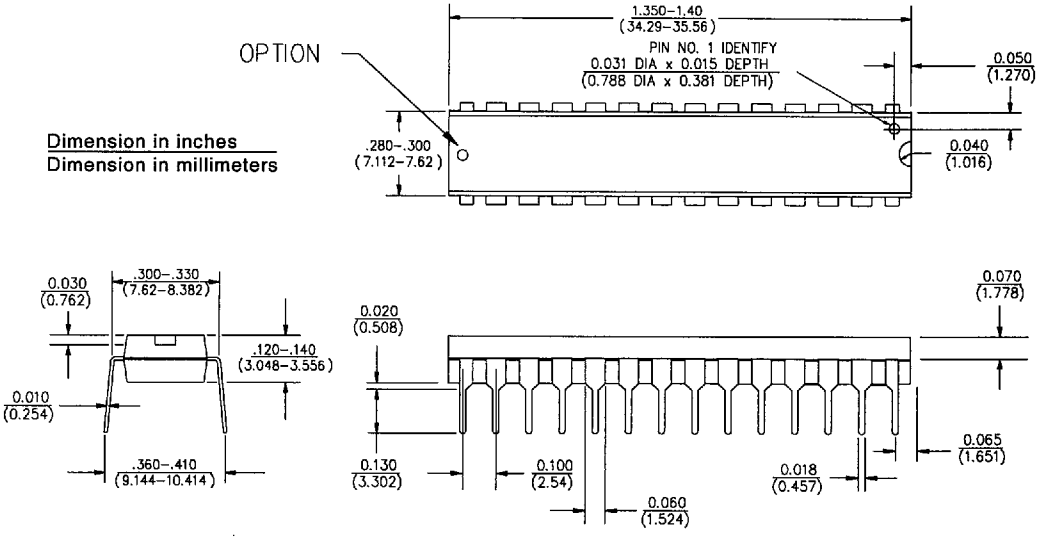
24-Pin Plastic DIP (P24)



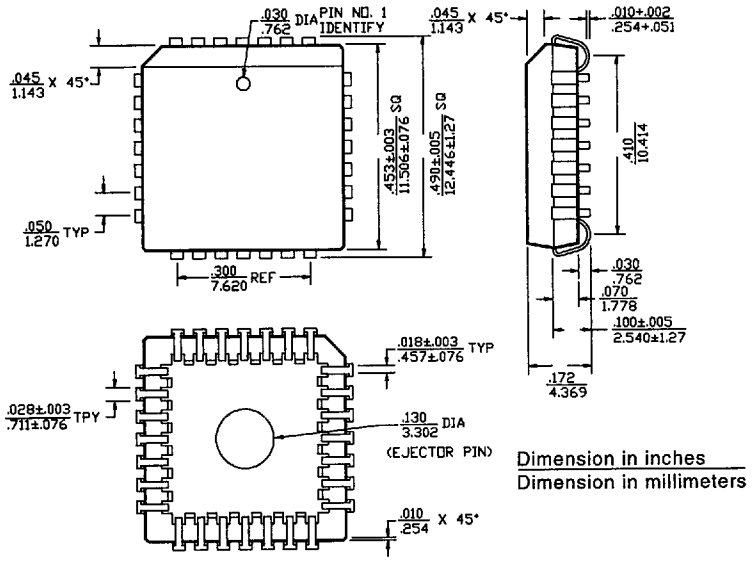
24-Pin SOIC (S24)



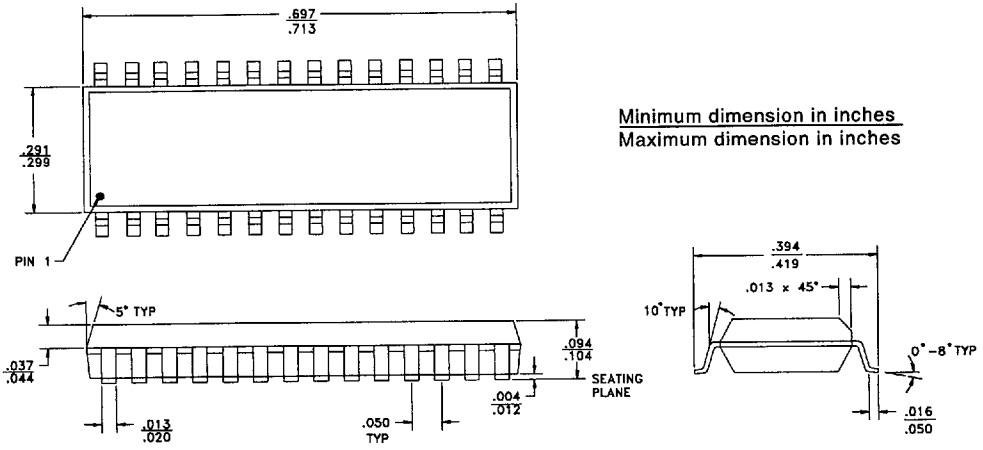
24-Pin TSSOP (T24)



28-Pin Plastic Dip (P28)

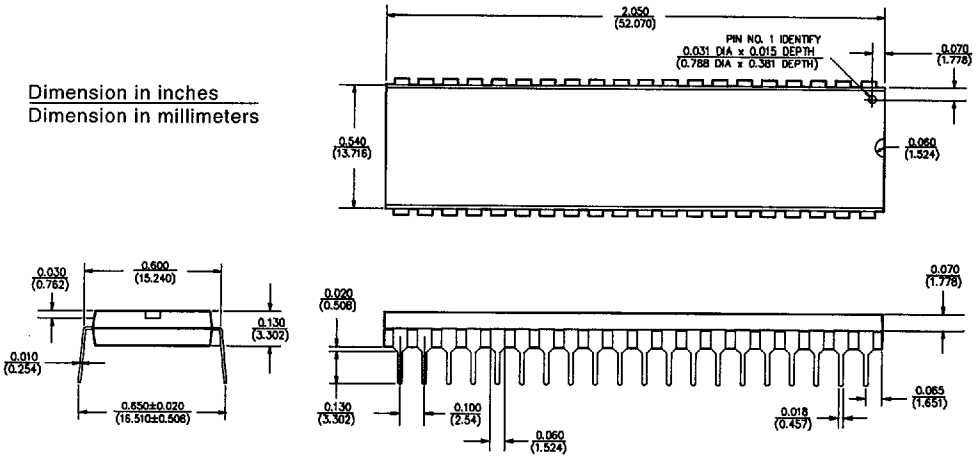


28-Pin PLCC (J28)

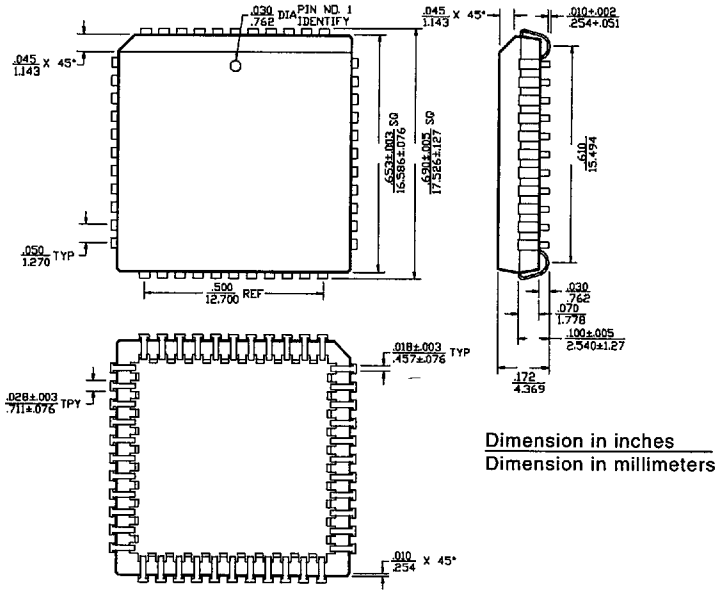


28-Pin SOIC (S28)

Dimension in inches
Dimension in millimeters



40-Pin Plastic DIP (T40)



Dimension in inches
Dimension in millimeters

44-Pin PLCC (J44)