

### 1.1 Scope.

This specification covers the detail requirements for two monolithic CMOS dual 12-bit DACPORTs™, each consisting of two 12-bit DACs, output amplifiers and reference. The AD7237A has an (8+4) micro-processor loading structure, while the AD7247A has a parallel loading structure.

### 1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

| Device | Part Number                    |
|--------|--------------------------------|
| -1     | AD7237ATQ/883B, AD7247ATQ/883B |

### 1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

#### Package Description

Q-24 24-Pin Cerdip, 0.3" Width

(For volume applications, the AD7237A and AD7247A are available in the LCC package. Contact your local Analog Devices Sales Office.)

### 1.3 Absolute Maximum Ratings. (T<sub>A</sub> = +25°C unless otherwise noted)

|                                                                               |                                                  |
|-------------------------------------------------------------------------------|--------------------------------------------------|
| V <sub>DD</sub> to GND (AD7247A)                                              | +0.3 V to +17 V                                  |
| V <sub>DD</sub> to AGND, DGND (AD7237A)                                       | -0.3 V to +17 V                                  |
| V <sub>DD</sub> to V <sub>SS</sub>                                            | -0.3 V to +34 V                                  |
| AGND to DGND (AD7237A)                                                        | +0.3 V, V <sub>DD</sub> +0.3 V                   |
| V <sub>OUTA</sub> , <sup>1</sup> V <sub>OUTB</sub> <sup>1</sup> to AGND (GND) | V <sub>SS</sub> -0.3 V to V <sub>DD</sub> +0.3 V |
| REFOUT <sup>1</sup> to AGND (GND)                                             | 0 V to V <sub>DD</sub>                           |
| REFIN to AGND (GND)                                                           | -0.3 V to V <sub>DD</sub> +0.3 V                 |
| Digital Inputs to DGND (GND)                                                  | -0.3 V to V <sub>DD</sub> +0.3 V                 |
| Operating Temperature Range                                                   | -55°C to +125°C                                  |
| Storage Temperature Range                                                     | -65°C to +150°C                                  |
| Lead Temperature (Soldering, 10 sec)                                          | +300°C                                           |
| Power Dissipation (Any Package) to +75°C                                      | 1000 mW                                          |
| Derates above +75°C by                                                        | 10 mW/°C                                         |

#### NOTE

<sup>1</sup>The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.

### 1.5 Thermal Characteristics.

Thermal Resistance  $\theta_{JC}$  = 35°C/W  
 $\theta_{JA}$  = 120°C/W

DACPORT is a trademark of Analog Devices, Inc.

# AD7237A/AD7247A—SPECIFICATIONS

Table 1.

| Test                                              | Symbol                      | Device | Limits      |      | Sub Groups | Test Condition <sup>1</sup>                                                            | Unit |
|---------------------------------------------------|-----------------------------|--------|-------------|------|------------|----------------------------------------------------------------------------------------|------|
|                                                   |                             |        | Min         | Max  |            |                                                                                        |      |
| Resolution                                        | RES                         | –1     |             | 12   | 1, 2, 3    |                                                                                        | Bits |
| Relative Accuracy                                 | RA                          | –1     | –0.5        | +0.5 | 1, 2, 3    |                                                                                        | LSB  |
| Differential Nonlinearity                         | DNL                         | –1     | –0.9        | +0.9 | 1, 2, 3    | Guaranteed Monotonic                                                                   | LSB  |
| Unipolar Offset Error                             | OFS                         | –1     | –3          | +3   | 1, 2, 3    | V <sub>SS</sub> = 0 V or –15 V.<br>DAC Latch Contents All Zeroes                       | LSB  |
| Bipolar Zero Error                                | Z <sub>E</sub>              | –1     | –6          | +6   | 1, 2, 3    | V <sub>SS</sub> = –15 V. DAC Latch<br>Contents 1000 0000 0000                          | LSB  |
| Full-Scale Error <sup>2</sup>                     | A <sub>E</sub>              | –1     | –6          | +6   | 1, 2, 3    |                                                                                        | LSB  |
| Reference Output                                  | REF OUT                     | –1     | 4.95        | 5.05 | 1, 2, 3    |                                                                                        | V    |
| Reference Load Change                             | ΔREF                        | –1     |             | –1   | 1, 2, 3    | ΔREFOUT vs. Δ I<br>Reference Load Current<br>Change (0–100 mA)                         | mV   |
| Reference Input Range                             | REFIN                       | –1     | 4.75        | 5.25 | 1, 2, 3    |                                                                                        | V    |
| Input Current                                     | I <sub>IN</sub>             | –1     | –5          | +5   | 13, 14, 15 |                                                                                        | μA   |
| Digital Input High Voltage                        | V <sub>INH</sub>            | –1     | 2.4         |      | 1, 2, 3    |                                                                                        | V    |
| Digital Input Low Voltage                         | V <sub>INL</sub>            | –1     |             | 0.8  | 1, 2, 3    |                                                                                        | V    |
| Digital Input Current <sup>3</sup>                | I <sub>IN</sub>             | –1     | –10         | +10  | 1, 2, 3    | Data Inputs; V <sub>IN</sub> = 0 V to V <sub>DD</sub>                                  | μA   |
|                                                   | I <sub>INH</sub>            |        | –10         | +10  |            | Control Inputs; V <sub>IN</sub> = V <sub>DD</sub>                                      |      |
|                                                   | I <sub>INL</sub>            |        |             | –150 |            | Control Inputs; V <sub>IN</sub> = 0 V                                                  |      |
| Input Capacitance                                 | C <sub>IN</sub>             | –1     |             | 16   | 13, 14, 15 |                                                                                        | pF   |
| Output Range Resistors                            |                             | –1     | 15          | 30   | 1, 2, 3    |                                                                                        | kΩ   |
| Output Voltage Ranges                             |                             | –1     | +5          | +10  | 1, 2, 3    | V <sub>SS</sub> = 0 V; Pin Strappable                                                  | V    |
| Output Voltage Ranges                             |                             | –1     | +5, +10, ±5 |      | 1, 2, 3    | V <sub>SS</sub> = –12 V to –15 V; Pin Strappable                                       | V    |
| Voltage Output Settling Time<br>Full-Scale Change | t <sub>SL</sub>             | –1     |             | 12   | 13, 14, 15 | V <sub>DD</sub> = +15 V, V <sub>SS</sub> = 0 or –12 V to –15 V<br>Settling to ±1/2 LSB | μs   |
| Power Supply Current                              | I <sub>DD</sub>             | –1     |             | 15   | 1, 2, 3    | Outputs Unloaded                                                                       | mA   |
|                                                   | I <sub>SS</sub>             | –1     |             | 5    | 1, 2, 3    | Outputs Unloaded (Dual Supplies)                                                       | mA   |
| CS to WR Setup Time                               | t <sub>1</sub>              | –1     | 0           |      | 9, 10, 11  | See Note 4                                                                             | ns   |
| CS to WR Hold Time                                | t <sub>2</sub>              | –1     | 0           |      | 9, 10, 11  |                                                                                        | ns   |
| WR Pulse Width                                    | t <sub>3</sub>              | –1     | 100         |      | 9, 10, 11  |                                                                                        | ns   |
| Data Valid to Write Setup Time                    | t <sub>4</sub>              | –1     | 80          |      | 9, 10, 11  |                                                                                        | ns   |
| Data Valid to Write Hold Time                     | t <sub>5</sub>              | –1     | 10          |      | 9, 10, 11  |                                                                                        | ns   |
| Address to Write Setup Time                       | t <sub>6</sub> <sup>5</sup> | –1     | 0           |      | 9, 10, 11  |                                                                                        | ns   |
| Address to Write Hold Time                        | t <sub>7</sub> <sup>5</sup> | –1     | 0           |      | 9, 10, 11  |                                                                                        | ns   |
| LDAC Pulse Width                                  | t <sub>8</sub> <sup>5</sup> | –1     | 100         |      | 9, 10, 11  |                                                                                        | ns   |

## NOTES

<sup>1</sup>V<sub>DD</sub> = 12 V to 15 V, V<sub>SS</sub> = 0 V or –12 V to –15 V; AGND = DGND = 0 V (AD7237A), GND = 0 V (AD7247A); R<sub>L</sub> = 2 kΩ, C<sub>L</sub> = 100 pF. Subgroups 10, 11, 13, 14, 15 are characterized at initial design are after any design changes and are not production tested.

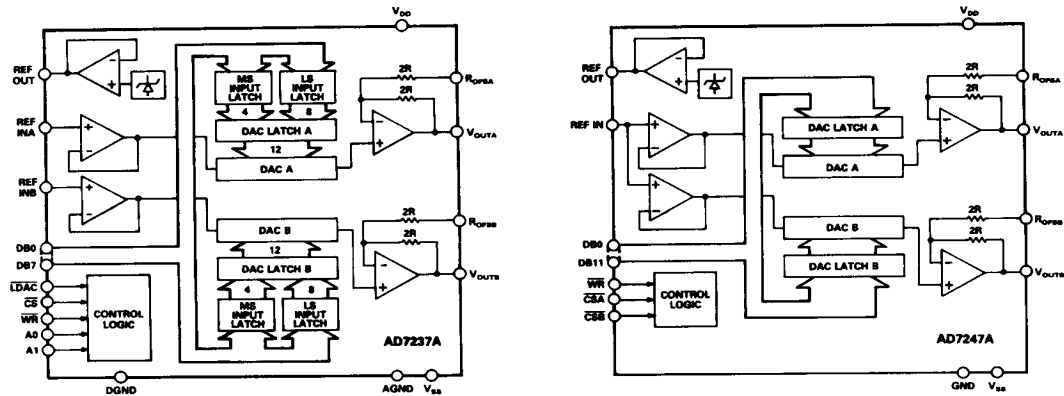
<sup>2</sup>Measured with respect to REFIN and includes unipolar/bipolar offset error.

<sup>3</sup>Control inputs are A0, A1, CS, WR and LDAC for the AD7237A and CSA, CSB and WR for the AD7247A.

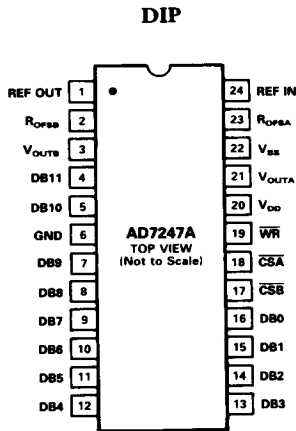
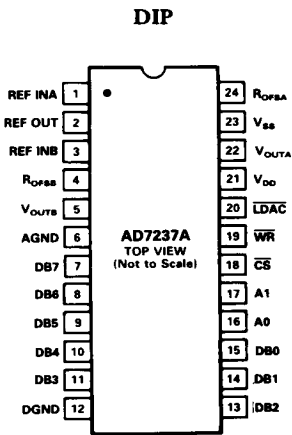
<sup>4</sup>All input signals are specified with t<sub>R</sub> = t<sub>F</sub> = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

<sup>5</sup>Applies to AD7237A only.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments



# AD7237A/AD7247A

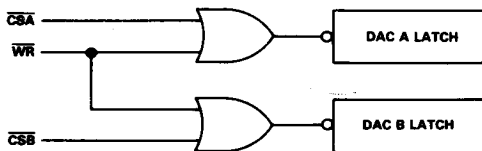


Figure 1. Input Control Logic AD7247A

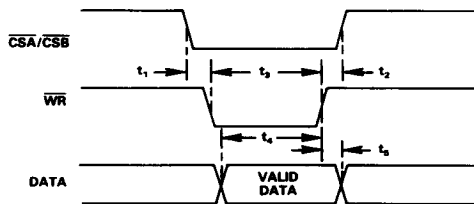


Figure 2. Timing Diagram AD7247A

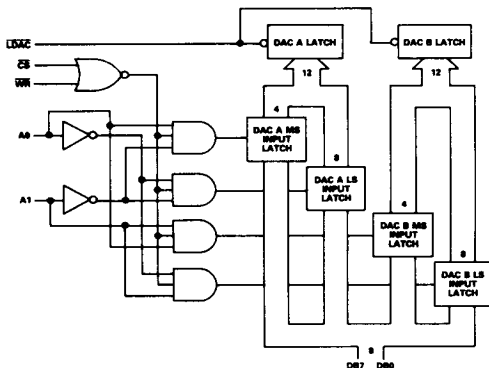


Figure 3. Input Control Logic AD7237A

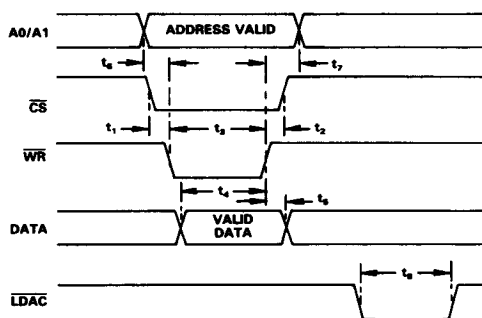


Figure 4. Timing Diagram AD7237A

Table 2. AD7247A Truth Table

| CSA | CSB | WR | Function                     |
|-----|-----|----|------------------------------|
| X   | X   | 1  | No Data Transfer             |
| 1   | 1   | X  | No Data Transfer             |
| 0   | 1   | 0  | DACA Latch Transparent       |
| 1   | 0   | 0  | DACB Latch Transparent       |
| 0   | 0   | 0  | Both DAC Latches Transparent |

X=Don't Care

Table 3. AD7237A Truth Table

| CS | WR | A1 | A0 | LDAC | Function                                                                           |
|----|----|----|----|------|------------------------------------------------------------------------------------|
| 1  | X  | X  | X  | 1    | No Data Transfer                                                                   |
| X  | 1  | X  | X  | 1    | No Data Transfer                                                                   |
| 0  | 0  | 0  | 0  | 1    | DAC A LS Input Latch Transparent                                                   |
| 0  | 0  | 0  | 1  | 1    | DAC A MS Input Latch Transparent                                                   |
| 0  | 0  | 1  | 0  | 1    | DAC B LS Input Latch Transparent                                                   |
| 0  | 0  | 1  | 1  | 1    | DAC B MS Input Latch Transparent                                                   |
| 1  | 1  | X  | X  | 0    | DACA and DACB DAC Latches Updated Simultaneously from the Respective Input Latches |

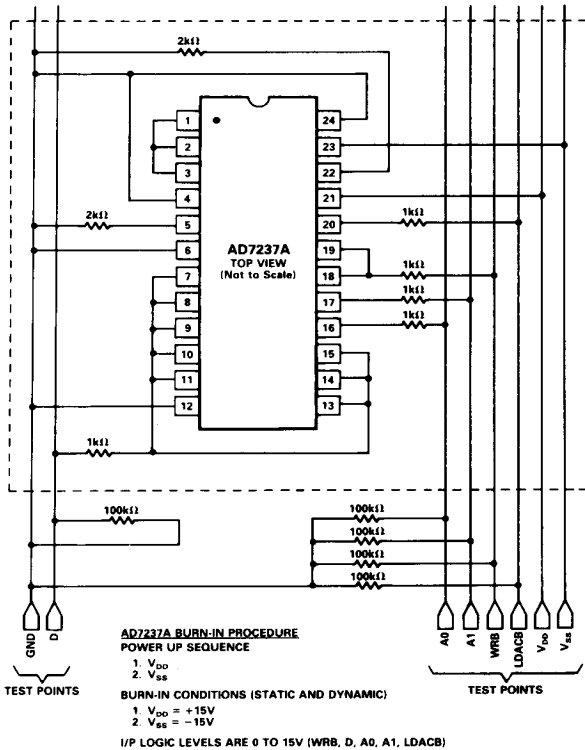
X = Don't Care.

## 3.2.4 Microcircuit Technology Group.

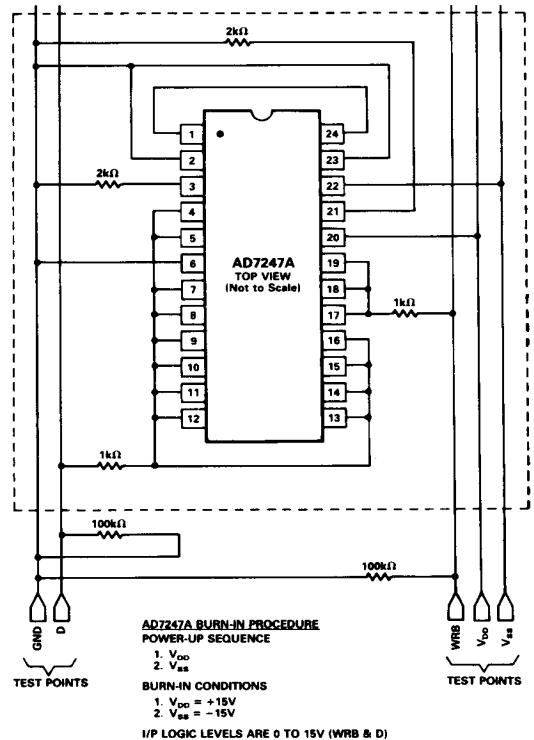
This microcircuit is covered by technology group (80).

## 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7237A Burn-In Diagram



AD7247A Burn-In Diagram