PEEL™22V10 -15/-25
CMOS Programmable Electrically Erasable Logic

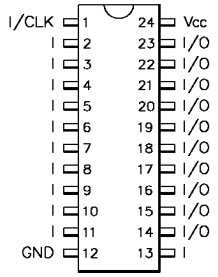
Features

- **High Speed/Low Power**
  - Speeds ranging from 15nS to 25nS
  - Power as low as 67mA at 25MHz
- **Electrically Erasable Technology**
  - Superior factory testing
  - Reprogrammable in plastic package
  - Reduces retrofit and development costs
- **Development/Programmer Support**
  - Third party software and programmers
  - ICT PLACE Development Software and PDS-3 programmer
- **Architectural Flexibility**
  - 132 product term X 44 input AND array
  - Up to 22 inputs and 10 outputs
  - 4 configurations per macrocell
  - Synchronous preset, asynchronous clear
  - Independent output enables
  - 24-pin DIP and 28-pin PLCC
- **Application Versatility**
  - Replaces random logic
  - Pin and JEDEC compatible with 22V10

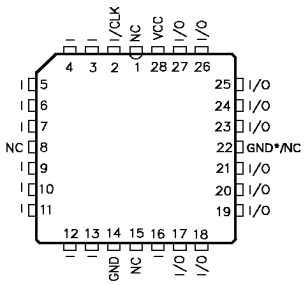
General Description

The PEEL22V10 is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL22V10 offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL22V10 is available in 24-pin DIP and 28-pin PLCC packages with speeds ranging from 15nS to 25nS with power consumption as low as 67mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability, thus ensuring the highest quality possbile. The PEEL22V10 is JEDEC file compatible with standard 22V10 PLDs. Development and programming support for the PEEL22V10 is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

Pin Configuration (Figure 1)

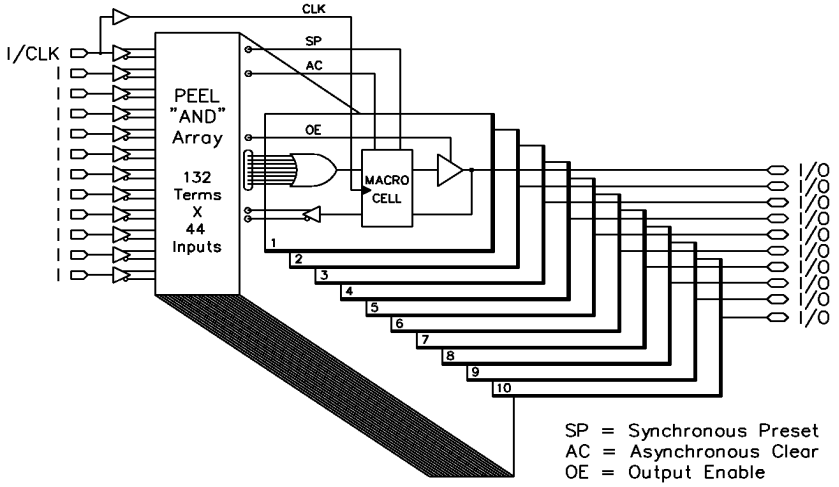


DIP



PLCC

Block Diagram (Figure 2)



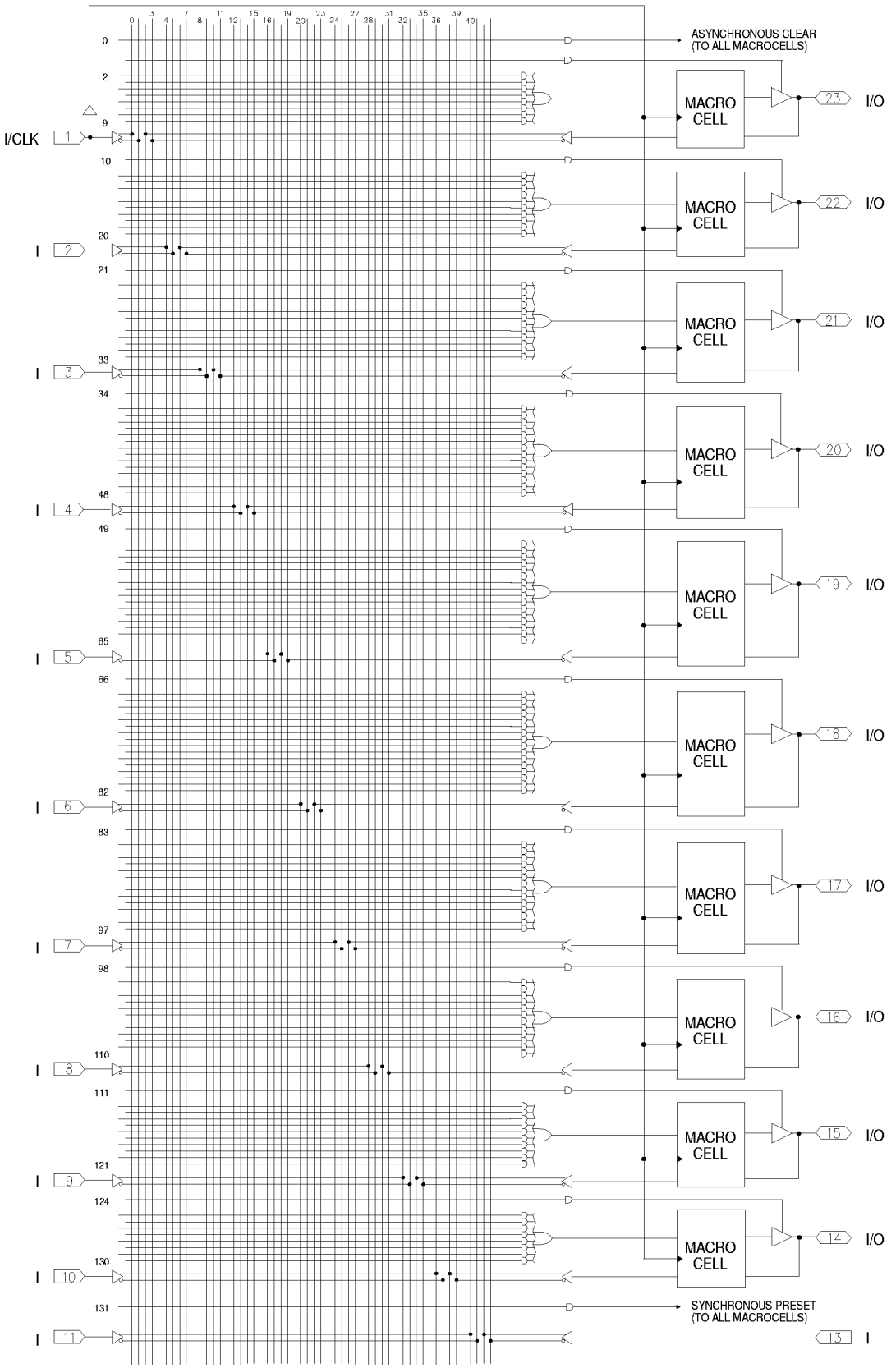


Figure 3. PEEL22V10 Logic Array Diagram

Function Description

The PEEL22V10 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL22V10 architecture is illustrated in the block diagram of Figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure, the PEEL22V10 can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 4 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions with either active-high or active-low polarity.

AND/OR Logic Array

The programmable AND array of the PEEL22V10 (shown in Figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

132 product terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12, 14 and 16) used to form logical sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous present term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and compliment of an input signal will always be FALSE, and thus will not effect the OR function that it drives. When all the connectionS on a product term are opened, a “don’t care” state exists and that term will always be TRUE.

When programming the PEEL22V10, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is then configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program the connections on unused product terms so that they will have no effect on the output function.)

Variable Product Term Distribution

The PEEL22V10 provides 120 product terms to drive the 10 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14 and 16 to form logical sums (see Figure 3). This distribution allows optimum use of device resources.

Programmable I/O Macrocell

The output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL22V10 to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in Figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the two EEPROM bits controlling these multiplexers (refer to Table 1). These bits determine output polarity and output type (registered or non-registered). Equivalent circuits for the four macrocell configurationS are illustrated in Figure 5.

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated out-

put. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

When configuring an I/O macrocell to implement a registered function (configurations 1 and 2 in Figure 5), the Q output of the flip-flop drives the feedback term. When configuring an I/O macrocell to implement a combinatorial function (configurationS 3 and 4 in Figure 5), the feedback signal is taken from the I/O pin. In this case, the pin can be used as a dedicated input or a bi-directional I/O. (Refer also to Table 1.)

Design Security

The PEEL22V10 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step after the device has been programmed. Once the security bit is set, it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

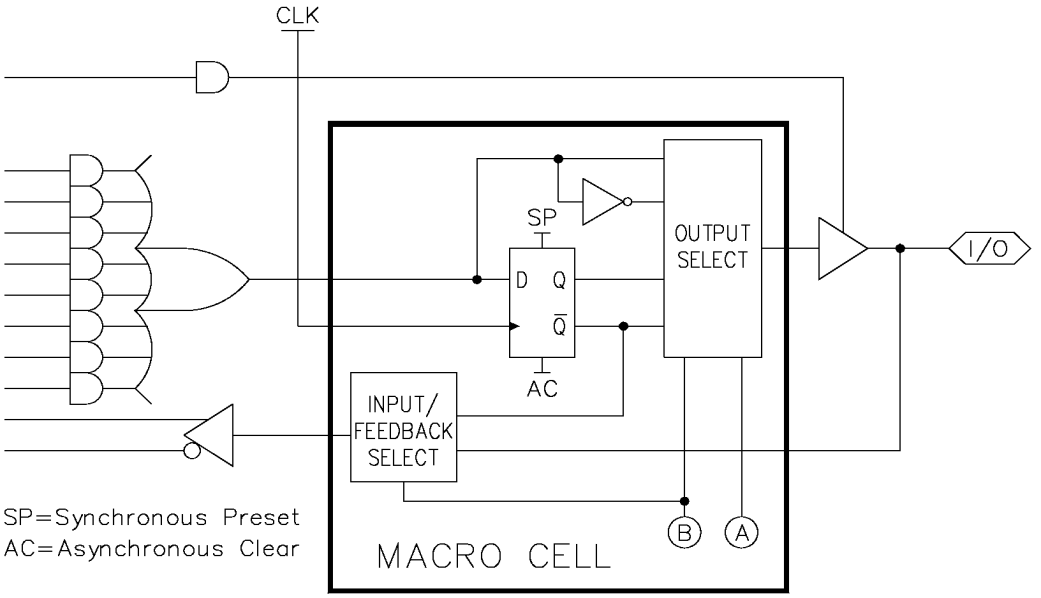


Figure 4. Block Diagram of the PEEL22V10 I/O Macrocell

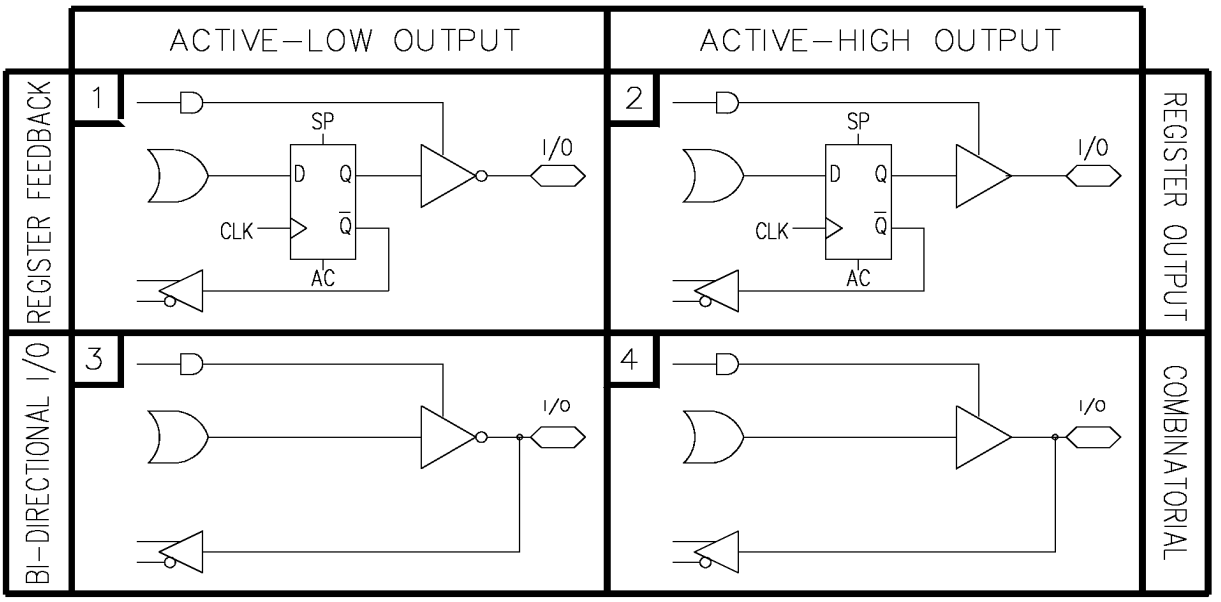


Figure 5. Equivalent Circuits for the Four Configurations of the PEEL22V10 I/0 Macrocell.

Configuration			Input/Feedback Select	Output Select	
#	A	B			
1	0	0	Register Feedback	Register	Active Low
2	1	0			Active High
3	0	1	Bi-Directional I/O	Combinatorial	Active Low
4	1	1			Active High

Table 1. PEEL22V10 Macrocell Configuration Bits

Absolute Maximum Ratings

This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin[2]	Relative to Ground[1]	-0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	±25	mA
T_{ST}	Storage Temperature		-65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	+70	°C
T_R	Clock Rise Time	See Note 3		20	nS
T_F	Clock Fall Time	See Note 3		20	nS
T_{RVCC}	V_{CC} Rise Time	See Note 3		250	ms

D.C. Electrical Characteristics Over the operating range

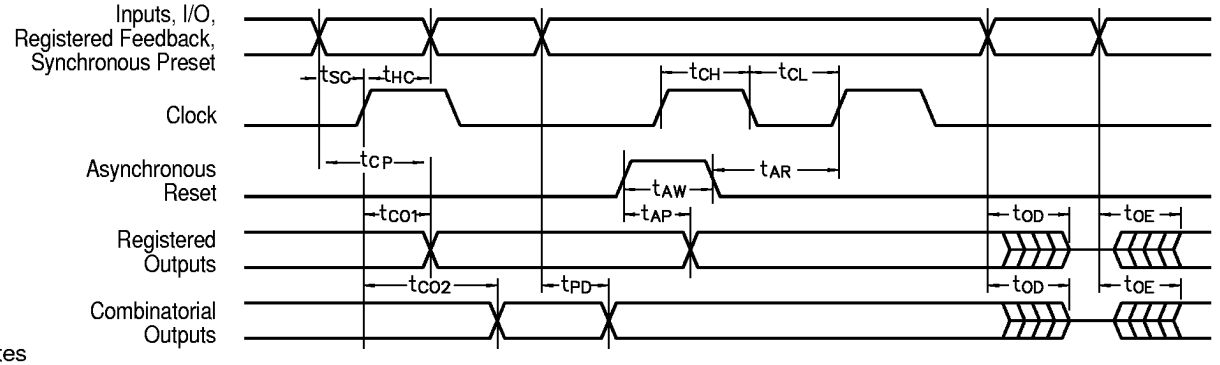
Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = -4.0mA		2.4		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA			0.5	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			-0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}			±10	µA
I_{SC}	Output Short Circuit Current	V_{CC} = 5V, V_O = 0.5V[9], T_A = 25°C		-30	-135	mA
I_{CC}	VCC Current (See CR-1 for typical ICC)	VIN = 0V or 3V f = 25MHz All outputs disabled[4]	-15		135	
			-25		67	
C_{IN}[7]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz			6	pF
C_{OUT}[7]	Output Capacitance				12	pF

A.C. Electrical Characteristics

Over the Operating Range [8, 11]

Symbol	Parameter	-15		-25		Unit
		Min	Max	Min	Max	
t_{PD}	Input[5] to non-registered output		15		25	ns
t_{OE}	Input[5] to output enable[6]		15		25	ns
t_{OD}	Input[5] to output disable[6]		15		25	ns
t_{CO1}	Clock to output		8		15	ns
t_{CO2}	Clock to comb. output delay via internal registered feedback		17		35	ns
t_{CF}	Clock to Feedback		5		9	ns
t_{SC}	Input[5] or feedback setup to clock	8		15		ns
t_{HC}	Input[5] hold after clock	0		0		ns
t_{CL}, t_{CH}	Clock low time, clock high time[8]	6		13		ns
t_{CP}	Min clock period Ext (t_{SC} + t_{CO1})	18		30		ns
f_{MAX1}	Internal Feedback ($1/t_{SC}+t_{CF}$)[12]	76.9		41.6		MHz
f_{MAX2}	External Feedback ($1/t_{CP}$)[12]	62.5		33.3		MHz
f_{MAX3}	No Feedback ($1/t_{CL}+t_{CH}$)[12]	83.3		38.4		MHz
t_{AW}	Asynchronous Reset pulse width	15		25		ns
t_{AP}	Input[5] to Asynchronous Reset		15		25	ns
t_{AR}	Asynch. Reset recovery time		15		25	ns
t_{RESET}	Power-on reset time for registers in clear state		5		5	µs

Switching Waveforms



Notes

1. Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20nS.
2. V_I and V_O are not specified for program/verify operation.
3. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
4. I/O pinS are 0V and 3V.
5. "Input" refers to an Input pin signal.
6. t_{OE} is measured from input tranSition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input tranSition to V_{OH} - 0.1V or V_{OL} + 0.1V; $V_{REF} = V_L$ see 22CV10 for test loads in Section 6 of the 1995/1996 Data Book.
7. Capacitances are tested on a sample basis.
8. Test conditionS assume: signal tranSition times of 3nS or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
9. Test one output at a time for a duration of less than 1 sec.
10. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
11. PEEL Device test loads are specified in Section 6 of the 1995/1996 Data Book.
12. Parameters are not 100% tested. SpecificationS are based on initial characterization and are tested after any design or process modification which may affect operational frequency.
13. Available only for 22V10A-15, 25 grades.

Ordering Information

PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PEEL22V10P-15	15nS	C	P24
PEEL22V10J-15	15nS	C	J28
PEEL22V10P-25	25nS	C	P24
PEEL22V10J-25	25nS	C	J28

Part Number