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CMOS Programmable Electrically Erasable Logic Device

Preliminary Data Sheet

T-46-13-47

PEEL™ 253

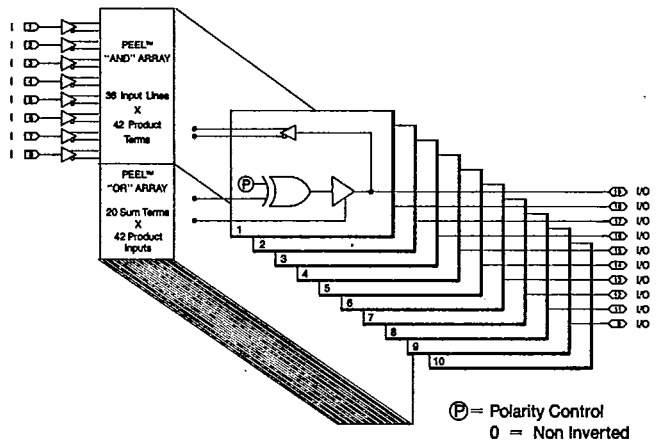
Features

- **Advanced CMOS E^2PROM Technology**
- **Low Power Consumption**
  —CMOS: 25mA + .7mA/MHz Max
  —TTL: 35mA + .7mA/MHz Max
- **High Performance**
  —T_{PD} 30nS Max, T_{OE} 30nS Max
- **Reprogrammability**
  —100% factory tested
  —Cost effective window-less package
  —Erases and programs in seconds
  —Adds convenience, reduces field retrofit and development cost
- **Development/Programmer Support**
  —Popular third party development tools and stand alone programmers
  —PC based evaluation and development tools from Gould
- **Plug-In Compatibility**
  —Signetics PLS 153, ICT 253
  —PC-based software translates existing JEDEC files to PEEL253 format
- **Architectural and Design Enhancements**
  —8 dedicated inputs, 10 I/O pins
  —Dual programmable logic arrays: AND (36 inputs X 42 product terms) OR (20 sum terms X 42 products)
  —Sharing of all 42 product terms
  —I/O polarity controls
  —Output enable terms in OR array
  —Security from unauthorized copying
  —Signature word for user specified ID
- **Application Versatility**
  —Replaces random SSI/MSI logic
  —Ideal for customized combinatorial functions: comparators, multiplexers, encoders, converters, etc.

General Description

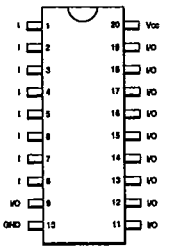
The Gould PEEL™ 253 is a CMOS Programmable Electrically Erasable Logic device that provides a high performance, low power, reprogrammable, and architecturally enhanced alternative to conventional programma-

Block Diagram



Ⓟ = Polarity Control
0 = Non Inverted
1 = Inverted

Pin Diagram



Pin Names

I = Input Only
I/O = Bi-Directional Input/Output
GND = Ground
Vcc = Power Supply (+5V)

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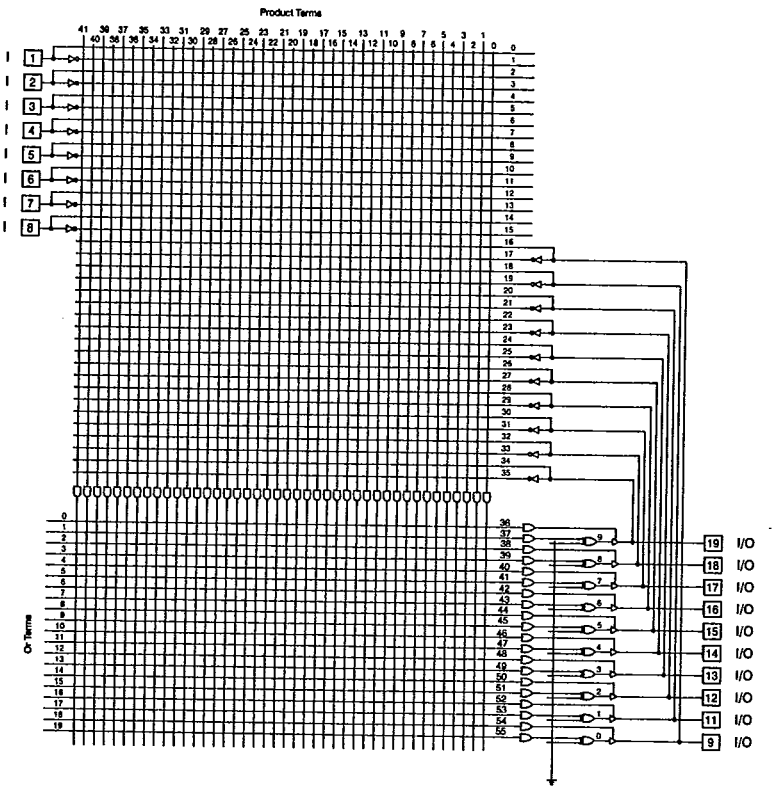
ble logic devices (PLDs). Designed in advanced CMOS E^2PROM technology, the PEEL 253 rivals speed parameters of comparable bipolar PLDs with a substantial improvement in power consumption. The E^2 reprogrammability of the PEEL 253 not only reduces development and field retrofit costs but enhances testability ensuring 100% field programmability and function. Additionally, the PEEL 253 technology allows for cost effective "window-less" packaging in a 20-pin 300-mil DIP.

Providing both programmable "AND" and programmable "OR" arrays, the PEEL 253 offers functional compatibility to the Signetics PLS153 (previously numbered 82S153) plus several architectural enhancements including: output enable terms in the "OR" array, 10 additional general purpose product terms, security from unauthorized copying of designs, and signature word for user specified device identification. Applications of the PEEL 253 include replacement of random SSI/MSI logic circuitry and a wide range of combinatorial logic functions, such as priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. Development and programming for the PEEL 253 is supported by popular development tools and programmers from third-party manufacturers, plus PC-based PEEL Development System from Gould.

PEEL253 Logic Array Diagram



PLDs

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Absolute Maximum Ratings Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	−0.6 to +7.0	V
V_{IO}	Voltage Applied to Any Pin[8]	Relative to GND[1]	−0.6 to V_{CC} + 0.6	V
T_A	Ambient Temp, Power Applied		−10 to +85	°C
T_{ST}	Storage Temperature		−65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 Seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	70	°C

D.C. Electrical Characteristics Over the operating range.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		−0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −3.2mA	2.4		V
V_{OHC}	Output HIGH Voltage CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8mA[4]		0.5	V
V_{OLC}	Output LOW Voltage CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
I_L	Input Leakage Current	V_{CC} = Max, GND ≤ V_I ≤ V_{CC}		10	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max, V_O = GND	−30	−90	mA
I_{OZ}	Output Leakage Current	I/O = High Impedence V_{CC} = Max, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{CCSC}	Power Supply Current, Standby, CMOS Interface	All Inputs = GND or V_{CC}[3]		35	mA
I_{CCAC}	Power Supply Current, Active, CMOS Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching[3].		I_{CCSC} + 0.5mA/MHz	mA
I_{CCST}	Power Supply Current, Standby, TTL Interface	V_{IN} = V_{IL} or V_{IH}[3]		45	mA
I_{CCAT}	Power Supply Current, Active, TTL Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching[3].		I_{CCST} + 0.5mA/MHz	mA

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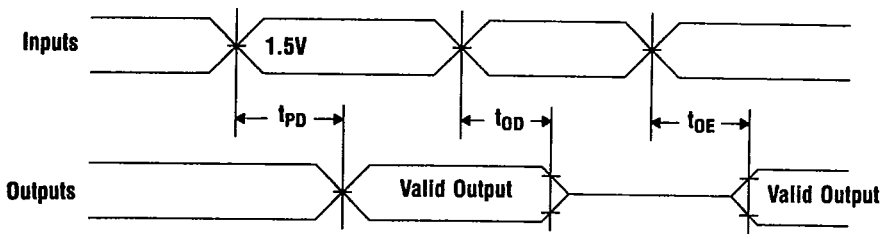
Capacitance These measurements are periodically sample tested.

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C V_{CC} = 5.0V, f = 1kHz		6	pF
C_{OUT}	Output Capacitance			12	pF

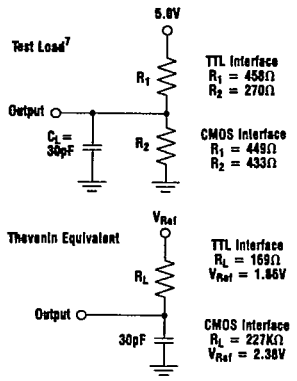
A.C. Electrical Characteristics Over the operating range[5].

Symbol	Parameter	253–30		253–35		253–40		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Propagation Delay, Input to Output		30		35		40	ns
t_{OE}	Input to Output Enable[6]		30		35		40	ns
t_{OD}	Input to Output Disable[6,7]		30		35		40	ns

Switching Waveforms



Test Loads



Notes:

1. Minimum DC input is −0.5V, however, inputs may undershoot to −2.0V for periods less than 30ns.
2. Test one output at a time. Duration of short circuit should not exceed 1 second.
3. All I/O pins open (no load).
4. Assumes worst-case conditions—all outputs loaded. V_{OL} = 0.5V @ I_{OL} = 15mA with one output loaded.
5. Test conditions assume: signal transitions of 5ns or less from the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified); and test loads shown.
6. t_{OD} and t_{OE} are measured at V_{OH} −0.1V and V_{OL} +0.1V.
7. C_L includes scope and jig capacitance. t_{OD} is measured with C_L = 5pF.
8. V_{IO} specified is not for program/verify operation. Contact Gould for information regarding PEEL253 program/verify specifications.

PLDs

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Preliminary Designation

The "Preliminary" designation on a Gould data sheet indicates that the product is not characterized. The specifications are subject to change, are based on design goals or preliminary part evaluation, and are not guaranteed. Gould or an authorized sales representative should be consulted for current information before using this product.

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