ANALOG DEVICES

T-51-09-12

Monolithic Octal 12-Bit DACPORTs

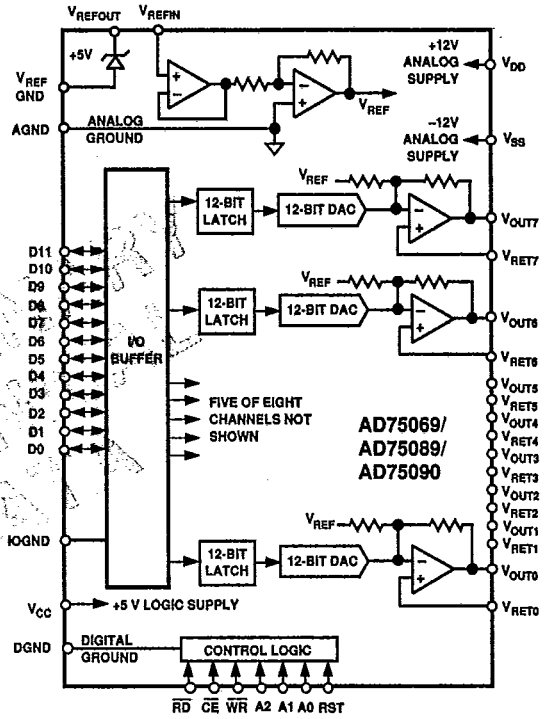
AD75069/AD75089/AD75090

2

FEATURES
- Eight Complete Voltage Output DACs
- On-Chip Voltage Reference
- On-Chip Data Latches with Readback Feature
- Variety of Output Voltage Ranges: +7.5 V/−2.5 V, ± 5 V, ±10 V
- Compact 44-Pin PLCC and Ceramic JLCC Packages

APPLICATIONS
- Automatic Test Equipment
- Instrumentation
- Avionics
- Robotics
- Process Control

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD75069/AD75089/AD75090 DACPORTs™ contain eight complete 12-bit, voltage output digital-to-analog converters in one monolithic IC. They thus offer the highest density 12-bit D/A functions available. The three models differ in their output voltage ranges: the AD75069 outputs −2.5 V to +7.5 V, the AD75089 outputs ±5 V, and the AD75090 outputs ±10 V.

Each DAC offers flexibility, accuracy and good dynamic performance. The R-2R structure is fabricated from thin-film resistors that are laser-trimmed to achieve guaranteed monotonicity over the full operating temperature range. DAC-to-DAC matching performance is specified.

The output amplifier combines the best features of bipolar and MOS devices to achieve good dynamic performance and low offset. Settling time is under 10 μs, and each output can drive a 2 mA, 500 pF load. Short circuit protection allows indefinite shorts to V_{CC}, V_{DD}, V_{SS}, and GND.

Digital circuitry is implemented in CMOS logic. The fast, low power, digital interface allows these DACPORTs to interface with most microprocessors through a single 12-bit wide bus. A readback feature allows the internal DAC registers to be read back through the digital port, as 12-bit words. When disabled, the readback drivers are placed in a high impedance mode.

A RESET control pin is provided to allow simultaneous asynchronous reset of all DAC data latches, causing the DAC outputs to go to the negative extreme of their range.

The analog portion of these DACPORTs consists of eight DAC cells, eight output amplifiers, a voltage reference, a control amplifier and switches. Each DAC cell is an inverting R-2R type. The output current from each DAC is switched to the on-chip application resistors and output amplifier. The chip may be operated from the internal reference or an external reference.

The high performance and functional completeness of these DACPORTs result from their fabrication in Analog Devices' BiMOS II process. This epitaxial BiCMOS process features bipolar transistors for precise analog circuitry, CMOS transistors for dense logic and analog switches, laser-trimmed thin-film resistors and double-level metal interconnects.

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AD75069/AD75089/AD75090—SPECIFICATIONS

(V_{CC} = +5 V, V_{DD} = +12 V, V_{SS} = −12 V, V_{REF} = +5 V, T_A = +25°C unless otherwise noted.)

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Parameter	Min	Typ	Max	Units
RESOLUTION		12		Bits
ANALOG OUTPUT				
Voltage Range, V_{OUT} max to V_{OUT} min				
AD75069		−2.5/+7.5		Volts
AD75089		±5		Volts
AD75090		±10		Volts
Output Current (Each Channel, Source or Sink)	2			mA
Load Capacitance			500	pF
Short Circuit Current (Each Channel)		25	40	mA
ACCURACY				
Gain Error, Including Internal Reference	−10	±5	10	LSB
Midscale Error	−4	±1/2	4	LSB
Integral Linearity Error	−1/2	±1/4	1/2	LSB
Integral Linearity Error, T_{MIN} to T_{MAX}	−1.5	±1/2	+1.5	LSB
Differential Linearity Error	−1/2	±1/4	1/2	LSB
Differential Linearity Error, T_{MIN} to T_{MAX}	−3/4	±1/2	+3/4	LSB
Gain Error Drift	−10	±5	10	ppm of FSR/°C
Midscale Drift	−10	±5	10	ppm of FSR/°C
Reference Temperature Coefficient	−25	±15	25	ppm/°C
Noise, 0.1 to 2 MHz Band				
AD75069, AD75089 (10 V Span)			300	μV rms
AD75090 (20 Span)			600	μV rms
REFERENCE INPUT				
Input Resistance	2.0	10		MΩ
Voltage Range	−3.0		+5.5	Volts
POWER REQUIREMENTS				
V_{CC}	4.5	5.0	5.5	Volts
I_{CC}		0.1	1	mA
V_{DD}, V_{SS}	±11.4	±12.0	±13.2	Volts
I_{DD}		15	20	mA
I_{SS}		−14	−16	mA
Total Power		350	432	mW
ANALOG GROUND CURRENT[1] PER EACH OF 8 CHANNELS	−600		+600	μA
MATCHING PERFORMANCE				
Gain[2]	−5	±2.5	5	LSB
Midscale[3]	−4	±2	4	LSB
Linearity[4]	−1	±1/2	1	LSB
CROSSTALK				
Analog (DC)			−90	dB
Digital (Transient)			−60	dB
DYNAMIC PERFORMANCE (R_L = 5 kΩ, C_L = 500 pF)				
Slew Rate	2.0	2.5		V/μs
Settling Time to ±1/2 LSB				
V_{OUT} max to V_{OUT} min or V_{OUT} min to V_{OUT} max				
AD75069, AD75089 (10 V Span)		6	8	μs
AD75090 (20 V Span)		8	10	μs
POWER SUPPLY GAIN SENSITIVITY				
11.4 V ≤ V_{DD} ≤ 13.2 V		±6	±10	ppm/%
−13.2 V ≤ V_{SS} ≤ −11.4 V		±1	±2	ppm/%

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Parameter	Min	Typ	Max	Units
DIGITAL INPUTS				
V_{IH}	2.0			Volts
V_{IL}	0		0.8	Volts
I_{IH} @ V_{IN} = V_{LL}	−10	±1	10	μA
I_{IL} @ V_{IN} = DGND	−10	±1	10	μA
DIGITAL OUTPUTS				
V_{OL} @ I_{SINK} = 1.6 mA			0.4	Volts
V_{OH} @ I_{SOURCE} = 0.5 mA	2.4			Volts
DIGITAL TIMING[5]				
Data Write Mode (Figure 1)				
Data Setup Time, t_{DSU}	30			ns
Address Setup Time, t_{ASU}	30			ns
Chip Enable-Write Time, t_{CEW}	10			ns
Write Pulse Width, T_W	80			ns
Write-Chip Enable Time, t_{WCE}	0			ns
Address Hold Time, t_{AH}	20			ns
Data Hold Time, t_{DH}	50			ns
Data Readback Mode (Figure 2)				
Address Setup Time , t_{ASU}	30			ns
Chip Enable-Read Time, t_{CER}	0			ns
Read Pulse Width, t_R	70			ns
Access Time from Read, t_{RD}			75	ns
Access Time from Chip Enable, t_{CED}			85	ns
Access Time from Address Change, t_{AD}			120	ns
Data Bus Release Time, t_{REL}			30	ns
Read-Chip Enable Time, t_{RCE}	0			ns
Address Hold Time, t_{AH}	20			ns
Asynchronous Reset				
Reset Pulse Width, t_{RST}	80			ns
TEMPERATURE RANGE (T_{MIN}, T_{MAX})				
A Versions	−40		+85	°C
J Versions	0		+70	°C

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NOTES
[1]Analog ground current is input code dependent.
[2]Gain matching error is the largest difference in gain error between any two DACs in one package.
[3]Midscale matching error is the largest difference in midscale values between any two DACs in one package.
[4]Linearity matching error is the difference in the worst case integral linearity error between any two DACs in one package.
[5]Reference level for timing measurements = 1.5 V.
See definitions of specifications later on in this data sheet.
Specifications subject to change without notice.
Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

TIMING DIAGRAMS

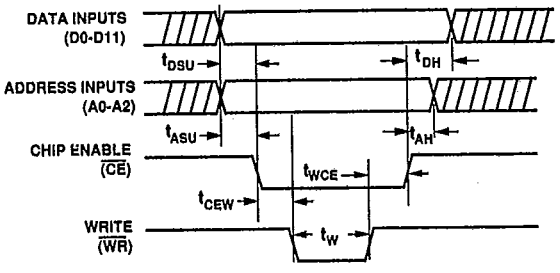

Figure 1. Write Timing Diagram

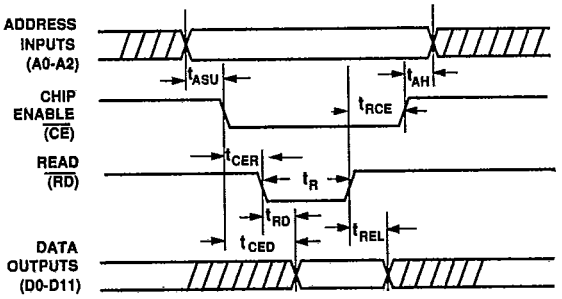

Figure 2. Readback Timing Diagram

AD75069/AD75089/AD75090

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ABSOLUTE MAXIMUM RATINGS*

(Specifications apply to all grades except where noted)

V_{CC} to DGND or IOGND . . . . . 0 V to + 7 V
V_{DD} to AGND . . . . . 0 V to +18 V
V_{SS} to AGND . . . . . −18 V to 0 V
AGND to DGND . . . . . −1 V to +1 V
AGND to VREFGND . . . . . ±13.2 V
AGND to VRET0–7 . . . . . ±13.2 V
V_{REFIN} Input . . . . . V_{DD} to V_{SS}
V_{DD} to V_{SS} . . . . . 0 V to +26.4 V
Digital Inputs . . . . . −0.3 V to +7 V
Analog Outputs
. . . . . Indefinite Shorts to V_{CC},V_{DD},V_{SS}, and AGND
Soldering Temperature . . . . . +300°C, 10 sec
Power Dissipation . . . . . 1000 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Output Voltage Range	Temperature Range	Package Option*
AD75069JP	−2.5 V/+7.5 V	0°C to +70°C	P-44A
AD75069AJ	−2.5 V/+7.5 V	−40°C to +85°C	J-44A
AD75089JP	± 5 V	0°C to +70°C	P-44A
AD75089AJ	± 5 V	−40°C to +85°C	J-44A
AD75090JP	±10 V	0°C to +70°C	P-44A
AD75090AJ	±10 V	−40°C to +85°C	J-44A

*J = J-Leaded Ceramic Chip Carrier; P = Plastic Leaded Chip Carrier (PLCC) package. For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

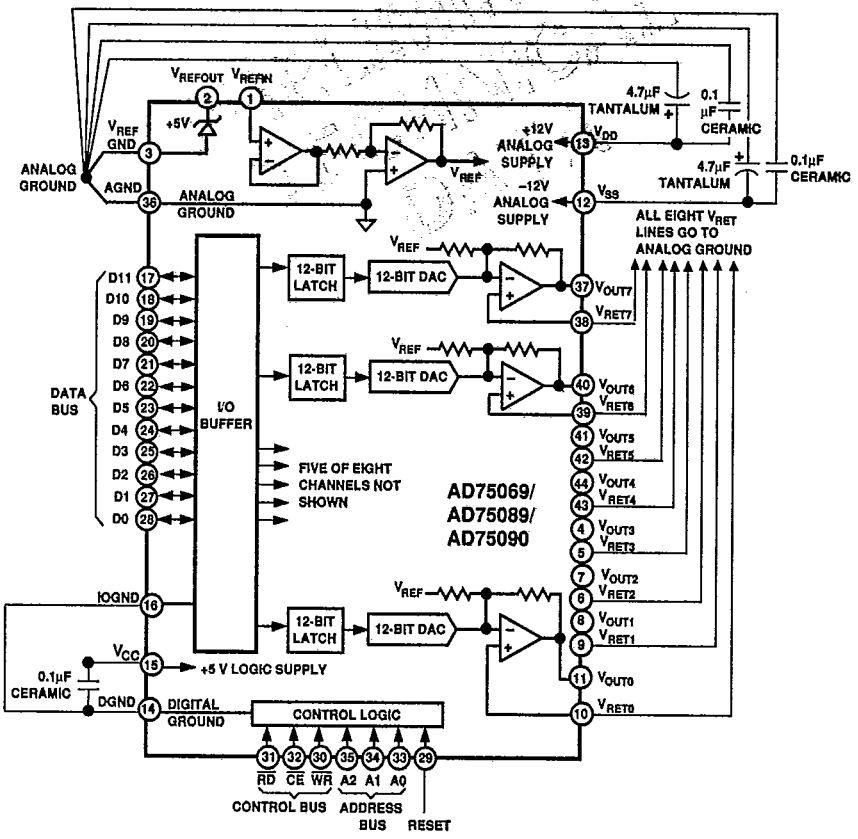

Figure 3. Recommended Circuit Schematic

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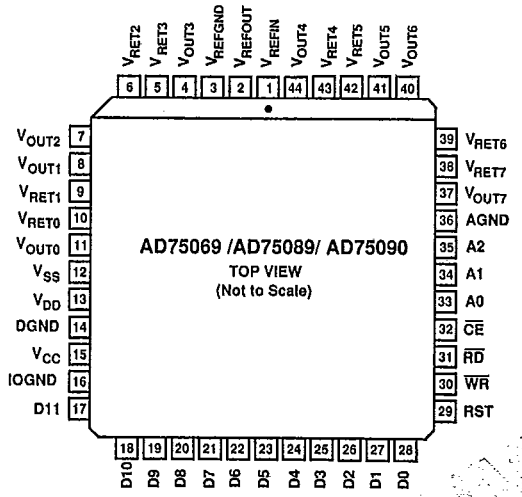
PIN CONFIGURATION

44-Pin PLCC Package



PIN DESCRIPTIONS

Pin	Name	Description
1	V_{REFIN}	Reference Input
2	V_{REFOUT}	5 V Reference Output
3	V_{REFGND}	Reference Ground
4	V_{OUT3}	Analog Output 3
5	V_{RET3}	Analog Return 3
6	V_{RET2}	Analog Return 2
7	V_{OUT2}	Analog Output 2
8	V_{OUT1}	Analog Output 1
9	V_{RET1}	Analog Return 1
10	V_{RET0}	Analog Return 0
11	V_{OUT0}	Analog Output 0
12	V_{SS}	−12 V Analog Power Supply
13	V_{DD}	+12 V Analog Power Supply
14	DGND	Digital Ground
15	V_{CC}	+5 V Digital Power Supply
16	IOGND	Bus Interface Ground
17	D11	Data Input Bit 11 (MSB)
18	D10	Data Input Bit 10
19	D9	Data Input Bit 9
20	D8	Data Input Bit 8
21	D7	Data Input Bit 7
22	D6	Data Input Bit 6
23	D5	Data Input Bit 5
24	D4	Data Input Bit 4
25	D3	Data Input Bit 3
26	D2	Data Input Bit 2
27	D1	Data Input Bit 1
28	D0	Data Input Bit 0 (LSB)
29	RST	Reset Input; Active High
30	$\overline{WR}$	Write Input; Active Low
31	$\overline{RD}$	Read Input; Active Low
32	$\overline{CE}$	Chip Enable Input; Active Low
33	A0	Address Input Bit 0 (LSB)
34	A1	Address Input Bit 1
35	A2	Address Input Bit 2 (MSB)
36	AGND	Analog Ground
37	V_{OUT7}	Analog Output 7
38	V_{RET7}	Analog Return 7
39	V_{RET6}	Analog Return 6
40	V_{OUT6}	Analog Output 6
41	V_{OUT5}	Analog Output 5
42	V_{RET5}	Analog Return 5
43	V_{RET4}	Analog Return 4
44	V_{OUT4}	Analog Output 4

DEFINITIONS OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR: Integral linearity error is the maximum deviation of the actual DAC output from the ideal analog output (a straight line drawn from −full scale to +full scale) for any digital input code.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a nondecreasing function of input. All versions of the AD75069/AD75089/AD75090 are monotonic over their full operating temperature range.

DIFFERENTIAL LINEARITY ERROR: Monotonic behavior requires that the differential linearity error be less than 1 LSB over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code. For example, for a 10 V output span, a change of 1 LSB in digital input code should result in a 2.44 mV change in the analog output (1 LSB = 10 V/4096 = 2.44 mV). If in actual use, however, a 1 LSB change in the input code results in a change of only 0.61 mV (1/4 LSB) in analog output, the differential nonlinearity error would be −1.83 mV, or −3/4 LSB.

GAIN ERROR: DAC gain error is a measure of the difference between the output span of an ideal DAC and an actual device.

MIDSCALE ERROR: Midscale error is the difference between the ideal midscale output and the actual output of a DAC when the input code is loaded with the MSB = "1" and the rest of the bits = "0."

SETTLING TIME: Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition.

CROSSTALK: Crosstalk is the change in an output caused by a change in one or more of the other inputs or outputs. It is due to capacitive and thermal coupling between channels.

FULL-SCALE RANGE: FSR is 20 V for ±10 V range and 10 V for ±5 V and −2.5/+7.5 V ranges.

TRANSISTOR COUNT

The AD75069/AD75089/AD75090 contains 5,225 transistors.

AD75069/AD75089/AD75090

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BINARY CODE TABLE

Offset Binary Value in DAC Latch	Analog Output Voltage
MSB LSB	
1111 1111 1111	V_{OUT} max
1000 0000 0000	Midscale = (V_{OUT} max + 1 LSB − V_{OUT} min)/2
0000 0000 0000	V_{OUT} min

ANALOG CIRCUIT CONSIDERATIONS

Grounding Recommendations

The AD75069/AD75089/AD75090 have twelve pins for analog and digital grounds, designated AGND, V_{RET0}–V_{RET7}, V_{REFGND}, IOGND, and DGND. The AGND pin is the ground reference point for the device. V_{REFGND} is the ground reference point for the on-chip voltage reference. V_{RET0} through V_{RET7} are the 8 ground return pins for the 8 DACs and their output amplifiers. The 10 analog ground pins should be connected radially to the analog ground point in the system. The external reference and any external loads should also be returned to the analog ground point. To minimize crosstalk, all paths to the single analog ground point must be short and direct.

The IOGND and DGND pins should be connected to the digital ground point in the circuit. These pins return current from the bus interface and logic portions, respectively, of the AD75069/AD75089/AD75090 circuitry to ground.

Analog and digital grounds should be connected at one point in the system. If there is a possibility that this connection may be broken or otherwise disconnected, then two diodes should be connected in inverse parallel between the analog and digital ground pins of the AD75069/AD75089/AD75090 to limit the maximum ground voltage difference.

Power Supplies and Decoupling

The AD75069/AD75089/AD75090 require three power supplies for proper operation. V_{CC} powers the logic portions of the device and requires +5 volts. V_{DD} and V_{SS} power the remaining portions of the circuitry and require ±12 V.

Decoupling capacitors should be used on all power supply pins. Good engineering practice dictates that the bypass capacitors be located as near as possible to the package pins. Recommended values are 4.7 μF tantalum and 0.1 μF ceramic from V_{DD} and V_{SS} to analog ground, and 0.1 μF from V_{CC} to digital ground.

Voltage Reference

The AD75069/AD75089/AD75090 are designed to operate from a reference voltage of 5 V. The internal reference can serve the entire chip. If superior tolerance, PSRR, or temperature performance are needed, external devices, such as the AD586, may be used.

Output Considerations

Each DAC output can source or sink ±2 mA of current to an external load. Short-circuit protection limits load current to a maximum load current of 40 mA. Load capacitance of up to 500 pF can be accommodated with no effect on stability.

AD75069/AD75089/AD75090 output voltage settling time is 10 μs maximum. Figure 4 shows the output voltage settling time of the AD75069 with a fixed 5 V reference and all bits switched from 1 to 0 and from 0 to 1.

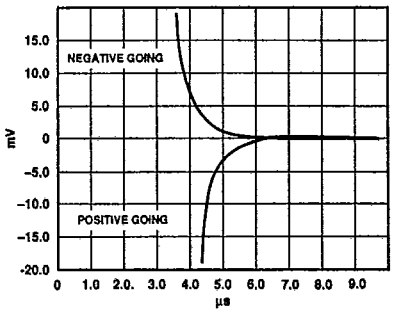

Figure 4. Settling Time; Full-Scale Output Change

Crosstalk

Crosstalk is a spurious signal on one DAC output caused by a change in one or more of the other DACs. Crosstalk can be induced by capacitive, thermal, or load-current induced feedthrough. Figure 5 shows typical crosstalk. The upper trace of the top photo shows DAC 6 switching from −2.5 V to +7.5 V and back to −2.5 V. The lower trace shows brief spikes in the output of DAC 7 caused by capacitive feedthrough from the input data. The longer disturbances are caused by analog feedthrough from DAC 6's output. The loads of both DACs are 5 kΩ in parallel with 500 pF. The lower photo shows the detail of the falling edge of DAC 6 (large trace) and the effect on DAC 7 (middle trace) under the same conditions.

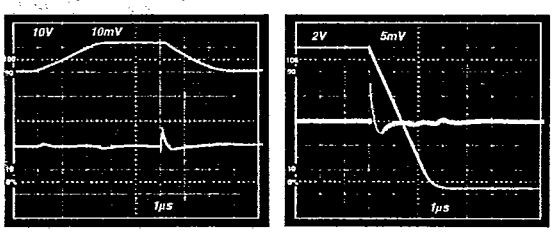

Figure 5. Output Crosstalk

DIGITAL INTERFACING

To write to the chip, apply the desired address, and then take Chip Enable ($\overline{CE}$) and Write ($\overline{WR}$) low. Typically, $\overline{CE}$ is tied to the system address decoder, and $\overline{WR}$ connects to the system write strobe.

If the data is changed while $\overline{CE}$ and $\overline{WR}$ are low, the DAC register is transparent, and it will follow the input data.

Readback

To read data back from the chip, apply the desired address, and then take Chip Enable ($\overline{CE}$) and Read ($\overline{RD}$) low. Typically, $\overline{CE}$ is tied to the system address decoder, and $\overline{RD}$ connects to the system read strobe.

If the address is changed while $\overline{CE}$ and $\overline{RD}$ are low, the data output will follow the selected address after a delay of t_{AD}.

Data Reset

To reset all data latches asynchronously, take Reset (RST) high. This clears all data latches and causes the DAC outputs to go to the negative end of their output range, i.e., −2.5 V for the AD75069, −5 V for the AD75089, and −10 V for the AD75090.