MAXIM

CMOS Dual 8-Bit Buffered Multiplying DACs

T-51-09-08

General Description

The AD7528/AD7628 contains two 8-bit multiplying digital-to-analog converters (DACs). Separate on-chip latches hold the input data for each DAC to allow easy interface to microprocessors. The data load operation is similar to a static RAM write cycle. Data is loaded using only CS, WR, and DAC Select (DAC A/DAC B) inputs.

Each DAC has a separate reference input and internal feedback resistor which allow fully independent operation while maintaining excellent DAC-to-DAC matching.

The AD7528 operates from a single +5V to +15V power supply whereas the AD7628 operates from +12V to +15V. The AD7528 has TTL compatible inputs at +5V supply only and the AD7628 has TTL compatible inputs from +12V to +15V supplies.

The AD7528/AD7628 is supplied in 20-lead narrow DIP and Small Outline Packages.

Applications

Programmable Attenuators
Digitally Controlled Filters
X-Y Graphics
Motion Control Systems
Digital-to-Synchro Conversion
Disk Drives

Features

- Data Latches For Both DACs
- AD7528—+5V to +15V Single Supply Operation
- AD7628—+12V to +15V Single Supply Operation With TTL/CMOS Compatible Inputs
- ±½ LSB Linearity
- Microprocessor Compatible
- Four-Quadrant Multiplication
- DACs Matched to 1%

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7528JN	0°C to +70°C	Plastic DIP	±1 LSB
AD7528KN	0°C to +70°C	Plastic DIP	±½ LSB
AD7528LN	0°C to +70°C	Plastic DIP	±½ LSB
AD7528JCWP	0°C to +70°C	Small Outline	±1 LSB
AD7528KCWP	0°C to +70°C	Small Outline	±½ LSB
AD7528LCWP	0°C to +70°C	Small Outline	±½ LSB
AD7528JC/D	0°C to +70°C	Dice	±1 LSB
AD7528AQ	-25°C to +85°C	CERDIP**	±1 LSB
AD7528BQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7528CQ	-25°C to +85°C	CERDIP**	±½ LSB

* *All devices — 20 lead packages*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*

Ordering Information continued on last page.

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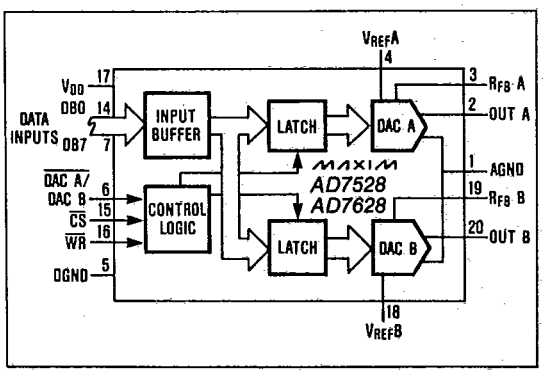
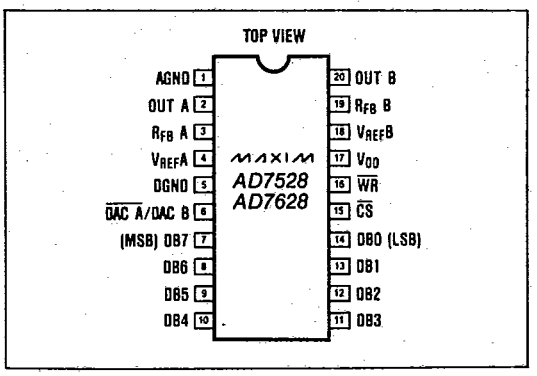
Functional Diagram



Pin Configuration



CMOS Dual 8-Bit Buffered Multiplying DACs

ABSOLUTE MAXIMUM RATINGS—AD7528, AD7628

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V, +17V
AGND to DGND ..... V_{DD}
DGND to AGND ..... V_{DD}
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
Pin 2, Pin 20 to AGND ..... -0.3V, V_{DD}
$V_{REF}A$, $V_{REF}B$ to AGND ..... ±25V
$V_{RFB}A$, $V_{RFB}B$ to AGND ..... ±25V

Operating Temperature Ranges
AD7528JN, KN, LN, JCWP,
KCWP, LCWP; AD7628KN, KCWP ..... 0°C to +70°C
AD7528AQ, BQ, CQ; AD7628BQ ..... -25°C to +85°C
AD7528SD, SQ, TD, TQ;
UD, UQ; AD7628TQ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) to +75°C 450mW
Derate Above +75°C by ..... 6 mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—AD7528, +5V Operation

(V_{DD} = +5V; V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				8			Bits
Relative Accuracy	INL	J,A,S K,B,T L,C,U				±1 ±1/2 ±1/2	LSB
Differential Non-Linearity	DNL	All Grades Guaranteed Monotonic Over Temp.				±1	LSB
Gain Error (Note 2)		J,A,S	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±4 ±6	LSB
		K,B,T	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±2 ±4	
		L,C,U	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±1 ±3	
Gain Temp. Coefficient (Note 2, 3)					±2	±70	ppm/°C
Supply Rejection (Note 4)	PSR	ΔV_{DD} = ±5%	T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.001 0.001	0.02 0.04	%FSR/%
Output Leakage Current (OUTA)		DAC A is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±400	nA
Output Leakage Current (OUTB)		DAC B is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±400	nA
REFERENCE INPUT							
R_{IN} ($V_{REF}A$, $V_{REF}B$)				8	10	15	kΩ
$V_{REF}A$, $V_{REF}B$ Input Resistance Match						±1	%
DYNAMIC PERFORMANCE (Note 4)							
Output Current Settling-Time to 1/2 LSB		DB0-DB7 = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF;	T_A = 25°C T_A = T_{MIN} to T_{MAX}			350 400	ns

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ELECTRICAL CHARACTERISTICS—AD7528, +5V Operation (Continued)

(V_{DD} = +5V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Note 4) (Continued)						
Propagation Delay (from digital input to 90% of final analog output current)		$\overline{DB0}$-$\overline{DB7}$ = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF; T_A = 25°C T_A = T_{MIN} to T_{MAX}			220 270	ns
Digital to Analog Glitch Impulse		For code transition 00000000 to 11111111		60		nV-sec
AC Feedthrough (V_{REF}A to OUTA)		V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB
AC Feedthrough (V_{REF}B to OUTB)		V_{REF}B = ±10V 100kHz Sinewave V_{REF}A = 0V T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB
Channel to Channel Isolation (V_{REF}A to OUTB)		V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V, both DACs loaded with 11111111		-90		dB
Channel to Channel Isolation (V_{REF}B to OUTA)		V_{REF}B = ±10V 100kHz Sinewave V_{REF}A = 0V, both DACs loaded with 11111111		-90		dB
Digital Crosstalk		Measured with code transition 0 to FS		30		nV-sec
Harmonic Distortion	THD	V_{IN} = 6V rms @ 1kHz		-85		dB
ANALOG OUTPUTS (Note 4)						
OUTA Capacitance	C_{OUTA}	DAC latches loaded with 00000000 DAC latches loaded with 11111111			50 120	pF pF
OUTB Capacitance	C_{OUTB}	DAC latches loaded with 00000000 DAC latches loaded with 11111111			50 120	pF pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±1 ±10	µA
Input Capacitance (Note 4)	C_{IN}	$\overline{DB0}$-$\overline{DB7}$ $\overline{WR}$, $\overline{CS}$, DAC A/DAC B			10 15	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH} T_A = 25°C T_A = T_{MIN} to T_{MAX}			1 1	mA
		Digital inputs 0V or V_{DD} T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	µA
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	200 230			ns
Chip Select to Write Hold Time	t_{CH}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	20 30			ns

Note 1: Specifications apply to both DACs in AD7528.
Note 2: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 3: Guaranteed, but not tested.
Note 4: These characteristics are for design guidance only and are not subject to test.

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ELECTRICAL CHARACTERISTICS—AD7528, +5V Operation (Continued)

(V_{DD} = +5V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram) (Continued)						
DAC Select to Write Setup Time	t_{AS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	200 230			ns
DAC Select to Write Hold Time	t_{AH}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	20 30			ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	180 200			ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	110 130			ns
Data Hold Time	t_{DH}		0			ns

ELECTRICAL CHARACTERISTICS—AD7528, +15V Operation

(V_{DD} = +15V; V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				8			Bits
Relative Accuracy	INL	J,A,S K,B,T L,C,U				±1 ±1/2 ±1/2	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temp.				±1	LSB
Gain Error (Note 2)		J,A,S	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±4 ±5	LSB
		K,B,T	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±2 ±3	
		L,C,U	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±1 ±1	
Gain Temp. Coefficient (Note 2, 3)					±2	±35	ppm/°C
Supply Rejection (Note 4)	PSR	ΔV_{DD} = ±5%	T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.001 0.001	0.01 0.02	%FSR/%
Output Leakage Current (OUTA)		DAC A is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
Output Leakage Current (OUTB)		DAC B is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
REFERENCE INPUT							
R_{IN} (V_{REF}A, V_{REF}B)				8	10	15	kΩ
V_{REF}A, V_{REF}B Input Resistance Match						±1	%
DYNAMIC PERFORMANCE (Note 4)							
Output Current Settling-Time to 1/2 LSB		$\overline{DB0}$-$\overline{DB7}$ = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF;	T_A = 25°C T_A = T_{MIN} to T_{MAX}			180 200	ns

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ELECTRICAL CHARACTERISTICS—AD7528, +15V Operation (Continued)

(V_{DD} = +15V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Note 4) (Continued)						
Propagation Delay (from digital input to 90% of final analog output current)		$\overline{DB0}$-$\overline{DB7}$ = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF; T_A = 25°C T_A = T_{MIN} to T_{MAX}			80 100	ns
Digital to Analog Glitch Impulse		For code transition 00000000 to 11111111		125		nV-sec
AC Feedthrough (V_{REF}A to OUTA)		V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB
AC Feedthrough (V_{REF}B to OUTB)		V_{REF}B = ±10V 100kHz Sinewave V_{REF}A = 0V T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB
Channel to Channel Isolation (V_{REF}A to OUTB)		V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V, both DACs loaded with 11111111		-90		dB
Channel to Channel Isolation (V_{REF}B to OUTA)		V_{REF}B = ±10V 100kHz Sinewave V_{REF}A = 0V, both DACs loaded with 11111111		-90		dB
Digital Crosstalk		Measured with code transition 0 to FS		60		nV-sec
Harmonic Distortion	THD	V_{IN} = 6V rms @ 1kHz		-85		dB
ANALOG OUTPUTS (Note 4)						
OUTA Capacitance	C_{OUTA}	DAC latches loaded with 00000000 DAC latches loaded with 11111111			50 120	pF pF
OUTB Capacitance	C_{OUTB}	DAC latches loaded with 00000000 DAC latches loaded with 11111111			50 120	pF pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		13.5			V
Input Low Voltage	V_{IL}				1.5	V
Input Current	I_{IN}	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±1 ±10	μA
Input Capacitance (Note 4)	C_{IN}	$\overline{DB0}$-$\overline{DB7}$ $\overline{WR}$, $\overline{CS}$, DAC A/DAC B			10 15	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH} T_A = 25°C T_A = T_{MIN} to T_{MAX}			1 1	mA
		Digital inputs 0V or V_{DD} T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	μA
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	60 80			ns
Chip Select to Write Hold Time	t_{CH}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	10 15			ns

Note 1: Specifications apply to both DACs in AD7528.
Note 2: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 3: Guaranteed, but not tested.
Note 4: These characteristics are for design guidance only and are not subject to test.

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ELECTRICAL CHARACTERISTICS—AD7528, +15V Operation (Continued)

(V_{DD} = +15V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram) (Continued)						
DAC Select to Write Setup Time	t_{AS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	60 80			ns
DAC Select to Write Hold Time	t_{AH}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	10 15			ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	60 80			ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	30 40			ns
Data Hold Time	t_{DH}		0			ns

ELECTRICAL CHARACTERISTICS—AD7628, +12V to +15V Operation

(V_{DD} = +10.8V to +15.75V; V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				8			Bits
Relative Accuracy	INL					±1/2	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temp.				±1	LSB
Gain Error (Note 2)		T_A = 25°C T_A = T_{MIN} to T_{MAX}				±2 ±3	LSB
Gain Temp. Coefficient (Note 2, 3)					±2	±35	ppm/°C
Supply Rejection (Note 4)	PSR	ΔV_{DD} = ±5%	T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.001 0.001	0.01 0.02	%FSR/%
Output Leakage Current (OUTA)		DAC A is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
Output Leakage Current (OUTB)		DAC B is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
REFERENCE INPUT							
R_{IN} (V_{REF}A, V_{REF}B)				8	10	15	kΩ
V_{REF}A, V_{REF}B Input Resistance Match						±1	%
DYNAMIC PERFORMANCE (Note 4)							
Output Current Settling-Time to 1/2 LSB		DB0-DB7 = 0V to +5V to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF;	T_A = 25°C T_A = T_{MIN} to T_{MAX}			350 400	ns
Digital to Analog Glitch Impulse		For code transition 00000000 to 11111111			125		nV-sec
AC Feedthrough (V_{REF}A to OUTA)	/	V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V	T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB

Note 1: Specifications apply to both DACs in AD7628.
Note 2: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 3: Guaranteed, but not tested.
Note 4: These characteristics are for design guidance only and are not subject to test.

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ELECTRICAL CHARACTERISTICS—AD7628, +12V to +15V Operation (Continued)

(V_{DD} = +10.8V to +15.75V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Note 4) (Continued)						
AC Feedthrough (V_{REF}B to OUTB)		V_{REF}B = ±10V, 100kHz Sinewave, V_{REF}A = 0V; T_A = 25°C / T_A = T_{MIN} to T_{MAX}			-70 / -65	dB
Channel to Channel Isolation (V_{REF}A to OUTB)		V_{REF}A = ±10V 100kHz Sinewave, V_{REF}B = 0V, both DACs loaded with 11111111		-90		dB
Channel to Channel Isolation (V_{REF}B to OUTA)		V_{REF}B = ±10V 100kHz Sinewave, V_{REF}A = 0V, both DACs loaded with 11111111		-90		dB
Digital Crosstalk		Measured with code transition 0 to FS		60		nV-sec
Harmonic Distortion	THD	V_{IN} = 6V rms @ 1kHz		-85		dB
ANALOG OUTPUTS (Note 4)						
OUTA Capacitance	C_{OUTA}	DAC latches loaded with 00000000 / DAC latches loaded with 11111111			25 / 60	pF / pF
OUTB Capacitance	C_{OUTB}	DAC latches loaded with 00000000 / DAC latches loaded with 11111111			25 / 60	pF / pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	T_A = 25°C / T_A = T_{MIN} to T_{MAX}			±1 / ±10	μA
Input Capacitance (Note 4)	C_{IN}	DB0-DB7 / $\overline{WR}$, $\overline{CS}$, DAC A/DAC B			10 / 15	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH}: T_A = 25°C / T_A = T_{MIN} to T_{MAX} K / T_A = T_{MIN} to T_{MAX} B,T			2 / 2 / 2.5	mA
		Digital inputs 0V or V_{DD}: T_A = 25°C / T_A = T_{MIN} to T_{MAX}			100 / 500	μA
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C / T_A = T_{MIN} to T_{MAX} K,B / T_A = T_{MIN} to T_{MAX} T	160 / 160 / 210			ns
Chip Select to Write Hold Time	t_{CH}		10			ns
DAC Select to Write Setup Time	t_{AS}	T_A = 25°C / T_A = T_{MIN} to T_{MAX} K,B / T_A = T_{MIN} to T_{MAX} T	160 / 160 / 210			ns
DAC Select to Write Hold Time	t_{AH}		10			ns
Write Pulse Width	t_{WR}	T_A = 25°C / T_A = T_{MIN} to T_{MAX} K,B / T_A = T_{MIN} to T_{MAX} T	150 / 170 / 210			ns
Data Setup Time	t_{DS}	T_A = 25°C / T_A = T_{MIN} to T_{MAX} K,B / T_A = T_{MIN} to T_{MAX} T	160 / 160 / 210			ns
Data Hold Time	t_{DH}		10			ns

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Interface Logic Information

DAC Selection

Both DAC latches share a common 8-Bit input port. The control input DAC A/DAC B selects which DAC will accept data from the input port.

Mode Selection

The inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC. See Mode Selection Table.

Mode Selection Table

DAC A/DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low state, H = High state, X = Don't care

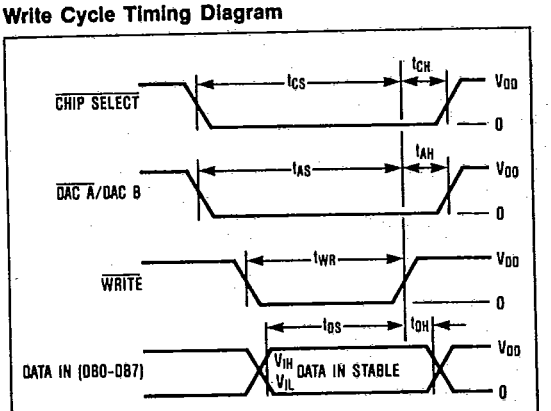
Write Mode

When $\overline{CS}$ and $\overline{WR}$ are both low, the selected DAC is in the write mode. The input latches of the selected DAC are transparent and its analog output responds to the data on the data bit lines DB0–DB7.

Hold Mode

The selected DAC latch retains the data that was present on DB0–DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

Write Cycle Timing Diagram



Note 1: For the AD7528, all input signal rise and fall times are measured from 10% to 90% of V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns; V_{DD} = +15V, $t_r = t_f$ = 40ns.

Note 2: For the AD7628, all input signal rise and fall times are measured from 10% to 90% of +5V. $t_r = t_f$ = 20ns; V_{DD} = +10.8V to +15.75V.

Note 3: Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

Detailed Description

The AD7528/AD7628 contains two identical 8-Bit multiplying digital-to-analog converters (DAC). Each DAC circuit consists of a thin-film R-2R resistor array with CMOS current steering switches. Figure 1 shows a simplified schematic of the DAC. The inverted R-2R ladder divides the voltage or current reference in a binary manner among the eight steering switches. The magnitude of the current appearing at the OUT terminal depends on the number of switches selected, and therefore the output is an analog representation of the digital input. The DAC OUT and analog ground terminals must be maintained at the same potential for proper operation.

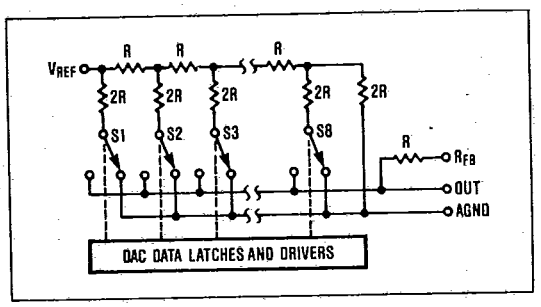


Figure 1. Simplified DAC Schematic

Equivalent-Circuit Analysis

The DAC equivalent-circuit, typical of both DACs, is shown in figure 2. Each DAC shares the analog ground pin 1. When all the digital inputs are high, 255/256 of the reference current flows to OUT A. A small junction leakage current ($I_{LEAKAGE}$), which doubles every 10°C, also flows to the output. The R-2R ladder termination resistor generates a constant 1/256 current which represents 1 LSB of the reference current, I_{REF}. C_{OUT} is the parallel combination of the capacitance associated with the individual NMOS current steering switches. The value of output capacitance is input code dependent and lies in the range 20pF to 30pF. The equivalent output resistance, R_O, also varies with input code in the range 0.8R to 3R, where R is the nominal ladder resistance.

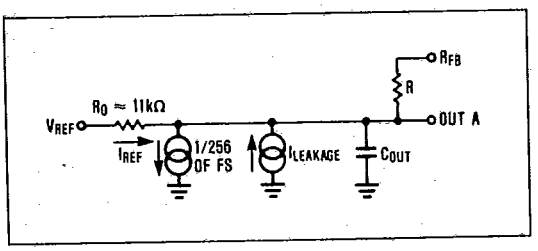


Figure 2. DAC Equivalent Circuit. All Digital Inputs High

CMOS Dual 8-Bit Buffered Multiplying DACs

Circuit Information—Digital Section

The AD7528's digital inputs are TTL compatible when operated with a V_{DD} of +5V (V_{IH} = 2.4V, V_{IL} = 0.8V). Internal level shifters convert from TTL to CMOS logic levels. When V_{IN} is in the region of 1.0 to 3.5 volts, the input buffers operate in their linear region and the quiescent current increases as indicated by the graph in figure 3. Therefore to minimize supply current it is recommended that the digital inputs be as close to the supply rails as possible (V_{DD} and DGND).

The AD7528 may be operated with any supply voltage in the range 5V < V_{DD} < 15V. With V_{DD} = +15V, the input logic levels are CMOS compatible only, i.e. 1.5V and 13.5V.

The AD7628's digital inputs are TTL and CMOS compatible with any supply voltage in the range of +12V to +15V.

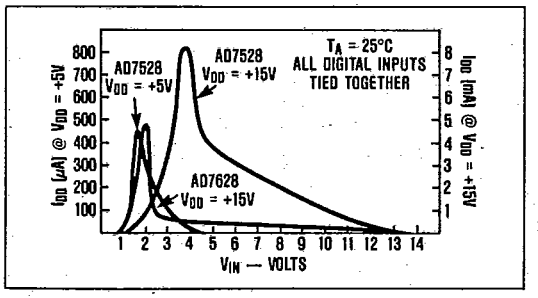
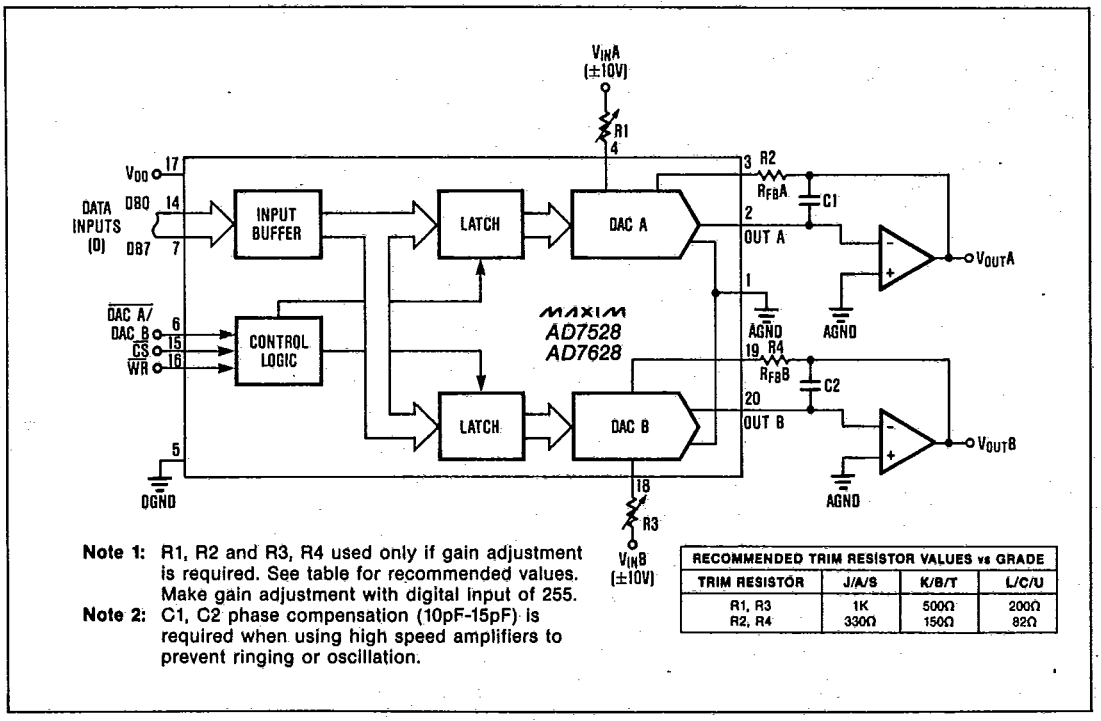


Figure 3. Typical Plots of Supply Current, I_{DD} vs. Logic Input Voltage V_{IN}, for V_{DD} = +5V and +15V



Note 1: R1, R2 and R3, R4 used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.

Note 2: C1, C2 phase compensation (10pF-15pF) is required when using high speed amplifiers to prevent ringing or oscillation.

RECOMMENDED TRIM RESISTOR VALUES vs GRADE			
TRIM RESISTOR	J/A/S	K/B/T	L/C/U
R1, R3	1K	500Ω	200Ω
R2, R4	330Ω	150Ω	82Ω

Figure 4. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication)

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Applications Information

To ensure system performance consistent with the AD7528/AD7628 specifications, careful attention must be given to the following points:

1. General Ground Management:

   AC or transient voltages between the AD7528/AD7628 AGND and DGND can cause noise injection into the analog output. Therefore, whenever possible, the analog and digital ground pins should be tied together at the AD7528/AD7628.

2. Output Amplifier Offset:

   CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The result is a code-dependent differential nonlinearity term at the amplifier output which depends on the amplifier's offset voltage, V_{OS}. The offset dependent nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier offset voltage should be no more than 1/10 LSB over the operating temperature range.

3. High Frequency Considerations:

   The combination of DAC output capacitance and the amplifier's feedback resistance adds a pole to the open-loop response which can cause ringing or oscillation in severe cases. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

4. Dynamic Performance:

   The dynamic performance of the two DACs in the AD7528/AD7628 depends on the gain and phase characteristics of the output amplifiers, together with the stray capacitance contributed by the PC layout, and the power supply decoupling components. A 0.1μF decoupling capacitor is recommended between V_{DD} and DGND.

5. Circuit Layout Suggestions:

   Analog and digital ground traces should be routed between the package pins to reduce coupling between the digital inputs and the analog output. Analog ground traces should also be placed between pins 17-18, 18-19, 3-4, and 4-5 to minimize reference feedthrough to the output in multiplying applications.

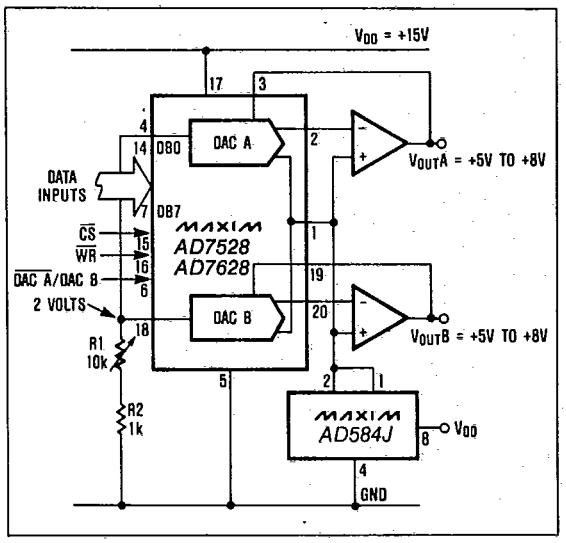


Figure 5. AD7528/AD7628 Single Supply Operation

Single Supply Operation

The AD7528/AD7628 R-2R ladder termination resistors are internally connected to AGND. This arrangement is particularly convenient for single supply operation because AGND may be biased at any voltage between V_{DD} and DGND. Figure 5 shows a circuit which provides dual +5V to +8V analog outputs by biasing AGND 5V above DGND. The two DAC reference inputs are tied together and a reference input voltage is obtained without a buffer amplifier by making use of the stable matched impedances of the DAC A and DAC B reference inputs. Current flows through the two DAC A and DAC B reference inputs. Current flows through the two DAC R-2R ladders into R1, and R1 is adjusted until $V_{REF}A$ and $V_{REF}B$ inputs are at +2V. DAC codes from 00000000 to 11111111 adjust the analog output voltages from +5V to +8V in 11.7mV steps.

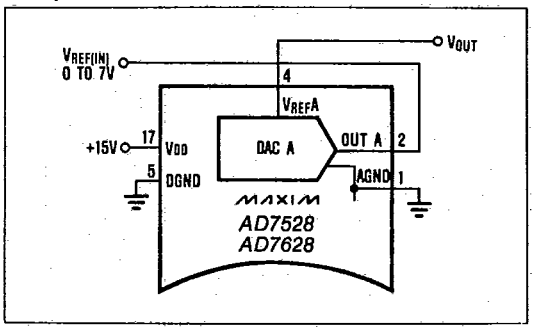


Figure 6. AD7528/AD7628 in Single Supply, Voltage Switching Mode

Figure 6 shows one DAC of the AD7528/AD7628 connected in the voltage switching mode which uses a positive reference voltage. This configuration is useful in that V_{OUT} is the same polarity as V_{IN} allowing single supply operation. However, to maintain linearity, V_{IN} must be limited to approximately +7V (V_{DD} = +15V), and the output must be buffered or loaded with a high impedance. In the voltage switching mode, the output resistance is independent of the digital input code and is typically 10kΩ.

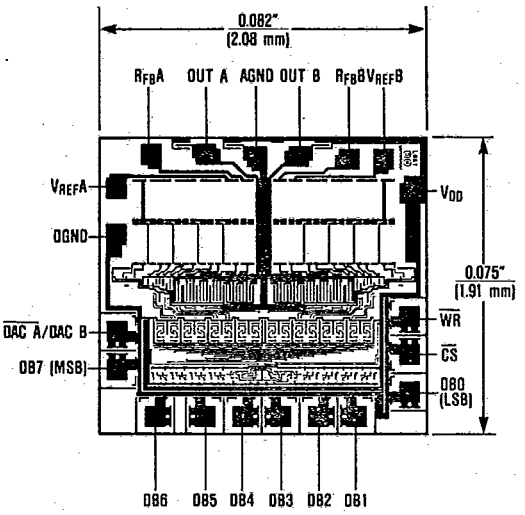
CMOS Dual 8-Bit Buffered Multiplying DACs

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7528SD	-55°C to +125°C	Ceramic	±1 LSB
AD7528TD	-55°C to +125°C	Ceramic	±½ LSB
AD7528UD	-55°C to +125°C	Ceramic	±½ LSB
AD7528SQ	-55°C to +125°C	CERDIP**	±1 LSB
AD7528TQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7528UQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7628KN	0°C to +70°C	Plastic DIP	±½ LSB
AD7628KCWP	0°C to +70°C	Small Outline	±½ LSB
AD7628KC/D	0°C to +70°C	Dice	±½ LSB
AD7628BQ	-25°C to +85°C	CERDIP	±½ LSB
AD7628TQ	-55°C to +125°C	CERDIP	±½ LSB

* *All devices — 20 lead packages*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*

Chip Topography



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