1.1 Scope.

This specification covers the detail requirements for a monolithic 10-bit CMOS multiplying digital-to-analog converter.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
–1	AD7533S(X)/883B
–2	AD7533T(X)/883B
–3	AD7533U(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = 25°C unless otherwise noted)

V_{DD} to GND	−0.3V, +17V
R_{FB} to GND	±25V
V_{REF} to GND	±25V
Digital Input Voltage Range	−0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2)	−0.3V to V_{DD}
Power Dissipation	
Up to +50°C	1000mW
Derates above +50°C	10mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: "Pin numbers refer to DIP package ONLY"

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-16 and E-20A
θ_{JA} = 120°C/W for Q-16 and E-20A

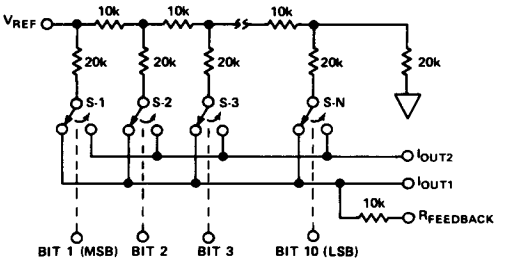
AD7533—SPECIFICATIONS

Table 1.

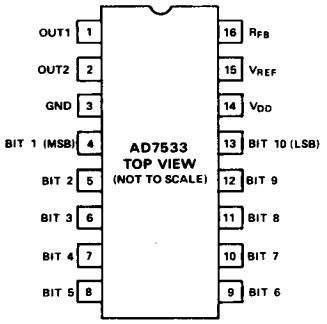
Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Resolution	RES	–1, 2, 3	10					Bits
Relative Accuracy	RA	–1	2	2	2			± LSB max
		–2	1	2	1	1		
		–3	1/2	2	1/2	1/2		
Gain Error[2]	AE	–1, 2, 3	15	14	15			± LSB max
Gain Tempco	TC_{AE}	–1, 2, 3	10					± ppm/°C max
Power Supply Rejection	PSRR	–1, 2, 3	0.008	0.005	0.008		Digital Inputs = V_{IH}; V_{DD} = 14V to +17V	± %/% max
Output Leakage Current I_{OUT1} (Pin 1)	I_{OL}	–1, 2, 3	200	50	200		Digital Inputs = V_{IL}; (V_{REF} = +10V)	± nA max
I_{OUT2} (Pin 2)	I_{OL}	–1, 2, 3	200	50	200		Digital Inputs = V_{IH}; (V_{REF} = +10V)	± nA max
Output Current Settling Time	t_{SL}	–1, 2, 3	800				To ± 1/2LSB; R_{OUT1} = 100Ω C_{OUT1} = 13pF; Digital Inputs = V_{IH} to V_{IL} or V_{IL} to V_{IH}	ns max
Feedthrough Error[3]	FT	–1, 2, 3	15				Digital Inputs = V_{IL}; V_{REF} = ± 10V; 100kHz Sinewave	± mV p-p max
Reference Input Resistance	R_{IN}	–1, 2, 3	5	5	5			kΩ min
			20	20	20			kΩ max
Input High Voltage	V_{IH}	–1, 2, 3	2.4	2.4	2.4			V min
Input Low Voltage	V_{IL}	–1, 2, 3	0.8	0.8	0.8			V max
Input Leakage Current	I_{IN}	–1, 2, 3	1	1	1		V_{IN} = 0V or V_{DD}	± μA max
Input Capacitance	C_{IN}	–1, 2, 3	5					pF max
Output Capacitance Pin 1	C_{OUT1}	–1, 2, 3	100				Digital Input = V_{IH}	pF max
Pin 2	C_{OUT2}	–1, 2, 3	35				Digital Input = V_{IH}	pF max
Pin 1	C_{OUT1}	–1, 2, 3	35				Digital Input = V_{IL}	pF max
Pin 2	C_{OUT2}	–1, 2, 3	100				Digital Input = V_{IL}	pF max
Supply Current	I_{DD}	–1, 2, 3	2	2	2		Digital Inputs = V_{IL} or V_{IH}	mA max

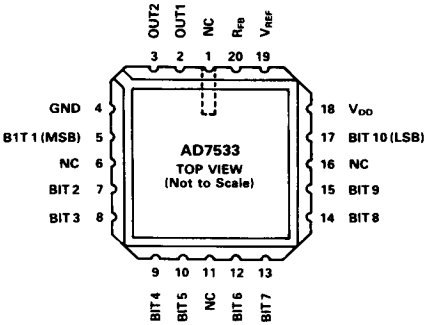
NOTES
[1] V_{DD} = +15V; V_{OUT1} = V_{OUT2} = 0V; V_{REF} = +10V unless otherwise stated.
[2] Measured using internal feedback resistor and includes effect of leakage current and gain TC.
[3] Feedthrough error can be reduced by connecting the lid of the ceramic package to ground.

3.2.1 Functional Block Diagram and Terminal Assignments.



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)



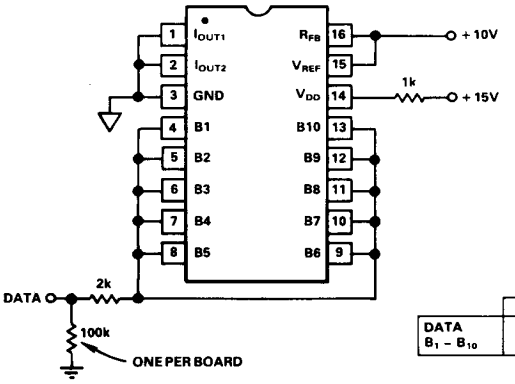


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



	STATIC	DYNAMIC	
DATA $B_1 - B_{10}$	+15V	V_{IL} = GND / V_{IH} = +15V	@ 60Hz