

1.1 Scope.

This specification covers the detail requirement for a complete 14-bit, monolithic CMOS, D/A converter which is loaded by a single 14-bit wide word using standard chip select and memory write logic. Double buffering, which is optional using LDAC, allows simultaneous update in a system containing multiple AD7538s.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD7538TQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

Package	Description
Q-24	24-Pin Cerdip

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to DGND	 -0.3 V dc to +17 V dc
V_{SS} to AGND	 -15 V dc to +0.3 V dc
AGND to DGND	 -0.3 V dc to $V_{DD} + 0.3$ V dc
Digital Input Voltage to DGND	 -0.3 V dc to $V_{DD} + 0.3$ V dc
V_{PIN3} to DGND	 -0.3 V dc to $V_{DD} + 0.3$ V dc
V_{REF} to AGND	 ± 25 V dc
V_{RFB} to AGND	 ± 25 V dc
Power Dissipation	 1000 mW
Storage Temperature Range	 -65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10 sec)	 $+300^\circ\text{C}$
Thermal Resistance, Junction-to-Case (θ_{JC})	 See MIL-M-38510, Appendix C

1.4 Recommended Operating Conditions.

Supply Voltage	
V_{DD}	 +11.4 V dc to +15.75 V dc
V_{SS}	 -200 mV dc to -500 mV dc
Ambient Operating Temperature Range, T_A	 -55°C to $+125^\circ\text{C}$

AD7538—SPECIFICATIONS

Table 1.

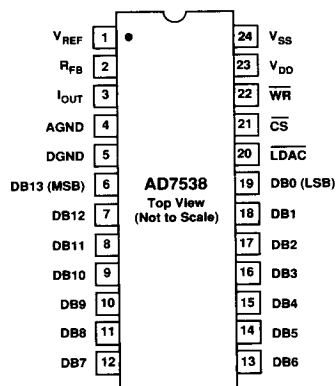
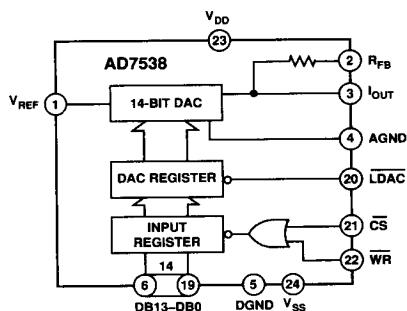
Test	Symbol	Device	Limits		Sub Groups	Condition ¹ ($-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ unless otherwise noted)	Unit
Resolution	RES	-1	14		1, 2, 3	Guaranteed Minimum Resolution	Bits
Relative Accuracy	RA	-1		+1.0	1, 2, 3	Guaranteed Monotonic to 14 Bits	LSB
Differential Nonlinearity	DNL	-1		± 1.0	1, 2, 3		LSB
Full-Scale Error	A_E	-1		± 4	1	DAC Registers Loaded with All 1s	LSB
				± 6	2, 3		
Output Leakage Current	I_{OUT}	-1		± 5	1	All Digital Inputs = 0 V, $V_{SS} = -300\text{ mV}$	nA
				± 20	2, 3		
				± 5	1	All Digital Inputs = 0 V, $V_{SS} = 0\text{ V}$	nA
				± 150	2, 3		
Reference Input Resistance	R_{IN}	-1	3.5	10	1, 2, 3	$V_{DD} = +15.75\text{ V}$	k Ω
Digital Input High Voltage	V_{IH}	-1	2.4		7, 8		V
Digital Input Low Voltage	V_{IL}	-1		0.8	7, 8		V
Input Current	I_{IN}	-1		± 1	1	$V_{IN} = 0\text{ V to } V_{DD}$	μA
				± 10	2, 3		
Input Capacitance	C_{IN}	-1		7	4		pF
Power Supply Current	I_{DD}	-1		4	1, 2, 3	All Digital Inputs = V_{IL} or V_{IH}	mA
				500	1, 2, 3	All Digital Inputs = 0 V or V_{DD}	μA
Output Current Settling Time to 0.003% FSR ²	t_S	-1		1.5	4	I_{OUT} Load = 100 Ω , $C_{EXT} = 13\text{ pF}$, DAC Register Alternately Loaded with All 1s and All 0s, $T_A = +25^{\circ}\text{C}$	μs
Power Supply Rejection ²	PSR	-1		± 0.01	1	Delta $V_{DD} = \pm 5.0\%$	%/%
				± 0.02	2, 3		
Output Capacitance ²	C_{OUT}	-1		260	4	DAC Register Loaded with All 1s	pF
				130	1, 4	DAC Register Loaded with All 0s	pF
$\overline{\text{CS}}$ to $\overline{\text{WR}}$ Setup Time	t_1		0		9, 10, 11	All Input Signal Rise and Fall Times Measured from 10% to 90% of 5.0 V. t_r to $t_f = 20\text{ ns}$. See Figure 1.	ns
$\overline{\text{CS}}$ to $\overline{\text{WR}}$ Hold Time	t_2		0		9, 10, 11		ns
LDAC Pulse Width	t_3		170		9		ns
			240		10, 11		
Write Pulse Width	t_4		170		9		ns
			240		10, 11		
Data Setup Time	t_5		140		9		ns
			180		10, 11		
Data Hold Time	t_6		20		9		ns
			30		10, 11		

NOTES

¹ $V_{DD} = +11.4\text{ V dc to } +15.75\text{ V dc}$, $V_{REF} = +10\text{ V dc}$, $V_{PIN3} = V_{PIN4} = 0\text{ V dc}$, $V_{SS} = 0\text{ V or } -300\text{ mV}$. Parts are guaranteed over this supply range. Individual tests are performed with known worst case supply conditions. Unless otherwise stated tests are done with $V_{DD} = +15.75\text{ V}$ and $+11.4\text{ V}$; $V_{SS} = -0.3\text{ V}$.

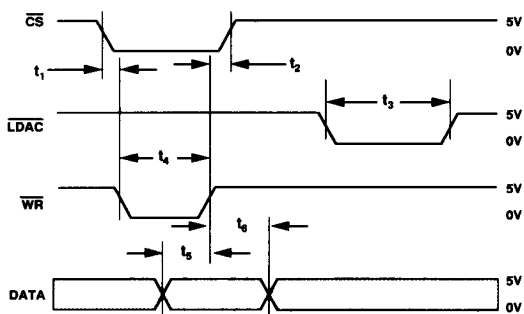
²Guaranteed if not tested.

3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).



NOTES:

1. ALL INPUT SIGNAL RISE AND FALL TIMES ARE MEASURED FROM 10% TO 90% OF +5.0V, $t_r = t_f = 20\text{ns}$.

2. TIMING MEASUREMENT REFERENCE LEVELS ARE: $\frac{V_{IH} + V_{IL}}{2}$

3. IF $\overline{LDAC}$ IS ACTIVATED PRIOR TO THE RISING EDGE OF $\overline{WR}$, THEN IT MUST STAY LOW FOR t_3 OR LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 1. Timing Diagram

Table 2. Truth Table

$\overline{CS}$	$\overline{LDAC}$	$\overline{WR}$	Operation
0	1	0	Load Input Register
1	0	X	Load DAC Register from Input Register
0	0	0	Input and DAC Registers are Transparent
1	1	1	No Operation
X	1	1	No Operation

1 = High Voltage Level

0 = Low Voltage Level

X = Irrelevant