



CMOS 12-Bit Buffered Multiplying DAC

AD7545

1.1 Scope.

T-51-09-12

This specification covers the detail requirements for a monolithic CMOS multiplying digital-to-analog converter with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit systems. The AD7545 can be used with any supply voltage from +5V to +15V.

1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification is as follows:

Device	Part Number ¹
-1	AD7545S(X)/883B
-2	AD7545T(X)/883B
-3	AD7545U(X)/883B
-4	AD7545GU(X)/883B

NOTE:

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{REF} to GND		-0.3, +17V
Digital Input Voltage to DGND		-0.3V to V_{DD}
V_{RFB} , V_{REF} to DGND		$\pm 25\text{V}$
V_{PIN1} to DGND		-0.3V to V_{DD}
AGND to DGND		-0.3V, V_{DD}
Power Dissipation		
Up to $+75^\circ\text{C}$		450mW
Derates above $+75^\circ\text{C}$		6mW/ $^\circ\text{C}$
Operating Temperature Range		-55°C to $+125^\circ\text{C}$
Storage Temperature Range		-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)		$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-20 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-20 and E-20A

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Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +15V$	Units
Resolution	RES	-1, 2, 3, 4	12					Bits
Relative Accuracy	RA	-1	2	2	2			$\pm$ LSB max
		-2	1	2	1	1		
		-3, 4	1/2	2	1/2	1/2		
Differential Nonlinearity	DNL	-1	4	4	4		10-Bit Monotonic T_{min} to T_{max}	$\pm$ LSB max
		-2, 3, 4	1	4	1	1	12-Bit Monotonic T_{min} to T_{max}	
Gain Error ²	AE	-1	25	25	25		DAC Register Loaded with 1111 1111 1111.	$\pm$ LSB max
		-2	15	25	15	15		
		-3	10	25	10	10		
		-4	7	25	7	6		
Gain Tempco	TC_{AE}	-1, 2, 3, 4	10					$\pm$ ppm/ $^{\circ}C$ max
Power Supply Rejection	PSRR	-1, 2, 3, 4	0.02	0.01	0.02		$\Delta V_{DD} = \pm 5\%$	$\pm$ %/% max
Output Leakage Current Pin 1	OUT1	-1, 2, 3, 4	200	10	200		DB0-DB11 = 0V; $\overline{WR}, \overline{CS} = 0V$	$\pm$ nA max
Output Current Settling Time	t_{SL}	-1, 2, 3, 4	2				To $\pm 1/2$ LSB; OUT1 Load = 100 Ω , DAC Output Measured from Falling Edge of $\overline{WR}$. $\overline{CS} = 0V$. $\overline{CS} = 0V$.	μs max
Feedthrough Error ³	FT	-1, 2, 3, 4	10				$V_{REF} = \pm 10V$, 10kHz Sinewave	mV p-p max
Reference Input Resistance Pin 19 to Ground	R_{IN}	-1, 2, 3, 4	7	7	7			k Ω min
			25	25	25			k Ω max
Digital Input High Voltage	V_{IH}	-1, 2, 3, 4	13.5	13.5	13.5			V min
Digital Input Low Voltage	V_{IL}	-1, 2, 3, 4	1.5	1.5	1.5			V max
Digital Input Leakage Current	I_{IN}	-1, 2, 3, 4	10	1	10		$V_{IN} = 0V$ or V_{DD}	$\pm$ μA max
Digital Input Capacitance DB0-DB11 $\overline{WR}, \overline{CS}$	C_{IN}	-1, 2, 3, 4	5				$V_{IN} = 0$	pF max
			20					
Output Capacitance	C_{OUT1}	-1, 2, 3, 4	70				DB0-DB11 = 0V, $\overline{WR}, \overline{CS} = 0V$	pF max
			200				DB0-DB11 = V_{DD} , $\overline{WR}, \overline{CS} = 0V$	
Chip Select to Write Setup Time ⁴	t_{CS}	-1, 2, 3, 4	200					ns min
Chip Select to Write Hold Time ⁴	t_{CH}	-1, 2, 3, 4	0					ns min
Write Pulse Width ⁴	t_{WR}	-1, 2, 3, 4	240				$t_{CS} \geq t_{WR}, t_{CH} \geq 0$	ns min
Data Setup Time ⁴	t_{DS}	-1, 2, 3, 4	120					ns min
Data Hold Time ⁴	t_{DH}	-1, 2, 3, 4	30					ns min
Supply Current from V_{DD}	I_{DD}	-1, 2, 3, 4	2	2	2		All Digital Inputs V_{IL} or V_{IH} .	mA max
			500	100	500		All Digital Inputs 0 or V_{DD} .	μA max

NOTES

¹ $V_{OUT1} = 0V$; $V_{REF} = +10V$, AGND = DGND unless otherwise stated.²Measured using internal feedback resistor and includes effect of 5ppm max gain TC.³Feedthrough error can be reduced by connecting the metal lid to ground.⁴Timing per Figure 1.

Table 1.

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Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +5V$	Units
Resolution	RES	-1, 2, 3, 4	12					Bits
Relative Accuracy	RA	-1	2	2	2			± LSB max
		-2	1	2	1	1		
		-3, 4	1/2	2	1/2	1/2		
Differential Nonlinearity	DNL	-1	4	4	4		10-Bit Monotonic T_{min} to T_{max}	± LSB max
		-2, 3, 4	1	4	1	1	12-Bit Monotonic T_{min} to T_{max}	
Gain Error ²	AE	-1	20	20	20		DAC Register Loaded with 1111 1111 1111.	± LSB max
		-2	10	20	10	10		
		-3	6	20	6	5		
		-4	2	20	2	1		
Gain Tempco	TC_{AE}	-1, 2, 3, 4	5					± ppm/°C max
Power Supply Rejection	PSRR	-1, 2, 3, 4	0.03	0.015	0.03		$\Delta V_{DD} = \pm 5\%$	± %/% max
Output Leakage Current Pin 1	OUT1	-1, 2, 3, 4	200	10	200		$DB0-DB11 = 0V$; $\overline{WR}, \overline{CS} = 0V$	± nA max
Output Current Settling Time	t_{SL}	-1, 2, 3, 4	2				To ± 1/2LSB; OUT1 Load = 100Ω, DAC Output Measured from Falling Edge of $\overline{WR}$. $\overline{CS} = 0V$.	μs max
Feedthrough Error ³	FT	-1, 2, 3, 4	10				$V_{REF} = \pm 10V$, 10kHz Sinewave	mV p-p max
Reference Input Resistance Pin 19 to Ground	R_{IN}	-1, 2, 3, 4	7	7	7			kΩ min
			25	25	25			kΩ max
Digital Input High Voltage	V_{IH}	-1, 2, 3, 4	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	-1, 2, 3, 4	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	-1, 2, 3, 4	10	1	10		$V_{IN} = 0V$ or V_{DD}	± μA max
Digital Input Capacitance $DB0-DB11$ $\overline{WR}, \overline{CS}$	C_{IN}	-1, 2, 3, 4	5				$V_{IN} = 0$	pF max
		-1, 2, 3, 4	20				$V_{IN} = 0$	pF max
Output Capacitance	C_{OUT1}	-1, 2, 3, 4	70				$DB0-DB11 = 0V$, $\overline{WR}, \overline{CS} = 0V$	pF max
			200				$DB0-DB11 = V_{DD}$, $\overline{WR}, \overline{CS} = 0V$	
Chip Select to Write Setup Time ⁴	t_{CS}	-1, 2, 3, 4	380					ns min
Chip Select to Write Hold Time ⁴	t_{CH}	-1, 2, 3, 4	0					ns min
Write Pulse Width ⁴	t_{WR}	-1, 2, 3, 4	400				$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	ns min
Data Setup Time ⁴	t_{DS}	-1, 2, 3, 4	210					ns min
Data Hold Time ⁴	t_{DH}	-1, 2, 3, 4	30					ns min
Supply Current from V_{DD}	I_{DD}	-1, 2, 3, 4	2	2	2		All Digital Inputs V_{IL} or V_{IH} .	mA max
			500	100	500		All Digital Inputs 0 or V_{DD} .	μA max

NOTES

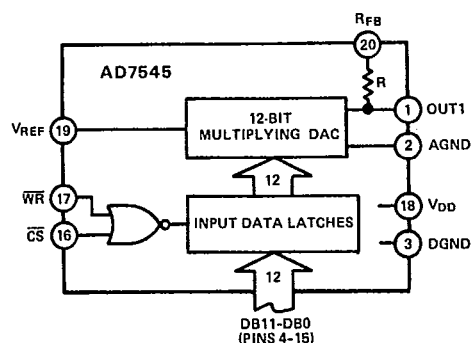
¹ $V_{OUT1} = 0V$; $V_{REF} = +10V$, AGND = DGND unless otherwise stated.²Measured using internal feedback resistor and includes effect of 5ppm max gain TC.³Feedthrough error can be reduced by connecting the metal lid to ground.⁴Timing per Figure 1.

Table 2.

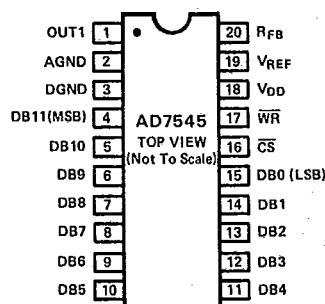
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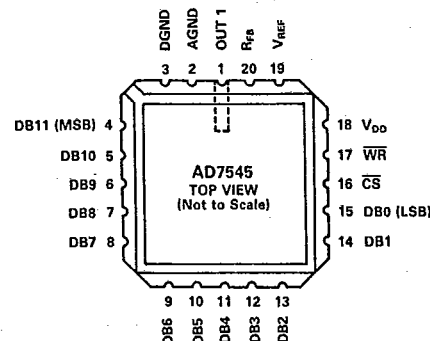
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (Cerdip)



E Package (LCC)



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

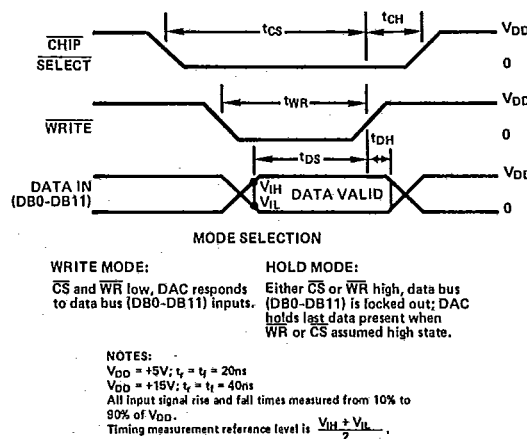
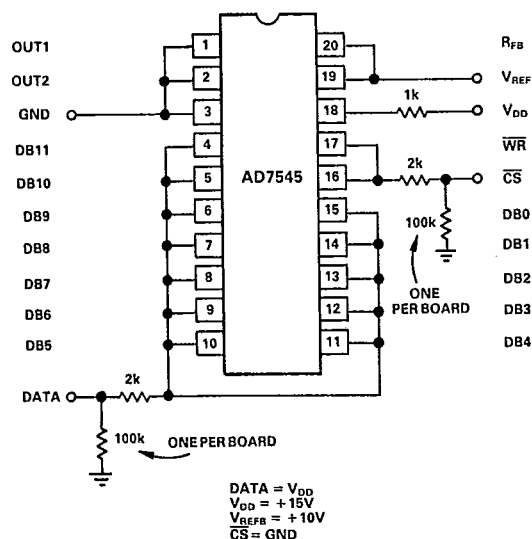


Figure 1. Write Cycle Timing Diagram

MODE SELECTION	
WRITE MODE: $\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0-DB11) inputs.	HOLD MODE: Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0-DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:
 $V_{DD} = +5V$; $t_r = t_f = 20ns$
 $V_{DD} = +15V$; $t_r = t_f = 40ns$
 All input signal rise and fall times measured from 10% to 90% of V_{DD} .
 Timing measurement reference level is $V_{IH} + V_{IL}/2$.

Table 3. Write Mode Selection

REV. C