1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 8-bit input/output port. This consists of an 8-bit sampling analog-to-digital converter, an 8-bit digital-to-analog converter with output amplifier, and a common reference and 8-bit parallel data bus.

1.2 Part Number.

The complete part numbers per Tables 1 and 2 of this specification are as follows:

Device	Part Number
−1	AD7569S(X)/883B
−2	AD7569T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C)

V_{DD} to AGND (DAC or ADC) ..... −0.3 V, +7 V
V_{DD} to DGND ..... −0.3 V, +7 V
V_{DD} to V_{SS} ..... −0.3 V, +14 V
AGND (DAC or ADC) to DGND ..... −0.3 V, V_{DD} +0.3 V
AGND (DAC) to AGND (ADC) ..... ±5 V
Logic Voltage to DGND ..... −0.3 V, V_{DD} +0.3 V
CLK Input Voltage to DGND ..... −0.3 V, V_{DD} +0.3 V
V_{OUT} to AGND (DAC) ..... V_{SS} −0.3 V, V_{DD} +0.3 V
V_{IN} to AGND (ADC) ..... V_{SS} −0.3 V, V_{DD} +0.3 V
Power Dissipation (to +75°C) ..... 450 mW
Derates above +75°C ..... 6 mW/°C
Operating Temperature Range ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-24 and E-28A
θ_{JA} = 120°C/W for Q-24 and E-28A

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Table 1.

DAC Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]/Comments	Units
Resolution	RES	−1, 2	8				Minimum Resolution for Which No Missing Codes Are Guaranteed.	Bits
Total Unadjusted Error	TUE	−1, 2	3					±LSB typ
Relative Accuracy	INL	−1	1	1	1			±LSB max
		−2	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	−1	1	1	1			±LSB max
		−2	3/4	1	3/4	3/4		
Unipolar Offset Error		−1	2.5	2	2.5			±LSB max
		−2	2	2	2	1.5		
Bipolar Zero Offset Error		−1	2.5	2	2.5			±LSB max
		−2	2	2	2	1.5		
Full-Scale Error[2]		−1	4	2	4			LSB max
		−2	3	2	3	1		
ΔFull Scale/ΔV_{DD}		−1, 2		1/2			V_{OUT} = 2.5 V; ΔV_{DD} = ±5%	±LSB max
ΔFull Scale/ΔV_{SS}		−1, 2		1/2			V_{OUT} = −2.5 V; ΔV_{SS} = ±5%	±LSB max
Signal-to-Noise Ratio	SNR	−1	44	44	44		V_{OUT} = 20 kHz Sine; $f_{SAMPLING}$ = 400 kHz	dB min
		−2	46	46	46			
Total Harmonic Distortion	THD	−1, 2	48	48	48		V_{OUT} = 20 kHz Sine; $f_{SAMPLING}$ = 400 kHz	dB max
Intermodulation Distortion	IMD	−1, 2	55				fa = 18.4 kHz; fb = 14.5 kHz $f_{SAMPLING}$ = 400 kHz	dB typ
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8	0.8			V max
Digital Input High Voltage	V_{IH}	−1, 2	2.4	2.4	2.4			V min
Unipolar Analog Output Voltage		−1, 2	0 to +1.25/2.5					
Bipolar Analog Output Voltage		−1, 2	±1.25/±2.5					
Input Leakage Current	I_{IN}	−1, 2	10	10	10		V_{IN} = 0 to V_{DD}	±μA max
Input Capacitance	C_{IN}	−1, 2	10					pF max
Supply Current from V_{DD}	I_{DD}	−1, 2	13	13	13			mA max
Supply Current from V_{SS}	I_{SS}	−1, 2	4	4	4			mA max

NOTES
[1]V_{DD} = +5 V ± 5%, V_{SS} = RANGE = $AGND_{DAC}$ = $AGND_{ADC}$ = DGND = 0 V, f_{CLK} = 5 MHz
[2]Includes internal voltage reference error and is calculated after offset error has been adjusted out.

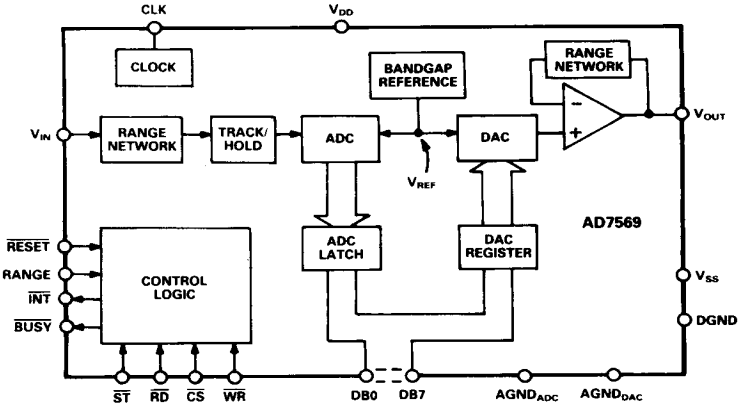
Table 2.

ADC Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]/Comments	Units
Resolution	RES	−1, 2	8				Minimum Resolution for Which No Missing Codes Are Guaranteed.	Bits
Total Unadjusted Error	TUE	−1, 2	4					±LSB typ
Relative Accuracy	INL	−1	1	1	1			±LSB max
		−2	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	−1	1	1	1			±LSB max
		−2	3/4	1	3/4	3/4		
Unipolar Offset Error		−1	3	2	3			±LSB max
		−2	2.5	2	2.5	1.5		
Bipolar Zero Offset Error		−1	4	3	4			±LSB max
		−2	3.5	3	3.5	2.5		
Full-Scale Error[2]		−1, 2	−7.5	−7.5	−7.5			LSB max
			+2	+2	+2			
ΔFull Scale/ΔV_{DD}		−1, 2		0.5			V_{IN} = +2.5 V; ΔV_{DD} = ±5%	±LSB max
ΔFull Scale/ΔV_{SS}		−1, 2		0.5			V_{IN} = −2.5 V; ΔV_{SS} = ±5%	±LSB max
Signal-to-Noise Ratio	SNR	−1	44	44	44	44	V_{IN} = 100 kHz Sine; $f_{SAMPLING}$ = 400 kHz	dB min
		−2	45	44	45	44		
Total Harmonic Distortion	THD	−1, 2	48	48	48		V_{IN} = 100 kHz Sine; $f_{SAMPLING}$ = 400 kHz	dB max
Intermodulation Distortion	IMD	−1, 2	60				fa = 99 kHz; fb = 96.7 kHz $f_{SAMPLING}$ = 400 kHz	dB typ
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8	0.8			V max
Digital Input High Voltage	V_{IH}	−1, 2	2.4	2.4	2.4			V min
Unipolar Analog Input Voltage	V_{IN_U}	−1, 2	0 to 1.25/+2.5				V_{DD} = +5 V; V_{SS} = 0 V	V
Bipolar Analog Input Voltage	V_{IN_B}	−1, 2	±1.25/±2.5				V_{DD} = +5 V; V_{SS} = −5 V	V
Input Current	I_{IN}	−1, 2	300	300	300			±μA max
Input Capacitance	C_{IN}	−1, 2	10					pF max
Input Leakage Current	I_{IL}	−1, 2	10	10	10			±μA max
CLK Input Current (High Level)	I_{INH}	−1, 2	40	40	40		V_{IN} = V_{DD}	μA max
CLK Input Current (Low Level)	I_{INL}	−1, 2	−1.6	−1.6	−1.6		V_{IN} = 0 V	mA max
Digital Output Low Voltage	V_{OL}	−1, 2	0.4	0.4	0.4			V max
Digital Output High Voltage	V_{OH}	−1, 2	4.0	4.0	4.0			V min
Floating State Leakage Current	I_{OUT}	−1, 2	10	10	10			±μA max

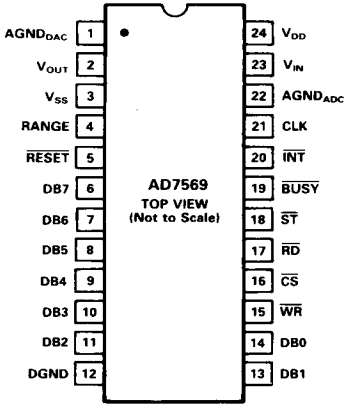
Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]/Comments	Units
Floating State Output Capacitance	C_{OUT}	−1, 2	10					pF max
Conversion Time (External Clock)	t_{CONV}	−1, 2	2.0	2.0	2.0		f_{CLK} = 5.0 MHz	µs max

NOTES
[1]V_{DD} = +5 V ± 5%, V_{SS} = RANGE = $AGND_{DAC}$ = $AGND_{ADC}$ = DGND = 0 V, f_{CLK} = 5 MHz
[2]Includes internal voltage reference error and is calculated after offset error has been adjusted out.

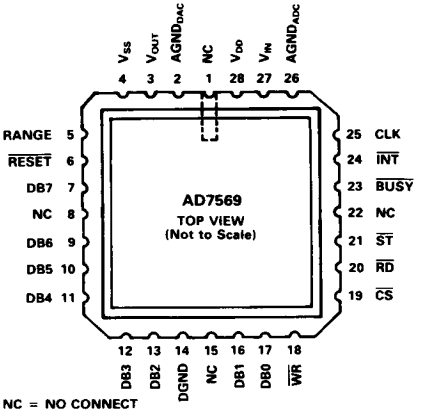
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (DIP)



E Package (LCC)

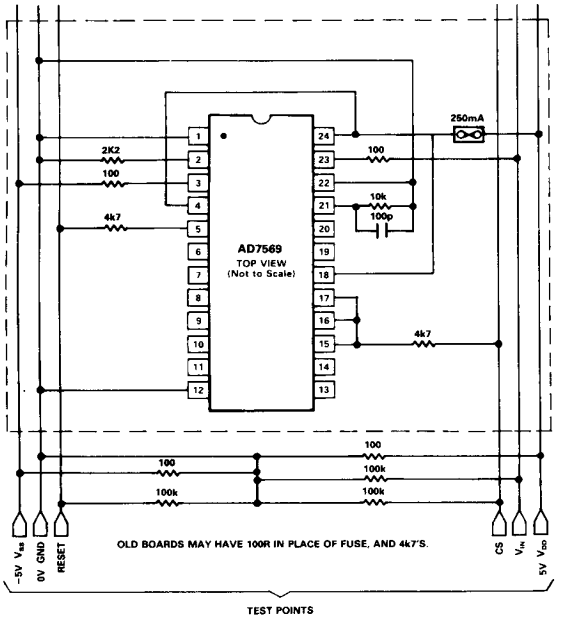


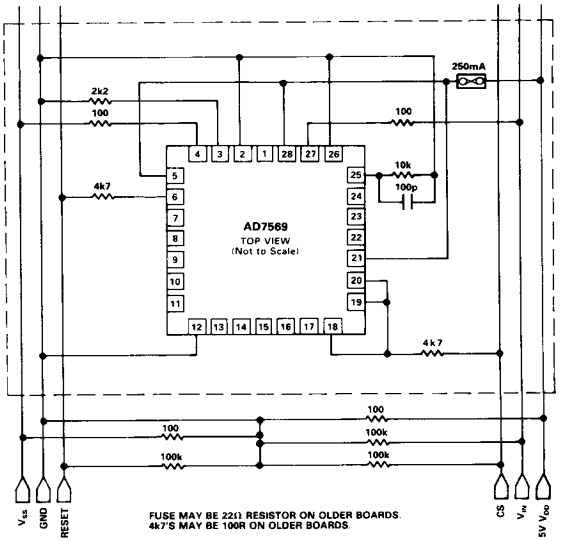
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



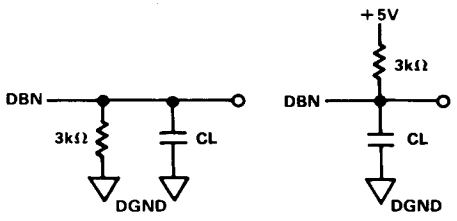


AD7569 Edge Connections

TIMING[1]

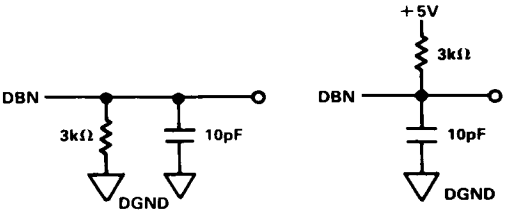
Test	Symbol	Device	Design Limit T_{min} to T_{max}	Units
	DAC Timing			
$\overline{WR}$ Pulse Width	t_1	−1, 2	90	ns min
$\overline{CS}$, A/B to $\overline{WRS}$ Setup Time	t_2	−1, 2	0	ns min
$\overline{CS}$, A/B to $\overline{WR}$ Hold Time	t_3	−1, 2	0	ns min
Data Valid to $\overline{WR}$ Setup Time	t_4	−1, 2	80	ns min
Data Valid to $\overline{WR}$ Hold Time	t_5	−1, 2	10	ns min
	ADC Timing			
$\overline{ST}$ Pulse Width	t_6	−1, 2	50	ns min
$\overline{ST}$ to $\overline{BUSY}$ Delay	t_7	−1, 2	150	ns max
$\overline{BUSY}$ to $\overline{INT}$ Delay	t_8	−1, 2	30	ns max
$\overline{BUSY}$ to $\overline{CS}$ Delay	t_9	−1, 2	0	ns min
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{10}	−1, 2	0	ns min
$\overline{RD}$ Pulse Width. Determined by t_{13}.	t_{11}	−1, 2	90	ns min
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{12}	−1, 2	0	ns min
Data Access Time after $\overline{RD}$; C_L = 20 pF	t_{13}[2]	−1, 2	90	ns max
Data Access Time after $\overline{RD}$; C_L = 100 pF			135	ns max
Bus Relinquish Time after $\overline{RD}$	t_{14}[3]	−1, 2	10	ns min
			85	ns max
$\overline{RD}$ to $\overline{INT}$ Delay	t_{15}	−1, 2	85	ns max
$\overline{RD}$ to $\overline{BUSY}$ Delay	t_{16}	−1, 2	160	ns max
Data Valid Time after $\overline{BUSY}$; C_L = 20 pF	t_{17}[2]	−1, 2	90	ns max
Data Valid Time after $\overline{BUSY}$; C_L = 100 pF			135	ns max

NOTES
[1]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[2]t_{13} and t_{17} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[3]t_{14} is defined as the time required for the data line to change 0.5 V when loaded with the circuit of Figure 2.



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Bus Relinquish Time Test