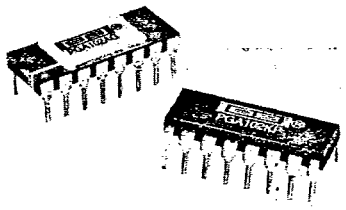
BURR-BROWN®



PGA102

AVAILABLE IN DIE FORM

Digitally-Controlled Programmable-Gain/Fast-Settling OPERATIONAL AMPLIFIER

FEATURES

- DIGITALLY-PROGRAMMABLE GAINS, X1, X10, X100
- LOW GAIN ERROR, 0.01%, max
- LOW GAIN DRIFT, 5ppm/°C, max
- LOW NONLINEARITY, 0.003%, max, 14-BIT
- FAST SETTLING, 2.8μs, 0.01%, typ
- THREE INDEPENDENT INPUT CHANNELS WITH SEPARATE GAIN ADJUSTMENT
- LOW COST
- SMALL 16-PIN DIP PACKAGE, CERAMIC AND PLASTIC

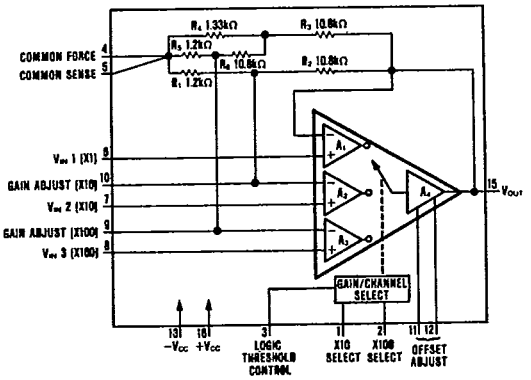
APPLICATIONS

- DATA ACQUISITION AMPLIFIER
- AUTORANGING AMPLIFIER UNDER COMPUTER CONTROL
- SUPER-ACCURACY, LOW COST, FIXED GAIN BLOCK
- TEST EQUIPMENT GAIN CONTROL
- PORTABLE INSTRUMENT GAIN SELECTION
- DATA LOGGING RANGING CONTROL
- 3-CHANNEL MULTIPLEXER

DESCRIPTION

The PGA102 is a precision digitally-programmable gain block. Its monolithic design permits low cost and high reliability. The user can select one of three gains (1, 10, 100), two of which are independently adjustable. The logic section has high input impedance and functions without a separate supply. Precision laser-trimmed offset and gains permit use without external adjustments. High performance thin-film resistors with excellent temperature tracking assure low gain drift and excellent stability.

The fast 2.8μsec settling makes the PGA102 ideal for rapid channel scanning in data acquisition systems. Also the high accuracy is very beneficial in test equipment and instrumentation applications where programmable or fixed gain is required.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C, ±V_{CC} = 15VDC unless otherwise specified.

PARAMETER	CONDITIONS	PGA102AG MIN	PGA102AG TYP	PGA102AG MAX	PGA102BG/SG MIN	PGA102BG/SG TYP	PGA102BG/SG MAX	PGA102KP MIN	PGA102KP TYP	PGA102KP MAX	UNITS
GAIN											
Inaccuracy[1]	R_L = 2kΩ, G = 1		±0.007	±0.02		±0.003	±0.01		•	•	%
	G = 10		±0.015	±0.03		±0.01	±0.02		•	±0.05	%
	G = 100		±0.02	±0.05		±0.015	±0.025		•	±0.06	%
vs Temperature	G = 1		±0.4	±5		•	•		•	•	ppm/°C
	G = 10		±2	±7		•	•		•	•	ppm/°C
	G = 100		±7	±20		•	•		±9	•	ppm/°C
Nonlinearity	R_L = 2kΩ, G = 1		0.001	0.003		•	•		•	•	% of FS
	G = 10		0.002	0.005		•	•		•	•	% of FS
	G = 100		0.003	0.01		•	•		•	•	% of FS
RATED OUTPUT											
Voltage	R_L = 2kΩ	±10	±12.5		•	•		•	•		V
Current	V_{OUT} = 10V	±5	±10		•	•		•	•		mA
Short Circuit Current		±10	±25		•	•		•	•		mA
Output Resistance			0.01			•			•		Ω
Load Capacitance	For stable operation		2000			•			•		pF
INPUT OFFSET VOLTAGE											
Initial[2]	G = 1		±200	±500		±100	±250		•	±1500	µV
	G = 10		±70	±200		±50	±100		•	±600	µV
	G = 100		±70	±200		±50	±100		•	±600	µV
vs Temperature	G = 1		±5	±20		•	•		±7	±50	µV/°C
	G = 10		±1	±7		•	•		±3	±10	µV/°C
	G = 100		±0.5	±3		•	•		±2	±7	µV/°C
vs Supply Voltage	±5 < V_{CC} < ±18V										
	G = 1		±30	±70		•	•		•	•	µV/V
	G = 10		±8	±30		•	•		•	•	µV/V
	G = 100		±8	±30		•	•		•	•	µV/V
INPUT BIAS CURRENT											
Initial	T_A = +25°C		±20	±50		•	•		•	•	nA
Over Temperature	$T_{A\ MIN}$ to $T_{A\ MAX}$		±25	±60		•	•		•	•	nA
ANALOG INPUT CHARACTERISTICS											
Voltage Range	Linear operation	±10	±12		•	•		•	•		V
Resistance			7×10^9			•			•		Ω
Capacitance			4			•			•		pF
INPUT NOISE											
Voltage Noise	f_B = 0.1Hz to 10Hz										
	G = 1		4.5			•			•		µV p-p
	G = 10		1.5			•			•		µV p-p
	G = 100		0.6			•			•		µV p-p
Voltage Noise Density	f_O = 1Hz, G = 1		490			•			•		nV/√Hz
	G = 10		178			•			•		nV/√Hz
	G = 100		83			•			•		nV/√Hz
	f_O = 10Hz, G = 1		155			•			•		nV/√Hz
	G = 10		56			•			•		nV/√Hz
	G = 100		20			•			•		nV/√Hz
	f_O = 100Hz, G = 1		93			•			•		nV/√Hz
	G = 100		31			•			•		nV/√Hz
	G = 100		18			•			•		nV/√Hz
	f_O = 1kHz, G = 1		79			•			•		nV/√Hz
	G = 10		31			•			•		nV/√Hz
	G = 100		18			•			•		nV/√Hz
Current Noise	f_B = 0.1Hz to 10Hz		76			•			•		pA p-p
Current Noise Density	f_O = 1Hz		8.8			•			•		pA/√Hz
	f_O = 10Hz		2.8			•			•		pA/√Hz
	f_O = 100Hz		0.99			•			•		pA/√Hz
	f_O = 1kHz		0.43			•			•		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Power Supply ..... ±18V
Input Voltage Range: Analog ..... ±V_{CC}
Digital ..... ($V_{PIN\ 3}$ − 5.6V) to +V_{CC}
Storage Temperature Range: G Package ..... −65°C to +150°C
P Package ..... −55°C to +125°C
Lead Temperature (soldering 10 seconds) ..... +300°C
Output Short-Circuit Duration ..... Continuous to Common
Junction Temperature: G Package ..... +175°C
P Package ..... +110°C

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	PGA102AG MIN	PGA102AG TYP	PGA102AG MAX	PGA102BG/SG MIN	PGA102BG/SG TYP	PGA102BG/SG MAX	PGA102KP MIN	PGA102KP TYP	PGA102KP MAX	UNITS
DYNAMIC RESPONSE											
±3dB Bandwidth	Small signal, G = 1		1500			•			•		kHz
	G = 10		750			•			•		kHz
	G = 100		250			•			•		kHz
	G = 1000		160			•			•		kHz
Full Power Bandwidth	V_{OUT} = ±10V, R_L = 2kΩ										
Slew Rate	V_{OUT} = ±10V step, R_L = 2kΩ	6	9		•	•		•	•		V/µs
Settling Time (0.1%)	V_{OUT} = 10V step, G = 1		1.6			•			•		µs
	G = 10		2.2			•			•		µs
	G = 100		5.2			•			•		µs
Settling Time (0.01%)	V_{OUT} = 10V step, G = 1		2.8			•			•		µs
	G = 10		2.8			•			•		µs
	G = 100		8.2			•			•		µs
Overload Recovery Time, 0.1%	50% overdrive, G = 1 (see Performance Curve)		2.5								µs
CROSSTALK											
DC	±10V to both Off channels		−155			•			•		dB
60Hz	±10V to both Off channels		−144			•			•		dB
DIGITAL INPUT CHARACTERISTICS											
Input "Low" Threshold	V_{IL}[3] on pin 1 or 2			VLTC+0.8		•			•		V
Input "Low" Current				1		•			•		µA
Input "High" Threshold	V_{IH}[3] on pin 1 or 2	VLTC+2		1	•	•		•	•		V
Input "High" Current			0.1	1		•			•		µA
Logic Threshold Control	VLTC on pin 3	$-V_{CC}$		V_{CC} − 4	•	•		•	•		V
Switching Time[4]	Between channels		1			•			•		µs
POWER SUPPLY											
Rated Voltage			±15			•			•		VDC
Voltage Range		±5		±18	•	•		•	•		VDC
Quiescent Current	V_{OUT} = 0V		±2.4	±3.3		•			•		mA
	No external load, V_{OUT} = ±10V			±5.3							mA
TEMPERATURE RANGE											
Specification, KP grade	$T_{A\ MIN}$ to $T_{A\ MAX}$							0		+70	°C
AG and BG grades		−25		+85	•		•			•	°C
SG grade					−55		+125				°C
Operating		−55		+125	•		•	−25		+85	°C
Storage		−65		+150	•		•	−55		+125	°C
Thermal Resistance	θ_{JA}		100			•			•		°C/W

* Specification same as AG grade.

NOTES: (1) Gain inaccuracy is the percent error between the actual and ideal gain selected. It may be externally adjusted to zero for gains of 10 and 100. (2) Offset voltage can be adjusted for any one channel. Adjustment affects temperature drift by approximately ±0.3µV/°C for each 100µV of offset adjusted. (3) Voltage on the logic threshold control pin, VLTC, adjusts the threshold for "Low" and "High" logic levels. (4) Total time to settle equals switching time plus settling time of the newly selected gain.

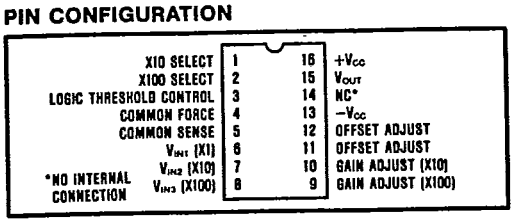
BURN-IN OPTION

Burn-in screening is an option available for the PGA102. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

PIN CONFIGURATION



ORDERING INFORMATION

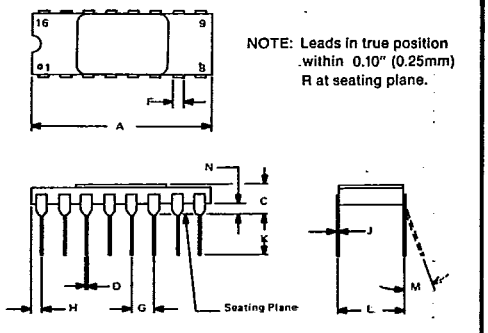
Model	Package	Temperature Range
PGA102AG	Ceramic DIP	-25°C to +85°C
PGA102BG	Ceramic DIP	-25°C to +85°C
PGA102SG	Ceramic DIP	-55°C to +125°C
PGA102KP	Plastic DIP	0°C to +70°C

BURN-IN SCREENING OPTION
See text for details.

Model	Package	Burn-In Temp. (160h)[1]
PGA102AG-BI	Ceramic DIP	+125°C
PGA102BG-BI	Ceramic DIP	+125°C
PGA102SG-BI	Ceramic DIP	+125°C
PGA102KP-BI	Plastic DIP	+85°C

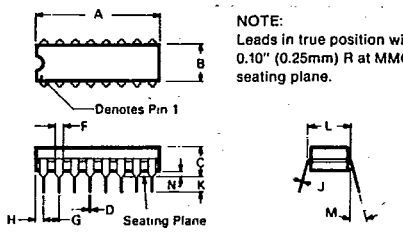
NOTE: Or equivalent combination. See text.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	–	10°	– –	10°
N	.025	.060	0.64	1.52

EPOXY DUAL-IN-LINE

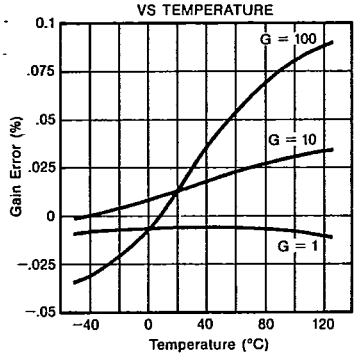


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.760	.885	19.30	22.48
B	.220	.280	5.59	7.11
C		.200		5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.008	.015	0.20	0.38
K	.100	– –	2.54	– –
L	.300 BASIC		7.62 BASIC	
M	– –	15°	– –	15°
N	.020	.050	0.51	1.27

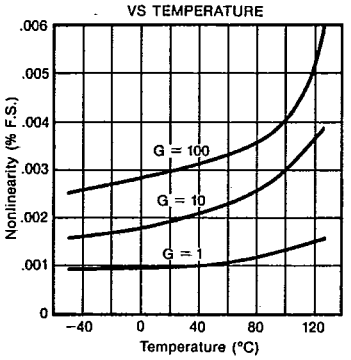
TYPICAL PERFORMANCE CURVES

T_A = 25°C, $\pm V_{CC}$ = 15VDC unless otherwise noted.

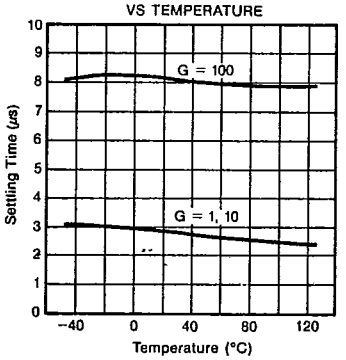
GAIN ERROR VS TEMPERATURE



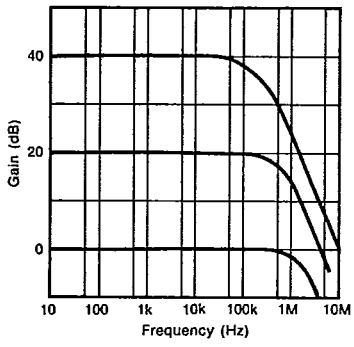
NONLINEARITY VS TEMPERATURE



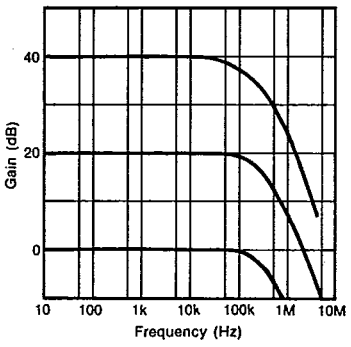
SETTLING TIME VS TEMPERATURE



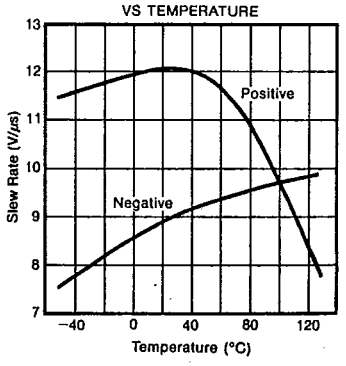
SMALL SIGNAL FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



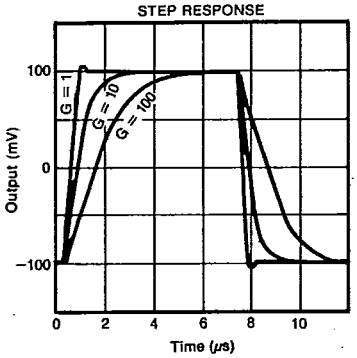
SLEW RATE VS TEMPERATURE



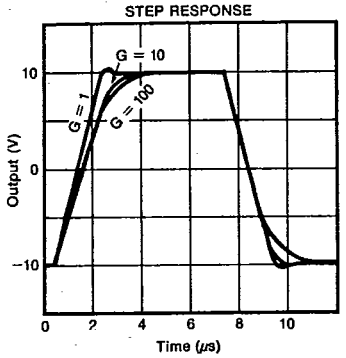
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = 25°C$, $\pm V_{CC} = 15VDC$ unless otherwise noted.

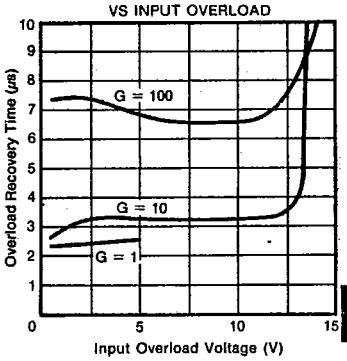
SMALL SIGNAL STEP RESPONSE



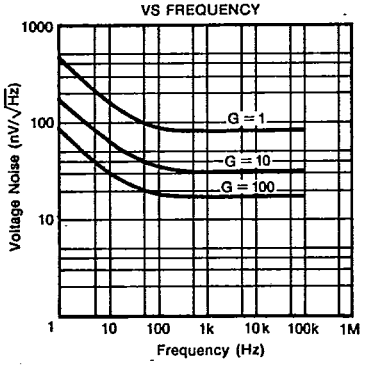
LARGE SIGNAL STEP RESPONSE



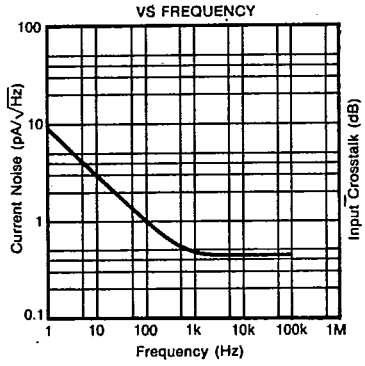
OVERLOAD RECOVERY VS INPUT OVERLOAD



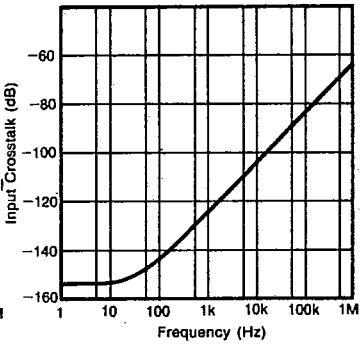
INPUT VOLTAGE NOISE VS FREQUENCY



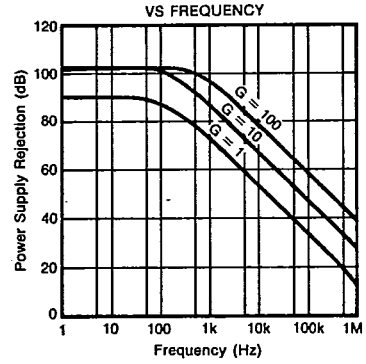
INPUT CURRENT NOISE VS FREQUENCY



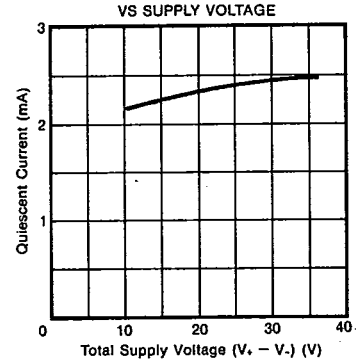
INPUT CROSSTALK VS FREQUENCY



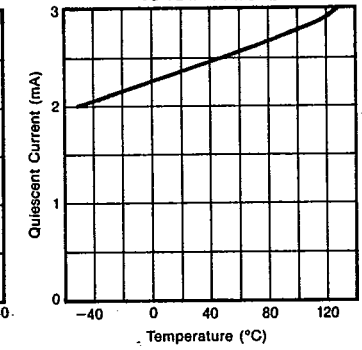
POWER SUPPLY REJECTION VS FREQUENCY



QUIESCENT CURRENT VS SUPPLY VOLTAGE



QUIESCENT CURRENT VS TEMPERATURE



THEORY OF OPERATION

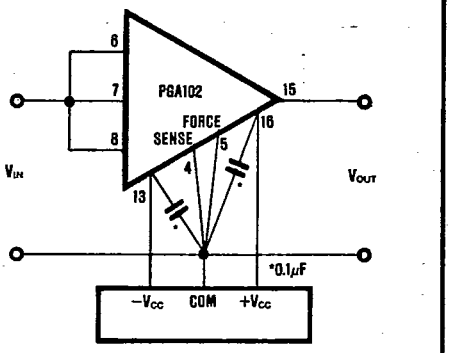
The PGA102 is a self-contained programmable-gain amplifier with digitally selectable gains of 1, 10, and 100.

A block diagram of the PGA102 is shown on the first page of this data sheet. The circuit contains three sections: (1) 3-channel switchable-input operational amplifier, (2) precision thin-film resistor network (R_1–R_6), and (3) gain/channel select digital circuit.

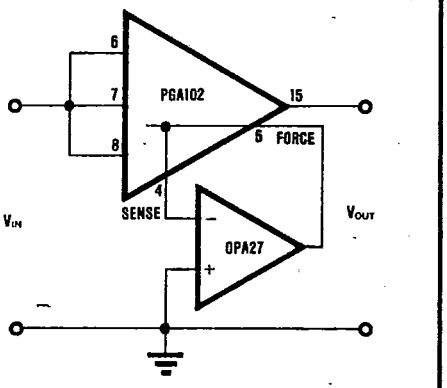
Under control of the channel select circuitry, only one input stage (A_1, A_2, or A_3) is active at any time. The selected input stage steers input signals (V_{IN1}, V_{IN2}, or V_{IN3}) to the output amplifier (A_4). At this time the unselected input stages are turned off by deactivation of their internal bias circuitry. Three different precision gains are produced by closing the feedback loop through the selected input stage. This unique feature of having each channel set to a specific gain allows the user more flexibility in applications. Low gain drift is achieved by the excellent tracking of the thin-film gain set resistors. The "trip point" on select pins 1 and 2 for changing channels, and hence gain, is set by the logic threshold control voltage on pin 3.

INSTALLATION AND OPERATING INSTRUCTIONS

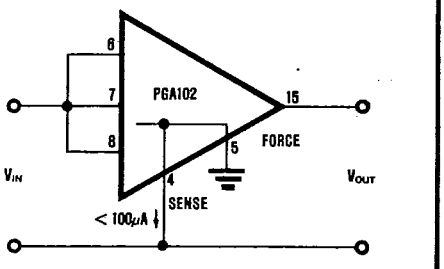
Figure 1 shows proper power supply and signal connections. The supplies should be decoupled with 0.1μF capacitors as close to the package as possible. To avoid gain errors, connect ground as indicated, being sure to minimize ground resistance. The PGA102 has a separate ground force and ground sense which virtually eliminate gain errors due to resistance in the common line. The gain error results from any resistance added in series with the internal junction of R_1, R_4, and R_5. Internally, wire bond resistance of 0.2Ω can cause a 0.02% error for gain of 10 and 0.2% error for gain of 100. By minimizing the current in the sense line, specified performance is achievable.



STAR CONNECTION, GAIN INACCURACY of < 0.1%
(a)



SEE APPLICATION FIGURE 14
(b)



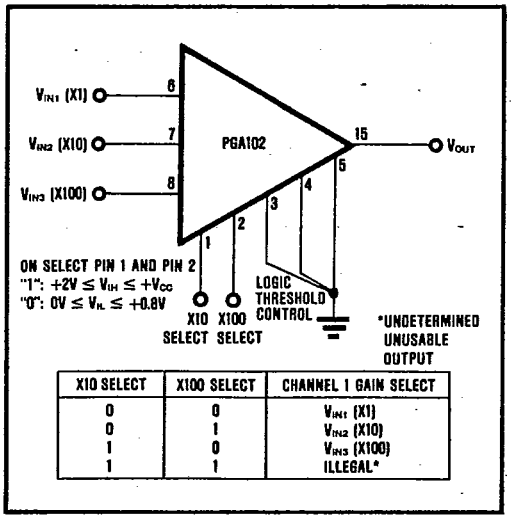
SEE APPLICATION FIGURES 9 AND 10
(c)

(b) AND (c) ELIMINATE GAIN ERRORS DUE TO RESISTANCE OF THE INTERNAL WIRE BOND (INACCURACY < 0.05%).

FIGURE 1. Power Supply and Signal Connections.

GAIN/CHANNEL SELECTION

Gain is chosen by digitally manipulating the voltage level on the X10 and X100 select pins as shown in Figure 2. The table in Figure 2 shows how to select a specific channel which has a gain of 1, 10, or 100. In this circuit, the logic threshold control has been grounded to give compatibility with TTL levels. However, this threshold can be set anywhere between $[-V_{CC} + 4V]$ and $[+V_{CC} - 2.6V]$ for compatibility with other logic such as CMOS.



X10 SELECT	X100 SELECT	CHANNEL 1 GAIN SELECT
0	0	V_{IN1} (X1)
0	1	V_{IN2} (X10)
1	0	V_{IN3} (X100)
1	1	ILLEGAL*

FIGURE 2. Channel Selection for Ground-Referenced Logic Threshold (TTL-compatible).

In general, the logic state is determined by the voltage on pin 1 or pin 2 relative to the threshold control voltage on pin 3. The input high (V_{IH}) and low (V_{IL}) voltages to switch states are shown below:

Logic one, "1": $(V_{LTC} + 2V) < V_{IH} < +V_{CC}$

Logic zero, "0": $(V_{LTC} - 5.6) < V_{IL} < (V_{LTC} + 0.8V)$

An external decoder and latch on the select lines may be added for operation in computer-controlled analog input/output systems.

OPTIONAL OFFSET ADJUSTMENT

The input offset voltage is laser trimmed and will not require user adjustment for most applications. However, pins 11 and 12 may be used to adjust the offset of the

active channel to zero as shown in Figure 3. This also affects the inactive channels (all offsets move as the potentiometer is adjusted). By compromising, the user can adjust for the average offset of all three channels using one potentiometer; or a compromise for just the X10 and X100 channels can be made, considering the unity gain channel's offset is insignificant for high-level inputs.

Figure 4 shows another approach to offset adjustment. An inexpensive CMOS switch (4016) may be used to independently connect the wipers of three potentiometers to $-V_{CC}$. Therefore, R_1, R_2, and R_3 adjust the offset of channels 1, 2, and 3 respectively.

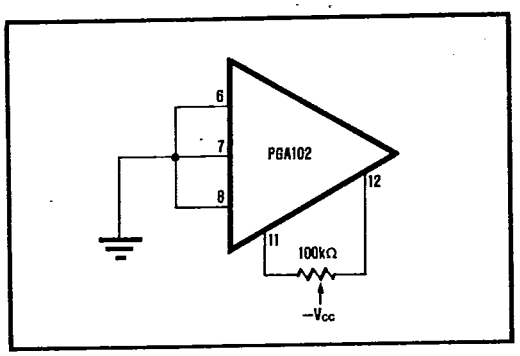


FIGURE 3. Offset Adjustment.

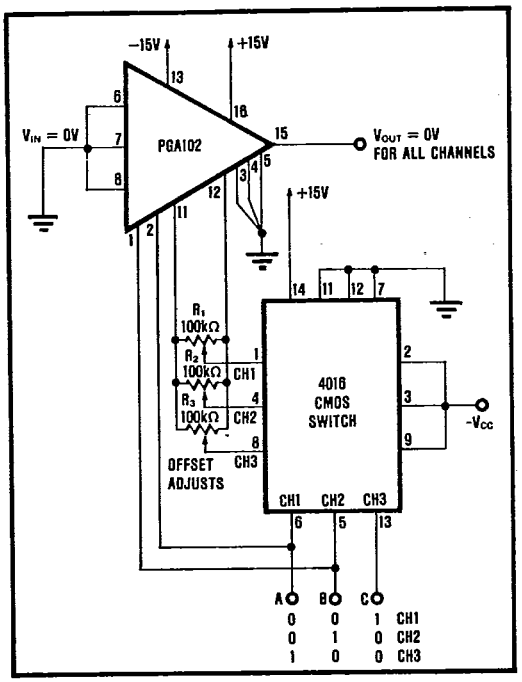


FIGURE 4. Independent Offset Adjustment of Channels 1, 2, and 3.

OPTIONAL GAIN ADJUSTMENT

The initial gain accuracy has been internally laser trimmed to high precision, but can be adjusted. Figure 5 shows independent fine-gain adjustment of channels 2 and 3. This involves either paralleling the internal input resistors for gain up or the internal feedback resistors for gain down. External resistors R_2, R_3, R_5, and R_6 are chosen to trade off range and resolution. Channel 1's gain cannot be adjusted due to the internal zero feedback resistance.

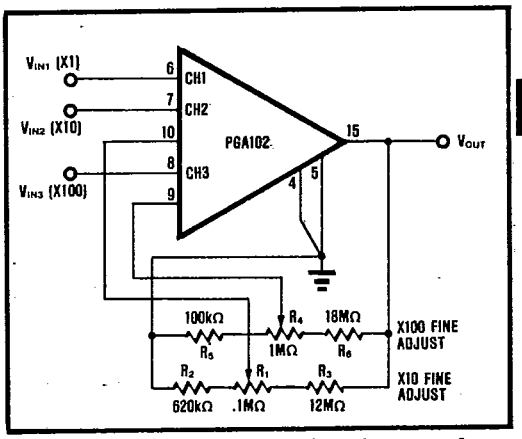


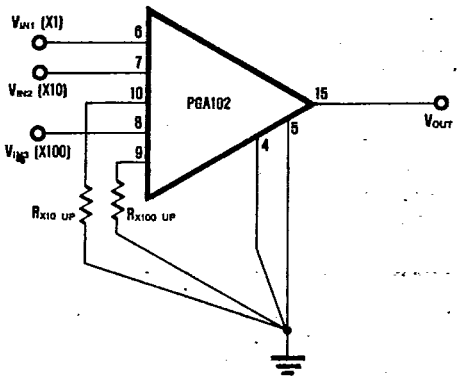
FIGURE 5. Independent Fine Gain Adjustment of Channels 2 and 3.

For applications requiring gains other than 1, 10, or 100, the PGA102 can be gained up (Figure 6) or down (Figure 7). It is important to realize that the temperature drift of the external gain adjustment resistors will affect the total gain drift. This becomes more predominant as the gain is changed further from the factory-set specification. For example, with small adjustments (20% or so), a 30ppm/°C external resistor will add 6ppm/°C to the 10ppm/°C internal resistor ratio tracking. For large adjustment (50% or so), the effect becomes larger. The best that can be achieved is 25ppm/°C (the TCR of one internal resistor) when the external resistor has 0ppm/°C. Also when adjusting the X10 channel, keep the gain above 5 to assure frequency stability.

LAYOUT CONSIDERATIONS

Proper attention to layout is necessary to achieve the specified performance of the PG102. Major goals are to reduce crosstalk, noise pickup, noise coupled from the power supply, and gain errors.

Be certain to separate the runs for analog and digital grounds to avoid coupling of digital transients. To reduce gain errors, connect analog grounds with a ground plane or a low resistance star configuration. Properly using the PGA102 ground force and sense (see Figure 1) assures the best performance, especially in high gains.

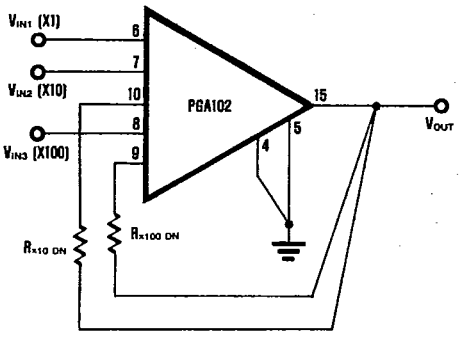


$$R_{X10\ UP} \approx \frac{10.8k\Omega}{G_{X10\ UP} - 10}$$

$$R_{X100\ UP} \approx \frac{108k\Omega}{G_{X100\ UP} - 100}$$

Example:
$R_{X10\ UP} \approx 1.08k\Omega$ and $R_{X100\ UP} \approx 1.08k\Omega$
Gives gains of 1, 20, 200

FIGURE 6. Gain Up Control.



$$R_{X10\ DN} \approx -\left(\frac{97.2k\Omega}{G_{X10\ DN} - 10} + 10.8k\Omega\right)$$

$$R_{X100\ DN} \approx 100\left(\frac{108k\Omega}{100 - G_{X100\ DN}} - 1.09k\Omega\right)$$

Example:
$R_{X10\ DN} \approx 8.64k\Omega$ and $R_{X100\ DN} \approx 107k\Omega$
Gives gains of 1, 5, 50

FIGURE 7. Gain Down Control.

CROSSTALK

Crosstalk expresses the signal feedthrough from an OFF channel that appears at the active input. It is expressed in dB, which translates to a percent of the input signal applied to the OFF channel. Crosstalk increases with increasing frequency (see Typical Performance Curve). Best performance is achieved by keeping input lines short and band limiting if possible.

SETTLING TIME

The PGA102 is designed for applications requiring fast settling. Settling time is the time required, after the onset of a step input signal, for the output voltage to settle and remain within a specified error band around the final value. It is very important because it limits maximum channel scanning or throughput rate in multiplexed systems. Since the error increases with source resistance, keep sources < 10kΩ for best results.

INPUT OVERLOAD RECOVERY

Another important parameter in data acquisition systems is overload recovery, especially when high gain is selected. The PGA102's fast recovery limits delays in capturing input signals in the presence of large transients. Best results are obtained by clamping input overvoltages to less than 13V (see Typical Performance Curve).

TYPICAL APPLICATIONS

The PGA102 is ideal for auto-gain-ranging systems with many multiplexed input channels that must be scanned quickly. Its high gain accuracy and low temperature drift permit application where computer error correction is not available. In other cases, the PGA102 provides an inexpensive precision fixed gain block requiring no precision external components. An external decoder and latch allow the user flexibility to configure the system as desired. Figures 8 through 15 show application circuits.

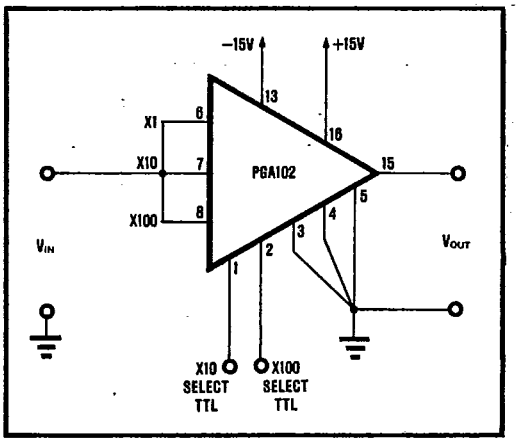


FIGURE 8. Fast Settling Programmable-Gain Amplifier (Gain = 1, 10, 100).

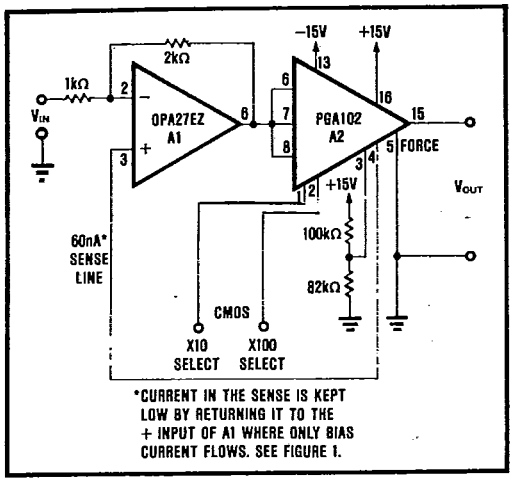


FIGURE 9. Fast-Settling Programmable-Gain Amplifier (Gain = 2, 20, 200).

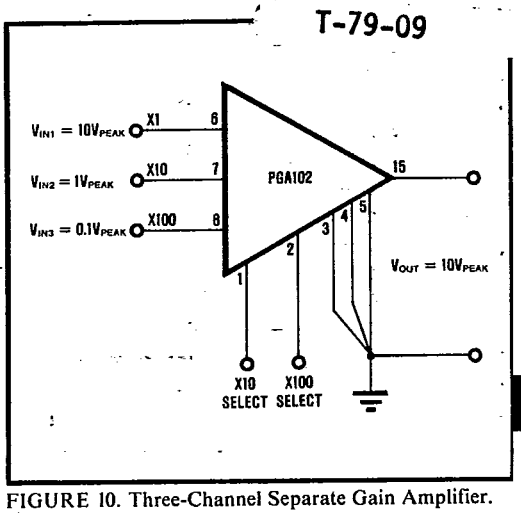


FIGURE 10. Three-Channel Separate Gain Amplifier.

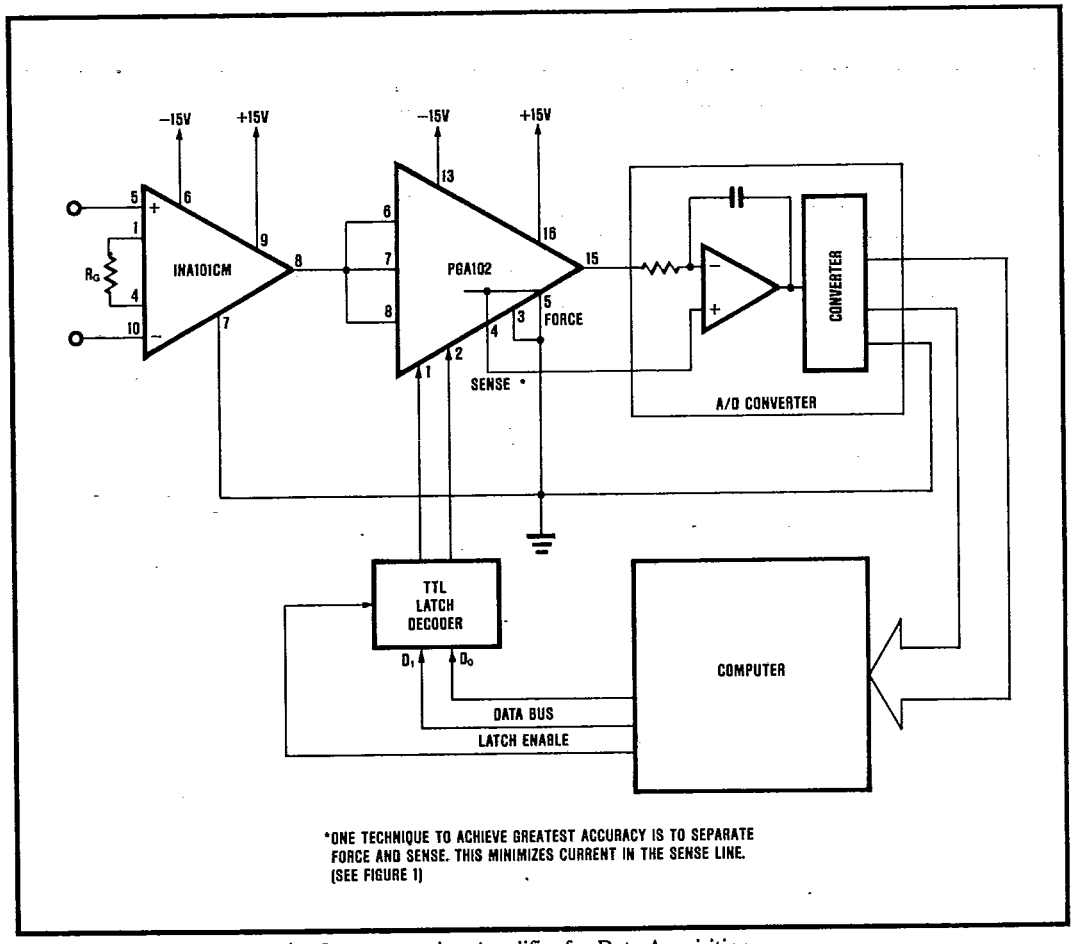


FIGURE 11. Auto-Gain Ranging Instrumentation Amplifier for Data Acquisition.

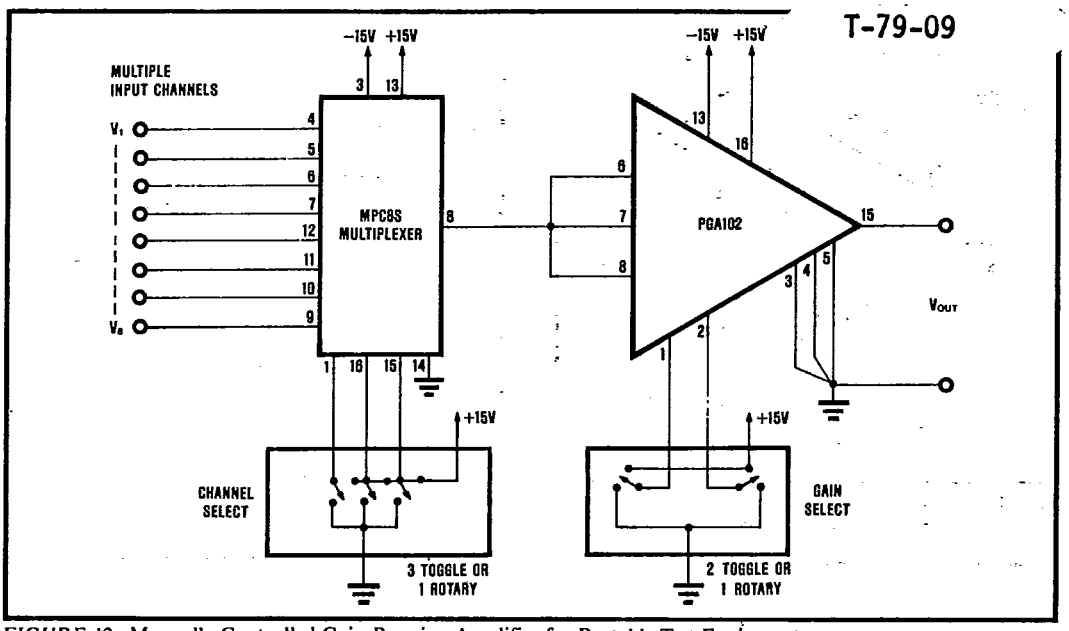


FIGURE 12. Manually Controlled Gain-Ranging Amplifier for Portable Test Equipment.

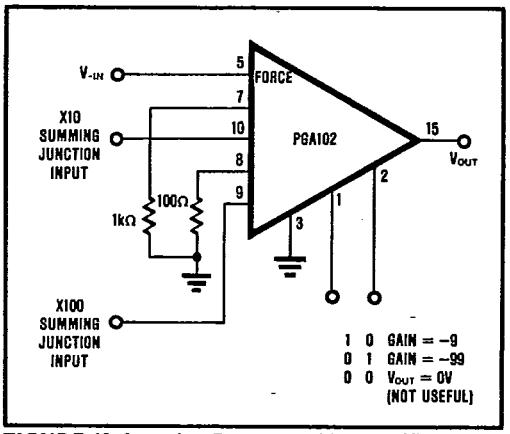


FIGURE 13. Inverting Programmable Amplifier. Summing Junctions Can Be Used for Offsetting.

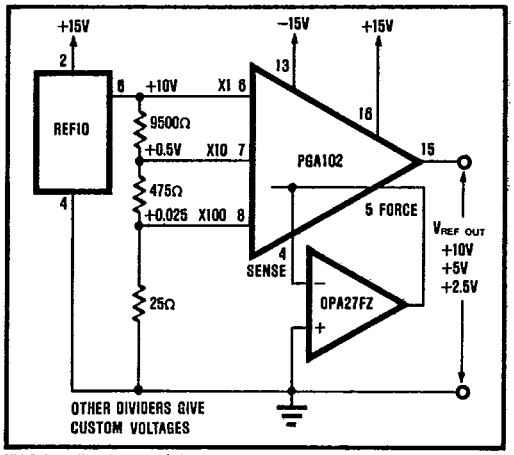


FIGURE 14. Precision Programmable Voltage Reference.

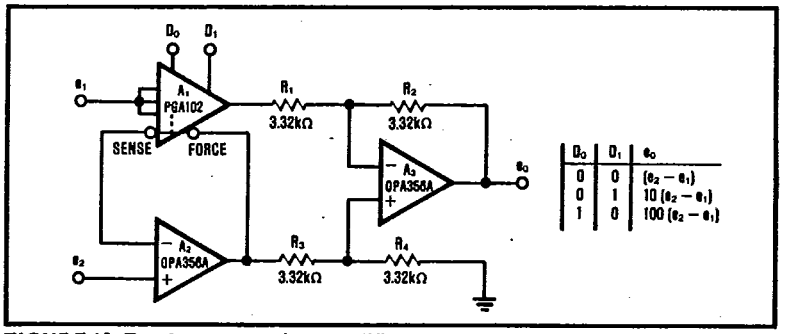


FIGURE 15. Fast Instrumentation Amplifier.