ANALOG DEVICES

LC²MOS 5μs 8-Bit ADC with Track/Hold

AD7575

1.1 Scope.

This specification covers the detail requirements for an 8-bit microprocessor compatible analog-to-digital converter with a built-in track/hold function. The successive approximation technique is used to achieve a conversion time of 5μs, while the on-chip track/hold allows full-scale signals up to 50kHz to be digitized. The AD7575 operates with a single +5V supply, a +1.23V bandgap reference and converts an input signal range of 0 to $2V_{REF}$.

1.2 Part Number.

The complete part numbers per Table 1 of this specification are as follows:

Device	Part Number[1]
−1	AD7575S(X)/883B
−2	AD7575T(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-18	18-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{DD} to AGND	−0.3V, +7V
V_{DD} to DGND	−0.3V, +7V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND (Pins 1, 2)	−0.3V, V_{DD}
Digital Output Voltage to DGND (Pins 4, 6–8, 10–14)	−0.3V, V_{DD}
CLK Input Voltage (Pin 5) to DGND	−0.3V, V_{DD}
V_{REF} to AGND	−0.3V to V_{DD}
AIN to AGND	−0.3V to V_{DD}
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-18 and E-20A
θ_{JA} = 120°C/W for Q-18 and E-20A

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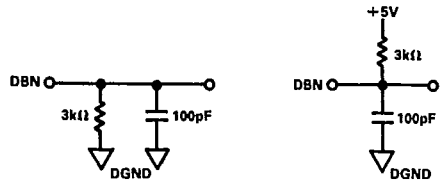
Table 1.

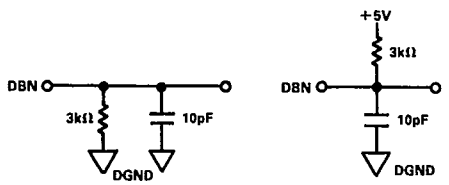
Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Resolution	RES	–1, 2	8				This is the minimum resolution for which no missing codes are guaranteed.	Bits
Total Unadjusted Error	TUE	–1	2	2	2			± LSB max
		–2	1	2	1	1		
Relative Accuracy	RA	–1	1	1	1			± LSB max
		–2	0.5	1	0.5	0.5		
Full-Scale Error		–1, 2	1	1	1			± LSB max
Offset Error		–1, 2	0.5	0.5	0.5		Measured with respect to an ideal first code transition which occurs at 1/2LSB.	± LSB max
Analog Input Voltage Range	AIN	–1, 2	0 to $2V_{REF}$					V
DC Input Impedance	Z_{IN}	–1, 2	10	10	10			MΩ min
Slew Rate Tracking		–1, 2	0.386					V/μs max
Signal Noise Ratio		–1, 2	45				V_{IN} = 2.46V p-p @ 10kHz	dB min
Reference Input Current	I_{REF}	–1, 2	500	500	500			μA max
Digital Input Low Voltage	V_{IL}	–1, 2	0.8	0.8	0.8		$\overline{CS}$, $\overline{RD}$, CLK	V max
Digital Input High Voltage	V_{IH}	–1, 2	2.4	2.4	2.4		$\overline{CS}$, $\overline{RD}$, CLK	V min
Digital Input Current	I_{IN}	–1, 2	10	1	10		$\overline{CS}$, $\overline{RD}$, V_{IN} = 0 or V_{DD}; V_{DD} = 5.2V	± μA max
Digital Input Capacitance	C_{IN}	–1, 2	10				$\overline{CS}$, $\overline{RD}$	pF max
Digital Input Low Current	I_{IL}	–1, 2	800	800	800		CLK; V_{IL} = 0V	μA max
Digital Input High Current	I_{IH}	–1, 2	800	800	800		CLK, V_{IH} = V_{DD}	μA max
Digital Output Low Voltage	V_{OL}	–1, 2	0.4	0.4	0.4		$\overline{BUSY}$, DB0 to DB7 I_{SINK} = 1.6mA; V_{DD} = 4.75V	V max
Digital Output High Voltage	V_{OH}	–1, 2	4.0	4.0	4.0		BUSY, DB0 to DB7 I_{SOURCE} = 40μA; V_{DD} = 4.75V	V min
Floating State Leakage Current	I_{OUT}	–1, 2	10	10	10		DB0 to DB7 V_{OUT} = 0 to V_{DD}; V_{DD} = 5.2V	± μA max
Floating State Output Capacitance	C_{OUT}	–1, 2	10				DB0 to DB7	pF max
Conversion Time with External Clock	t_{CONV}	–1, 2	5	5	5		f_{CLK} = 4MHz	μs
Conversion Time with External Clock @ +25°C	t_{CONV}	–1, 2	5			5	Recommended Clock Components: R = 100kΩ, C = 100pF	μs min
			15			15		μs max
$\overline{CS}$ to $\overline{RD}$ Setup Time, t_1	t_{WSCS}	–1, 2	0					ns min
$\overline{RD}$ to BUSY Propagation Delay, t_2	t_{WBPD}	–1, 2	120					ns max
Data Access Time after $\overline{RD}$, t_3[2]	t_{DAR}	–1, 2	120					ns max
$\overline{RD}$ Pulse Width, t_4	t_{RD}	–1, 2	120					ns min
$\overline{CS}$ to $\overline{RD}$ Hold Time, t_5	t_{RHS}	–1, 2	0					ns min
Data Access Time after $\overline{BUSY}$, t_6[2]	t_{DAB}	–1, 2	100					ns max
Data Hold Time, t_7[3]	t_{DH}	–1, 2	10					ns min
			100					ns max
$\overline{BUSY}$ to $\overline{CS}$ Delay, t_8	t_{BCD}	–1, 2	0					ns min
Power Supply Current	I_{DD}	–1, 2	7	7	7		V_{DD} = 5.2V	mA max
Power Supply Rejection		–1, 2	0.25	0.25	0.25			± LSB max

NOTES
[1] V_{DD} = +5V; (unless otherwise stated) V_{REF} = +1.23V; AGND = DGND = 0V; f_{CLK} = 4MHz external. All input control signals are specified with t_r = t_f = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2] t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V to 2.4V.
[3] t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.



a. High-Z to V_{OH} b. High-Z to V_{OL}

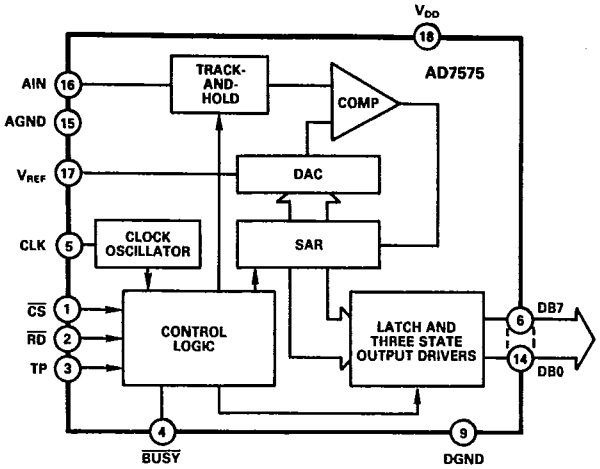
Figure 1. Load Circuits for Data Access Time Test



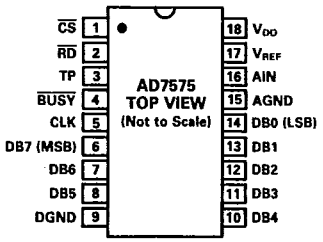
a. V_{OH} to High-Z b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

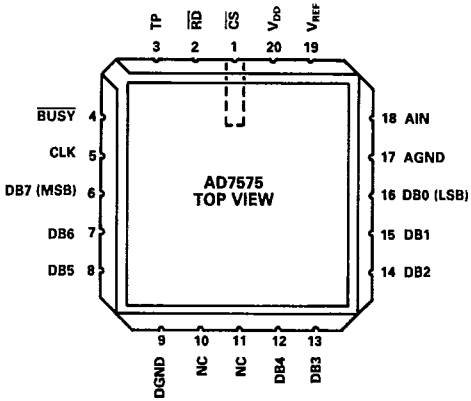
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (Cerdip)



E Package (LCC)

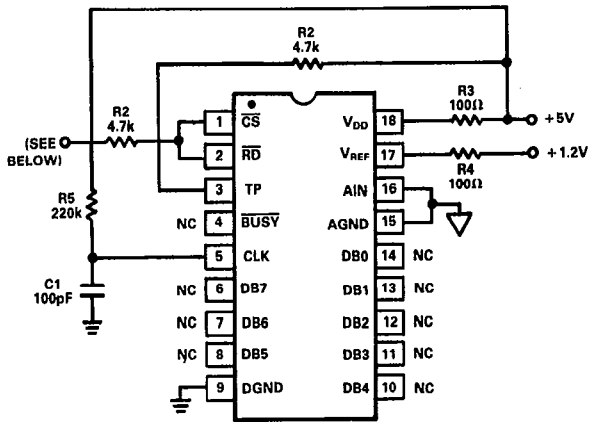


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

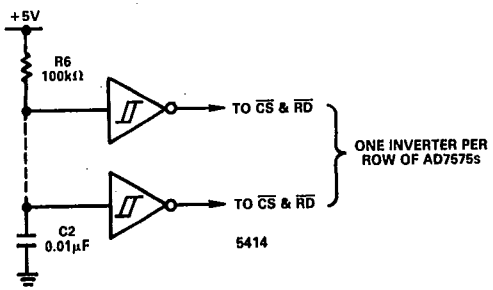
4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ALL RESISTORS ARE 1/4W.
$\overline{CS}$ AND $\overline{RD}$ ARE TAKEN HIGH FOR 0.6ms – 0.7ms APPROXIMATELY AND ARE THEN BROUGHT LOW. THIS IS ACHIEVED AS FOLLOWS:

NOTE
$\overline{CS}$/$\overline{RD}$ PULSE MAY BE GENERATED EXTERNALLY.



5.0 Timing and Control of the AD7575.

The two logic inputs on the AD7575, $\overline{CS}$ and $\overline{RD}$, control both the starting of conversion and the reading of data from the part. A conversion is initiated by bringing both these control inputs LOW. Two interface options then exist for reading the output data from the AD7575. These are the Slow Memory Interface and ROM Interface and their operation is outlined below. It should be noted that the TP pin of the AD7575 must be hardwired HIGH to ensure correct operation of the part. This pin is used in testing the device and should not be used as a feedthrough pin in double-sided printed circuit boards.

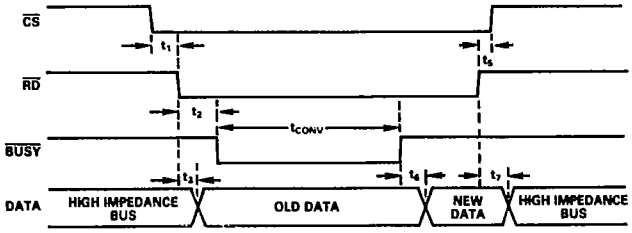


Figure 3. Slow Memory Interface Timing Diagram

5.1 Slow Memory Interface.

The first interface option is intended for use with microprocessors which can be forced into a WAIT STATE for at least 5μs (such as the 8085A). The microprocessor starts a conversion and is halted until the result of the conversion is read from the converter. Conversion is initiated by executing a memory READ to the AD7575 address bringing $\overline{CS}$ and $\overline{RD}$ LOW. $\overline{BUSY}$ subsequently goes LOW (forcing the microprocessor READY input LOW) placing the processor into a WAIT state. The input signal, which had been tracked by the analog input, is held on the third falling clock edge of the input clock after $\overline{CS}$ and $\overline{RD}$ have gone LOW. The AD7575 then performs a conversion on this acquired input signal value. When the conversion is complete ($\overline{BUSY}$ goes HIGH), the processor completes the memory READ and acquires the newly-converted data. The timing diagram for this interface is shown in Figure 3.

The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT and then READ data with a single READ instruction. The fast conversion time of the AD7575 ensures that the microprocessor is not placed in a WAIT state for an excessive amount of time.

Faster versions of many processors, including the 8085A-2, test the condition of the READY input very soon after the start of an instruction cycle. Therefore, $\overline{BUSY}$ of the AD7575 must go LOW very early in the cycle for the READY input to be effective in forcing the processor into a WAIT state. When using the 8085A-2, the processor S0 status signal provides the earliest possible indication that a READ operation is about to occur. Hence, S0 (which is LOW for a READ cycle) provides the READ signal to the AD7575. The connection diagram for the AD7575 to 8085A-2 Slow-Memory interface is shown in Figure 4.

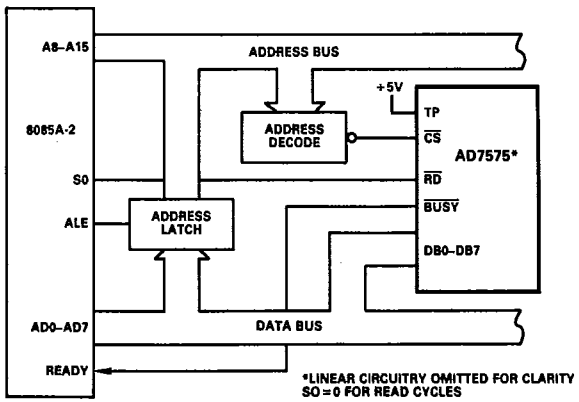


Figure 4. AD7575 to 8085A-2 Slow Memory Interface

5.2 ROM Interface.

The alternative interface option on the AD7575 avoids placing the microprocessor into a WAIT state. In this interface, a conversion is started with the first READ instruction and the second READ instruction accesses the data and starts a second conversion. The timing diagram for this interface is shown in Figure 5. It is possible to avoid starting another conversion on the second READ (see below).

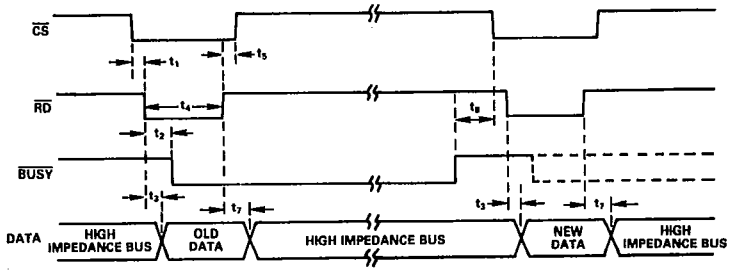


Figure 5. ROM Interface Timing Diagram

Conversion is initiated by executing a memory READ instruction to the AD7575 address causing $\overline{CS}$ and $\overline{RD}$ to go LOW. Data is also obtained from the AD7575 during this instruction. This is old data and may be disregarded if not required. $\overline{BUSY}$ goes LOW indicating that conversion is in progress and returns HIGH when conversion is complete. Once again the input signal is held on the third falling edge of the input clock after $\overline{CS}$ and $\overline{RD}$ have gone LOW.

The $\overline{BUSY}$ line may be used to generate an interrupt to the microprocessor or monitored to indicate that conversion is complete. The processor then reads the newly-converted data. Alternatively, the delay between the convert start (first READ instruction) and the data READ (second READ instruction) must be at least as great as the AD7575 conversion time. For the AD7575 to operate correctly in the ROM interface mode $\overline{CS}$ and $\overline{RD}$ should not go LOW before $\overline{BUSY}$ returns HIGH.

Normally, the second READ instruction starts another conversion as well as accessing the output data. However, if $\overline{CS}$ and $\overline{RD}$ are brought LOW within one external clock period of $\overline{BUSY}$ going HIGH then a second conversion does not occur.

Figures 6 and 7 show connection diagrams for interfacing the AD7575 in the ROM Interface mode. Figure 6 shows the AD7575 interface to the 6502/6809 microprocessors while the connection diagram for interfacing to the Z-80 is shown in Figure 7.

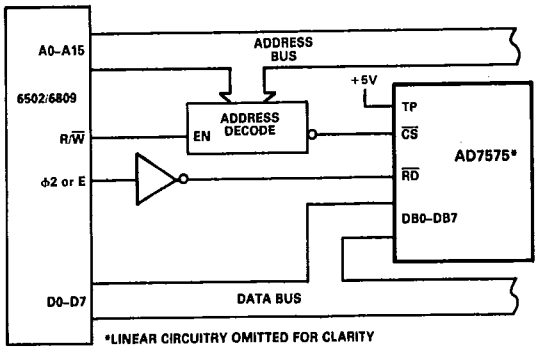


Figure 6. AD7575 to 6502/6809 ROM Interface

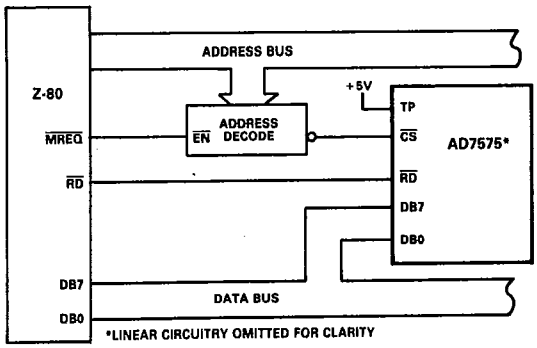


Figure 7. AD7575 to Z-80 ROM Interface

As a result of its very fast interface timing the AD7575 can also be interfaced to the DSP processor, the TMS32010. The AD7575 will interface (within specifications) to the TMS32010 running at up to 18MHz but will typically work over the full clock frequency range of the TMS32010. Figure 8 shows the connection diagram for this interface. The AD7575 is mapped at a port address. Conversion is initiated using an IN A, PA instruction where PA is the decoded port address for the AD7575. The conversion result is obtained from the part using a second IN A, PA instruction and the resultant data is placed in the TMS32010 accumulator.

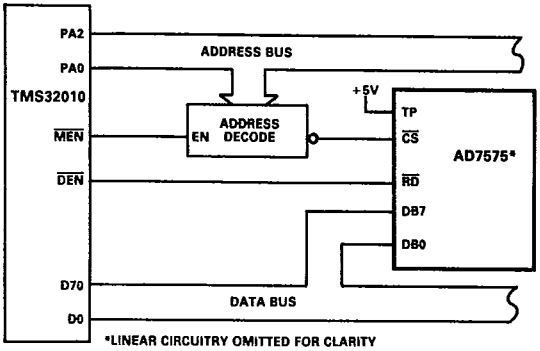


Figure 8. AD7575 to TMS32010 ROM Interface

In many applications it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. The interfaces outlined previously require that for sampling at equi-distant intervals the user must count clock cycles or match software delays. This is especially difficult in interrupt driven systems where uncertainty in interrupt servicing delays would require that the AD7575 would have to have priority interrupt status and even then redundant software delays may be necessary to equalize loop delays.

This problem can be overcome by using a real time clock to control the starting of conversion. This can be derived from the clock source used to drive the AD7575 CLK pin. Since the sampling instant occurs three clock cycles after $\overline{CS}$ and $\overline{RD}$ go LOW then the input signal sampling intervals are equi-distant. The resultant data is placed in a FIFO latch which can be accessed by the microprocessor at its own rate whenever it requires the data. This ensures that data is not READ from the AD7575 during a conversion. If a data READ is performed during a conversion, valid data from the previous conversion will be accessed but the conversion in progress may be interfered with and an incorrect result is likely.

If $\overline{CS}$ and $\overline{RD}$ go LOW within 20ns of a falling clock edge the AD7575 may or may not see that falling edge as the first of the three falling clock edges to the sampling instant. In this case the sampling instant could vary by one clock period. If it is important to know the exact sampling instant, $\overline{CS}$ and $\overline{RD}$ should not go LOW within 20ns of a falling clock edge.