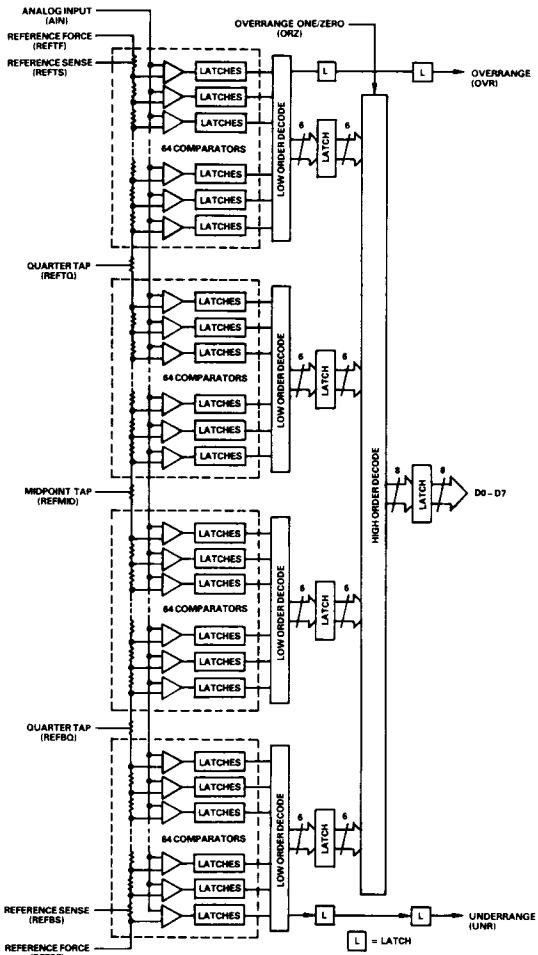
200 MSPS Wideband 8-Bit A/D Converter

AD770*

FEATURES

250MHz Full Power Bandwidth
200 MSPS Guaranteed Conversion Rate
19pF typ Input Capacitance
Unipolar and Bipolar Input Range
+5V/−5.2V Power Supplies
Overflow and Underflow Signals

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD770 is an 8-bit analog-to-digital converter that is designed for high-speed digitization of wide-bandwidth signals. It uses an advanced VLSI bipolar process and a proprietary design to achieve a combination of sampling rate and signal bandwidth previously unavailable in flash ADCs.

The AD770 incorporates 257 high speed comparators that are optimized for low input capacitance and wide bandwidth, unaffected by temperature or signal amplitude. The multistage comparator design reduces the probability of errors due to metastable states or insufficient gain.

The decoding logic further reduces errors by using a two-stage error-correcting architecture to virtually eliminate "sparkle codes." Inputs and outputs are ECL compatible. Output format controls allow stacking of two devices for 9-bit resolution. Overflow and underflow output signals are provided.

The AD770 can operate with unipolar and bipolar signal ranges up to 4V p-p. End-point reference Force and Sense connections are provided to preserve high accuracy and minimize temperature drift. Midpoint and quarter-point reference taps are also provided to allow linearity or transfer function corrections.

The AD770 is available in three grades. The JD and KD grades are specified for operation over the 0 to +70°C temperature range, while the SD grade is specified for the −55°C to +125°C temperature range. All grades are packaged in a 40-pin ceramic DIP. Other package options are available on request; please contact the factory.

PRODUCT HIGHLIGHTS

1. **Performance:** The AD770 is specified for operation at 200 MSPS. Full power bandwidth is 250MHz; small signal bandwidth is 400MHz.
2. **Ease of Use:** The AD770 input has a typical capacitance of 19pF, simplifying input buffering requirements. Bipolar and unipolar input signals can be converted without offsetting. Differential or single-ended clock inputs can be accommodated by pin-strapping.
3. **Features:** Taps are provided at mid- and quarter-scale points of the reference ladder to permit linearity trimming or piecewise-linear transfer function modification. Overflow and underflow signals are also provided. These can be wire-or'd to provide an indication that the input signal has exceeded the range of the converter.

*Protected by U.S. Patent No. 4,884,075.

AD770—SPECIFICATIONS

DC SPECIFICATIONS (typical at +25°C, V_{CC} = 5.0 V, V_{EE} = 5.2 V, V_{REFTS} = −1.0 V, V_{REFBS} = 1.0 V, unless otherwise specified)

Parameter	Conditions	AD770J/S Min	AD770J/S Typ	AD770J/S Max	AD770K Min	AD770K Typ	AD770K Max	Units
TEMPERATURE RANGE	AD770J, AD770K	0		+70	0		+70	°C
	AD770S	−55		+125				°C
RESOLUTION		8			8			Bits
DC ACCURACY								
Linearity Error	+25°C	−1		+1	−0.75		+0.75	LSB
	T_{min}–T_{max}	−1.25		+1.25	−1		+1	LSB
Differential Linearity	+25°C	−0.9		+0.9	−0.75		+0.75	LSB
	T_{min}–T_{max}	−1.25		+1.25	−0.9		+0.9	LSB
Absolute Accuracy	+25°C	−1.75		+1.75	−1		+1	LSB
	T_{min}–T_{max}	−2		+2	−1.25		+1.25	LSB
REFERENCE LADDER								
Ladder Resistance		160	200	260	160	200	260	Ω
Ladder TC			0.34			0.34		%/°C
Top Force-Sense Offset	T_{min}–T_{max}		3	5		3	5	LSB
Bottom Force-Sense Offset	T_{min}–T_{max}		3	5		3	5	LSB
ANALOG INPUT								
Input Current	V_{IN} = −1V to +1V			300			300	µA
	T_{min}–T_{max}			500			500	µA
Input Capacitance		17	19	22	17	19	22	pF
DIGITAL INPUTS	T_{min}–T_{max}							
Logic HIGH (V_{IH})		−1.0		−0.7	−1.0		−0.7	V
Logic LOW (V_{IL})		−1.9		−1.6	−1.9		−1.6	V
Logic HIGH Current (I_{IH})				200			200	µA
Logic LOW Current (I_{IL})				200			200	µA
Input Capacitance			3			3		pF
DIGITAL OUTPUTS								
Logic HIGH (V_{OH})	100Ω Load to −2V	−1.0		−0.7	−1.0		−0.7	V
Logic LOW (V_{OL})	100Ω Load to −2V	−1.9		−1.6	−1.9		−1.6	V
V_{BB}			−1.2			−1.2		V
POWER SUPPLIES								
V_{CC}		4.75	5.0	5.25	4.75	5.0	5.25	V
V_{EE}		−5.46	−5.2	−4.9	−5.46	−5.2	−4.9	V
I_{CC} (Analog)			210	269		210	269	mA
I_{CC} (Digital)			62	78		62	78	mA
I_{EE} (Analog)			54	69		54	69	mA
I_{EE} (Digital)			69	88		69	88	mA
Power Consumption			2000	2550		2000	2550	mW

Specifications subject to change without notice.

AC SPECIFICATIONS (typical at +25°C, V_{CC} = 5.0 V, V_{EE} = −5.2 V, unless otherwise noted)

Parameter	Conditions		AD770J/S Min	AD770J/S Typ	AD770J/S Max	AD770K Min	AD770K Typ	AD770K Max	Units
TIMING	T_{min}–T_{max}, 100Ω Load to −2V								
Max Conversion Rate			**200**			**200**			MSPS
Aperture Delay				340			340		ps
Aperture Jitter				3			3		ps rms
Pipeline Delay			1.5		1.5	1.5		1.5	Clock Cycles
Output Delay			**2**		**6**	**2**		**6**	ns
Output Rise				1			1		ns
Output Fall				1			1		ns
Output Skew				1.4	**2.35**		1.4	**2.35**	ns
DYNAMIC PERFORMANCE	F_{IN}	Full Scale							
(@200 MSPS)	(MHz)	A_{IN} (Volts)							
Full-Power Bandwidth		±1		250			250		MHz
Small-Signal Bandwidth		±1		400			400		MHz
Harmonic Distortion[1]	1	±1		50			53		dB
	10	±1		43.5			45.5		dB
	50	±1		35.5			36		dB
	100	±1		25.5			26		dB
	1	±0.5		49			52		dB
	10	±0.5		42			43.5		dB
	50	±0.5		38			39		dB
	100	±0.5		31.5			32		dB
Signal-to-Noise Ratio[1]	1	±1		44.0 (7.0)			44.5 (7.1)		dB (ENOB)
	10	±1		41.5 (6.6)			42.0 (6.7)		dB (ENOB)
	50	±1		34.0 (5.4)			34.5 (5.4)		dB (ENOB)
	100	±1		25.0 (3.9)			25.5 (3.9)		dB (ENOB)
	1	±0.5		40.5 (6.4)			41.0 (6.5)		dB (ENOB)
	10	±0.5		39.0 (6.2)			39.5 (6.3)		dB (ENOB)
	50	±0.5		35.5 (5.6)			35.5 (5.6)		dB (ENOB)
	100	±0.5		30.0 (4.7)			31.0 (4.9)		dB (ENOB)

NOTES
[1]Signal-to-Noise Ratio includes harmonics in the noise factor.
Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

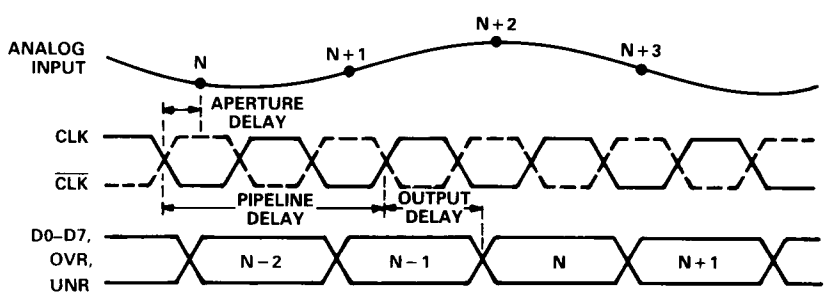
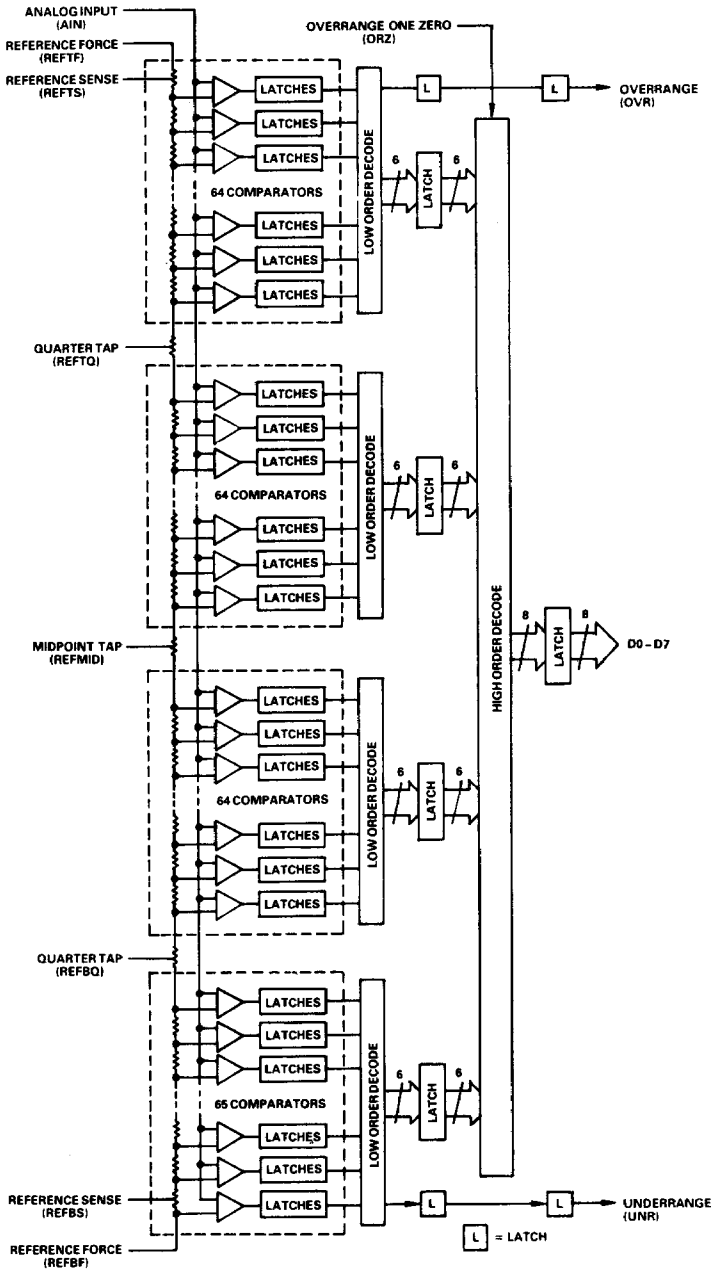


Figure 1. AD770 Timing Diagram

FUNCTIONAL BLOCK DIAGRAM

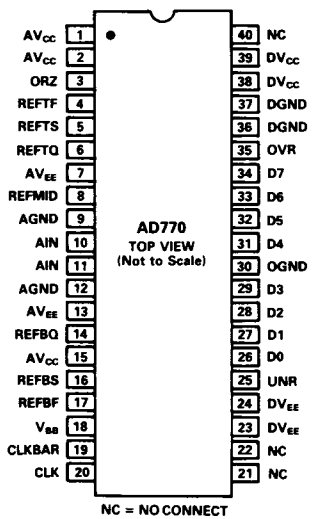


AD770 PIN DESCRIPTION

SYMBOL	PIN NO.	TYPE	NAME AND FUNCTION
AGND	9, 12	P	Analog Ground
AIN	10, 11	AI	Analog Input
AV_{CC}	1, 2, 15	P	+5V Analog Power
AV_{EE}	7, 13	P	5.2V Analog Power
CLK	20	DI	Clock Input
CLKBAR	19	DI	Complementary Clock Input
DGND	36, 37	P	Digital Ground
DV_{CC}	38, 39	P	+5V Digital Power
DV_{EE}	23, 24	P	5.2V Digital Power
D0	26	DO	Data Bit Output (LSB)
D1	27	DO	Data Bit Output
D2	28	DO	Data Bit Output
D3	29	DO	Data Bit Output
D4	31	DO	Data Bit Output
D5	32	DO	Data Bit Output
D6	33	DO	Data Bit Output
D7	34	DO	Data Bit Output (MSB)
DGND	30	P	Digital Output Ground (collectors of output transistors.)
ORZ	3	DI	Overrange Zero. Sets the Polarity of the Data Bits for Overrange Condition. If ORZ%HIGH, D0-D7 are LOW for Overrange Conditions.
OVR	35	DO	Overrange Output. Indicates that AIN$ (REFTS - 0.5LSB).
REFBF	17	AI	Negative Reference Force
REFBQ	14	AI	Negative Reference Quarter Point
REFBS	16	AO	Negative Reference Sense
REFMID	8	AI	Reference Midpoint
REFTF	4	AI	Positive Reference Force
REFTQ	6	AI	Positive Reference Quarter Point
REFTS	5	AO	Positive Reference Sense
UNR	25	DO	Underrange Output. UNR m= HIGH when AIN<(REFBS − 0.5 LSB).
V_{BB}	18	DO	ECL Threshold Output for Clocks

TYPE: AI = Analog Input
AO = Analog Output
DI = Digital Input
DO = Digital Output
P = Power

AD770 PINOUT (40-PIN DIP)



NC = NO CONNECT

EVALUATION BOARD

The ADEB770 Evaluation Board allows the designer to easily evaluate the performance of the AD770. The ADEB770 includes a pin-socketed AD770, an input signal buffer and an adjustable reference generator. The input buffer can be bypassed for maximum versatility.

On the output side, latched and buffered digital data is available at the output connector along with an output clock. Decimation hardware allows output data to be undersampled by factors of 16 through 2, allowing the user to interface the board to commonly available logic analyzers.

A reconstructed analog output is also provided by an on-board D/A converter.

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect to	Min	Max	Units
AV_{CC}	AGND	−0.3	5.5	V
DV_{CC}	DGND	−0.3	5.5	V
AV_{EE}	AGND	−5.72	0.3	V
DV_{EE}	DGND	−5.72	0.3	V
AV_{CC}	DV_{CC}	−0.5	0.5	V
AV_{EE}	DV_{EE}	−0.5	0.5	V
AIN	AGND	−3	+2.25	V
AIN	REFTF, REFBF	−4.3	4.3	V
CLK, CLKBAR, ORZ	AGND	−4.0	0	V
REFTF, REFBF	AGND	−3	+2.25	V
AGND	DGND	−0.5	0.5	V
CLK	CLKBAR	−4.5	4.5	V
I_{AIN}			110	mA
I_{REFTF}, I_{REFBF}			30	mA
I_{REFTS}, I_{REFBS}			3	mA
I_{REFMID}, I_{REFTQ}, I_{REFBQ}			30	mA
I_{BB}			4	mA
I_{CLK}, $I_{CLK\ BAR}$, I_{ORZ}			1	mA
$I_{D0\text{-}D7}$, I_{OVR}, I_{UNR}			40	mA
Junction Temperature			175	°C
Power Dissipation (+25°C)			3	W
Storage Temperature		−65	+150	°C
Thermal Resistance				
θ_{JA} (Still Air) (typ)			36	°C/W
θ_{JC} (typ)			10	°C/W

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Description	Temperature Range	Linearity Error Max @ +25°C	Package Option*
AD770JD	40-Pin Ceramic DIP	0°C to +70°C	±1	D-40
AD770KD	40-Pin Ceramic DIP	0°C to +70°C	±3/4	D-40
AD770SD	40-Pin Ceramic DIP	−55°C to +125°C	±1	D-40
AD770EB-1	Evaluation Board for AD770		±1	
AD770EB-2	Evaluation Board for AD770		±3/4	

*D = Ceramic DIP. For outline information see Package Information section.

DEFINITION OF SPECIFICATIONS

Linearity Error
Linearity Error is the deviation of the transfer function from a reference line. For the AD770, the linearity error is measured from the center of each code to the best-fit straight line.

Differential Linearity
In an ideal ADC, the code transitions are exactly 1LSB apart. The Differential Linearity is the deviation of the transition spacing from the ideal value. A Differential Linearity spec of less than 1LSB signifies that there are no missing output codes over the entire input range.

Absolute Accuracy
The Absolute Accuracy is the deviation of the center-point of each code from a straight line drawn between the reference sense points (REFTS, REFBS).

Force-Sense Offset
The Force-Sense Offset is the difference between the force and sense pin voltages divided by the input range. This offset will cause a corresponding offset error if the full-scale range is defined w.r.t. the reference force lines rather than with respect to the reference sense lines.

Aperture Delay
The delay between the falling edge of CLK and the time at which AIN is sampled.

Aperture Jitter
The sample-to-sample variation in aperture delay.

Pipeline Delay
The delay from the falling edge of CLK that samples the input to the rising edge of CLK that outputs the corresponding digital code.

Output Delay
The delay between the rising edge of CLK and the time when the output bits reach the logic threshold value for bits D0 to D7 and OVR.

Output Skew
The bit-to-bit variation in output delay for bits D0 to D7 and OVR.

Full-Power Bandwidth
The input frequency at which the amplitude of the reconstructed output signal is reduced by 3dB for a full-scale input.

Total Harmonic Distortion (THD)
The rms sum of the first six harmonic components divided by the output signal amplitude. For frequencies above the Nyquist frequency, the aliased components are used.

Signal-to-Noise Ratio (SNR)
The ratio of the signal amplitude to the rms sum of all other spectral components, including harmonics but excluding dc. SNR is expressed in dB and in Effective Number Of Bits (ENOB). These two notations are related by the following formula for full-scale inputs:

$$ENOB = (SNR - 1.8)/6.02$$

(For REFTS = +1.000V, REFBS = −1.000V)

Input			Output		
$A_{IN}>$	$A_{IN}<$	ORZ	D7 . . . . . D0	UNR	OVR
0.996V		0	1 1 1 1 1 1 1 1	0	1
0.996V		1	0 0 0 0 0 0 0 0	0	1
0.988V	0.996V	X	1 1 1 1 1 1 1 1	0	0
0.980V	0.988V	X	1 1 1 1 1 1 1 0	0	0
0.973V	0.980V	X	1 1 1 1 1 1 0 1	0	0
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
−0.004V	0.004V	X	1 0 0 0 0 0 0 0	0	0
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
−0.998V	0.980V	X	0 0 0 0 0 0 1 0	0	0
−0.996V	0.998V	X	0 0 0 0 0 0 0 1	0	0
−1.004	−0.996V	X	0 0 0 0 0 0 0 0	0	0
	−1.004V	X	0 0 0 0 0 0 0 0	1	0

X = Don't care

Table I. AD770 Truth Table

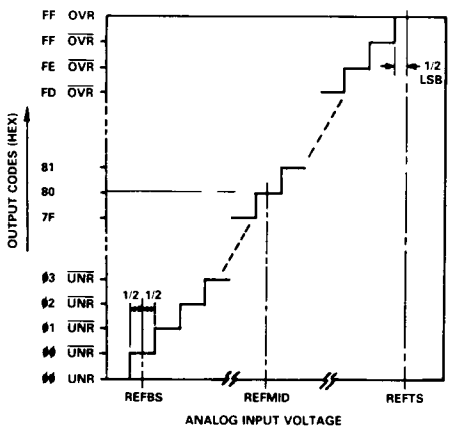


Figure 2. AD770 Transfer Function

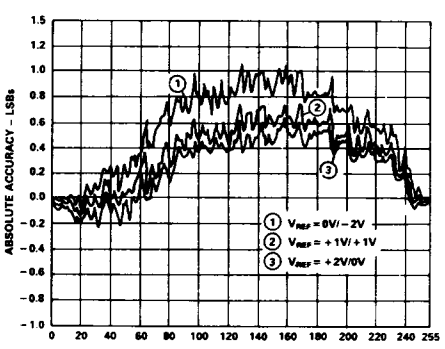


Figure 3. Typical Absolute Accuracy vs. Output Code for Various Range Offsets

AD770—Dynamic Performance

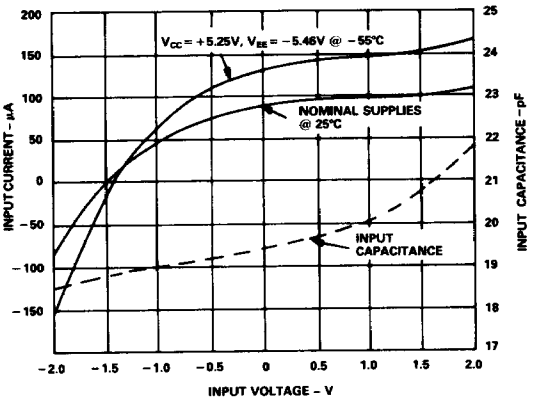


Figure 4. Input Current and Input Capacitance vs. Input Voltage

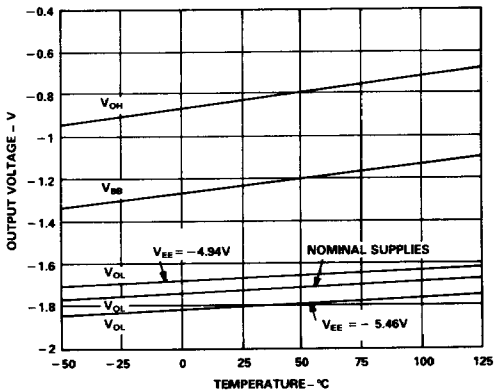


Figure 5. Logic Levels vs. Temperature

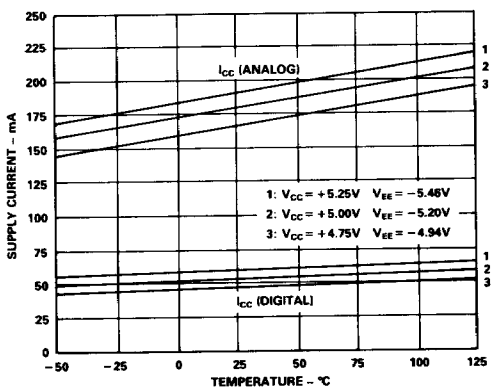


Figure 6. I_{CC} vs. Temperature

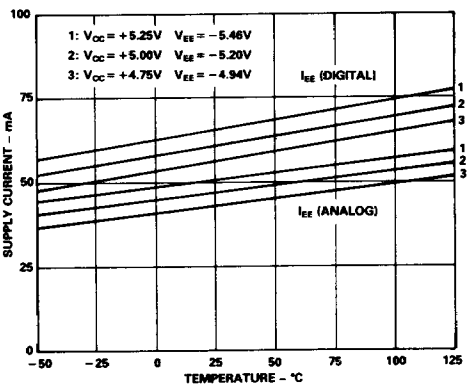


Figure 7. I_{EE} vs. Temperature

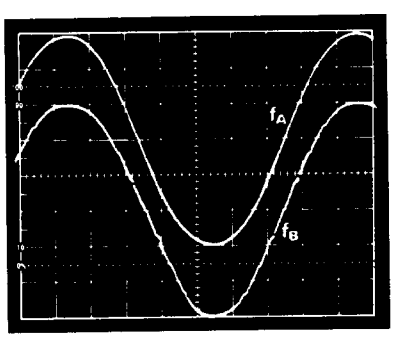


Figure 8. Reconstructed Output of AD770 Decimated by 1:32 @ 200MSPS

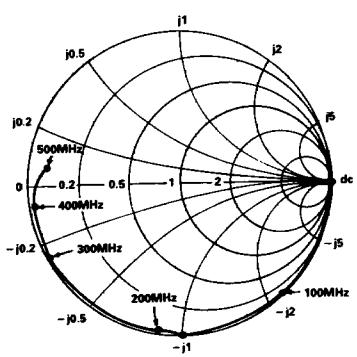


Figure 9. Smith Chart: Input Impedance Normalized to 50Ω vs. Input Frequency

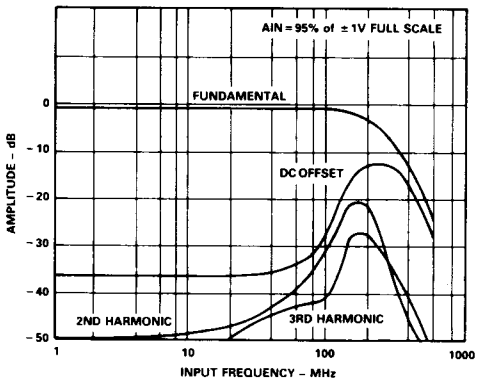


Figure 10. Harmonic Distortion vs. Input Frequency @ 200MSPS: Full Power

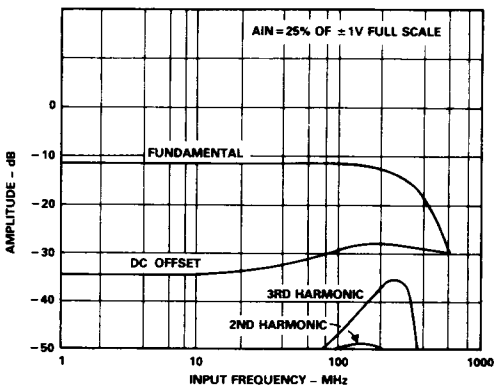


Figure 11. Harmonic Distortion vs. Input Frequency @ 200 MSPS: Small Signal

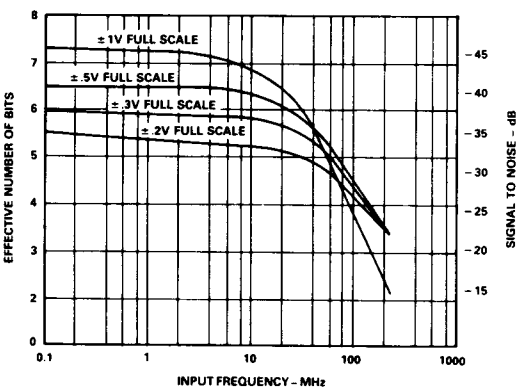


Figure 12. SNR vs. Input Frequency in ENOB and dB

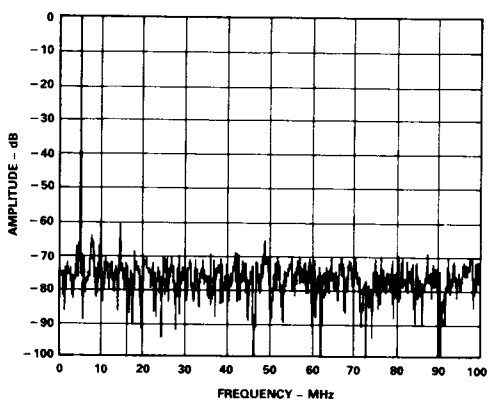


Figure 13. 1024pt FFT of AD770 Output @ 200 MSPS. F_{IN} = 5MHz at ± 1V Full Scale

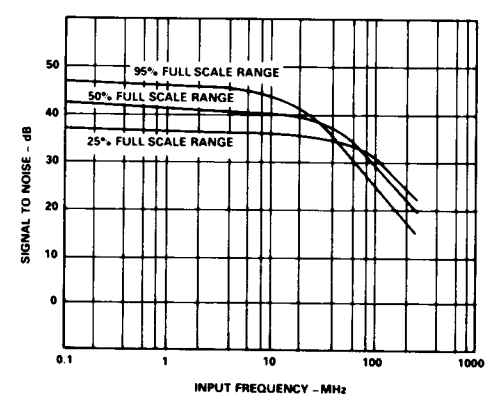


Figure 14. SNR vs. Input Frequency at ± 1V F.S. Input

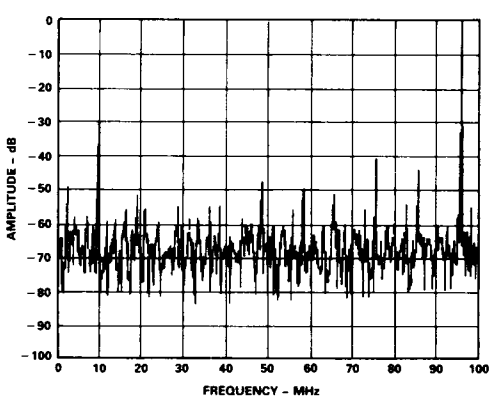


Figure 15. 1024pt FFT of AD770 Output @ 200 MSPS. F_{IN} = 95MHz at ± 1V F.S.

GROUNDING AND DECOUPLING

The user is advised to provide separate, low impedance analog and digital ground planes and tie them together at one place on the board, preferably at, or as near to, the ADC as possible.

The dominant consideration in the selection of bypass capacitors for the AD770 is minimization of series resistance and inductance. Ceramic and film-type capacitors generally feature lower series inductance than tantalum or electrolytic types. The capacitors should be installed on the board with the shortest possible lead lengths. Chip capacitors are optimal in this respect. As shown in Figure 18, the analog ground plane provides bypassing for the analog power supplies (AV_{CC}, AV_{EE}) as well as for the reference top, bottom, mid and quarter voltages. The digital ground plane should be used to bypass the digital supplies (DV_{CC}, DV_{EE}).

To prevent output ringing, a ferrite bead in series with DGND Pins 36 and 37 is recommended. Output lines should be single fanout, properly terminated 100Ω striplines for best results.

DRIVING THE AD770

The AD770 can be driven directly from most signal sources. The termination of the signal source, however, will affect the input bandwidth. Two possibilities are shown in Figure 16.

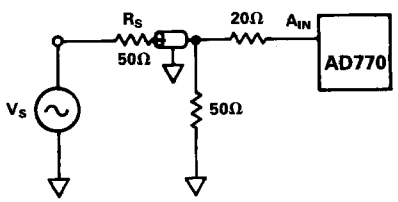


Figure 16a. 50Ω Shunt Termination

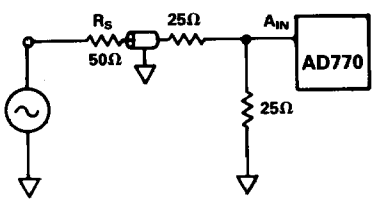
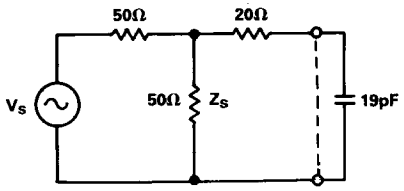


Figure 16b. 50Ω Termination (−6dB) Employing 25Ω Series and 25Ω Shunt Resistors

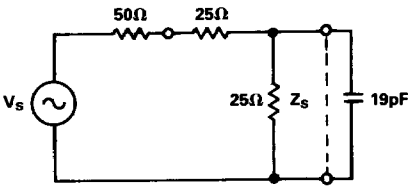
Both terminations result in 50Ω to ground; however the network of Figure 16b provides a lower impedance to the AD770 over frequency as well as a higher −3dB point at the device. The trade-off is that Figure 16b attenuates the signal source by a factor of two (−6dB). These effects may be illustrated by modeling the input to the AD770 as a 19pF capacitor and analyzing the two termination networks as shown in Figure 17.

The −6dB network requires an input signal with twice the amplitude of the simple 50Ω shunt termination, but the benefits can be easily justified. The termination impedance reaches a high frequency value of 25Ω, versus 14Ω for the standard termination network. Another advantage is that the half-power bandwidth is more than twice that of the standard 50Ω shunt network.



1. **IMPEDANCE SEEN BY AD770:**
   $Z_S = 20\Omega + (50 \| 50) = 45\Omega$
2. **−3dB POINT AT AD770:**
   $f_o = (2\pi 45\Omega \cdot 19pF)^{-1}$
   $f_o = 186MHz$

Figure 17a. Network for 50Ω Shunt Termination



1. **IMPEDANCE SEEN BY AD770:**
   $Z_S = 25\Omega \| 25\Omega + 50\Omega) = 19\Omega$
2. **−3dB POINT AT AD770:**
   $f_o = (2\pi 19\Omega \cdot 19pF)^{-1}$
   $f_o = 441MHz$

Figure 17b. Network for 25Ω Series and 25Ω Shunt Termination.

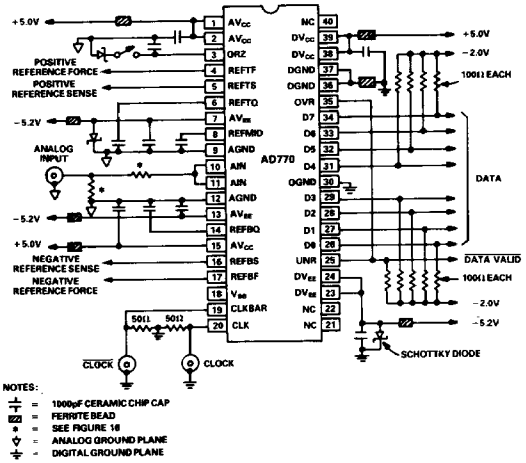


Figure 18. AD770 Application Example

LATCHING THE OUTPUT DATA

A simplified AD770 timing diagram is illustrated in Figure 19. The input signal is sampled on the falling edge of CLK. The output data for that sample is delayed by the Pipeline Delay plus the Output Delay. The Pipeline Delay is two CLK low periods and one CLK high period, and thus depends on the conversion rate and the clock duty cycle. Output Delay is measured from the second CLK rising edge after the falling edge which samples the analog input signal. Output Delay is not dependent on the conversion rate.

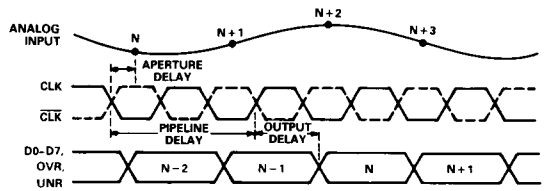


Figure 19. AD770 Timing Diagram

Output Delay varies from unit to unit due to manufacturing process variations. This factor, and the timing requirements of the external latch, must be considered when designing the output clock circuit.

Figure 20 shows a more detailed timing diagram that illustrates the effect of Output Delay variations and external latch timing requirements. Data bit transitions are shown for units at the extreme limits of Output Delay (T_D). For a unit with $T_D = T_{Dmin}$, the data bits will begin to slew after a delay of T_{Dmin}, and all bits will have settled after a further delay of T_{SK} (Output Skew). The data will then be stable until the next output data transition.

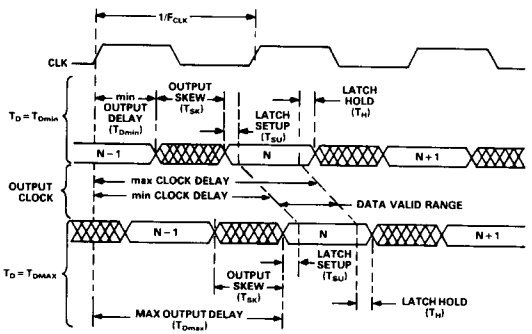


Figure 20. Detailed Timing Diagram Showing Output Delay Variation

However, the Setup and Hold times (T_{SU} and T_H) of the external latch must be subtracted to obtain the interval during which the external latch can be clocked (Data Valid Range). Thus:

$$\text{Data Valid Range} = 1/F_{CLK} - T_{SK} - T_{SU} - T_{TH}$$

The clock circuit will require a maximum delay that can also be easily derived:

$$\text{Max Clock Delay (for } T_D = T_{Dmin}) = 1/F_{CLK} + T_{Dmin} - T_H$$

For a unit with $T_D = T_{Dmax}$, the clock delay will be determined by the Maximum Output Delay (T_{Dmax}):

$$\text{Min Clock Delay (for } T_D = T_{Dmax}) = T_{Dmax} + T_{SU}$$

If the Maximum Clock Delay for $T_D = T_{Dmin}$ is greater than the Minimum Clock Delay for $T_D = T_{Dmax}$, a fixed clock delay set between these two values can be used to latch the output of the AD770.

$$T_{Dmax} + T_{SU} < \text{Fixed Clock Delay} < 1/F_{CLK} + T_{Dmin} - T_H$$

For example, a 120 MSPS system using 100K ECL logic would have the following conditions:

$T_{Dmax} = 6.0\text{ns}$
$T_{SU} = 0.7\text{ns}$
$F_{CLK} = 120\text{MHz}$
$T_{Dmin} = 2.0\text{ns}$
$T_H = 0.7\text{ns}$

Max Clock Delay (for $T_D = T_{Dmin}$) $= 1/F_{CLK} + T_{Dmin} - T_H$
$= 9.6\text{ns}$

Min Clock Delay (for $T_D = T_{Dmax}$) $= T_{Dmax} + T_{SU} = 6.7\text{ns}$

A fixed clock delay could thus be used, with the following limits:

$6.7\text{ns} < \text{Clock Delay} < 9.6\text{ns}$

As the sample rate increases, the range of fixed clock delays becomes narrower. At 150 MSPS, using the same logic family, the range becomes:

$6.7\text{ns} < \text{Clock Delay} < 8.0\text{ns}$

At 200 MSPS, a fixed delay can no longer be used, since

Max Clock Delay (for $T_D = T_{Dmin}$) = 6.3ns
Min Clock Delay (for $T_D = T_{Dmax}$) = 6.7ns

The user should calculate whether a fixed delay can be used in the system. If a fixed delay cannot be used, a variable delay line is needed.

VARIABLE DELAY LINE

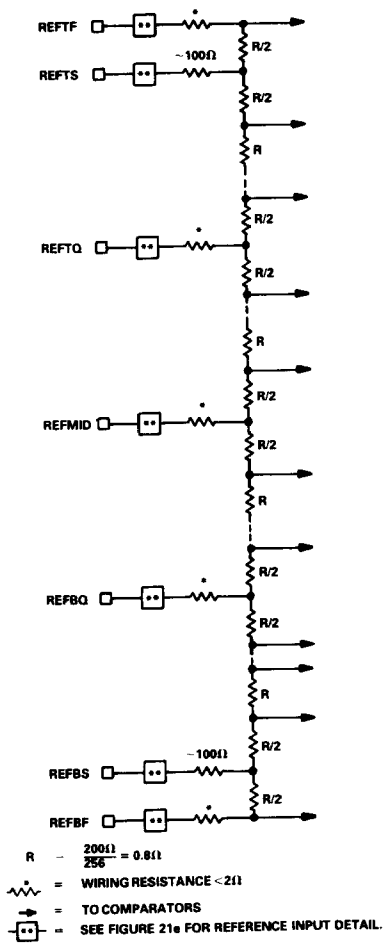
Continuing with the example above, we can determine the span of delays that is needed.

At 200 MSPS:

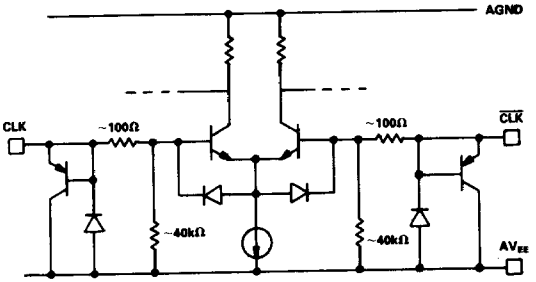
Max Clock Delay (for $T_D = T_{Dmin}$) = 6.3ns
Min Clock Delay (for $T_D = T_{Dmax}$) = 6.7ns
Data Valid Range (for each device) < 1.25ns.

The clock delay should have an adjustment range between (6.3 − 1.25/2) = 5.7ns and (6.7 + 1.25/2) = 7.3ns to center the clock edge in the middle of the Data Valid range for all devices.

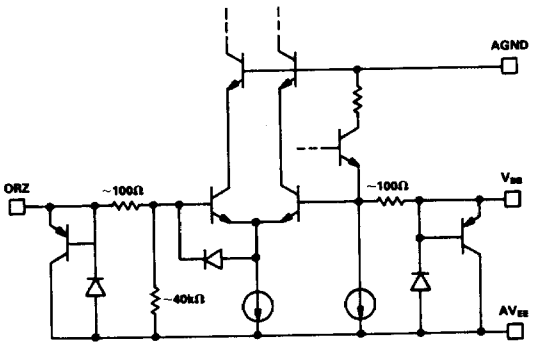
If a variable delay line is used, some means must be provided to verify that the delay is correctly set for each device. This can be done by providing a test signal synchronized to the system timing and adjusting the delay to the centerpoint of the range that gives a stable output.



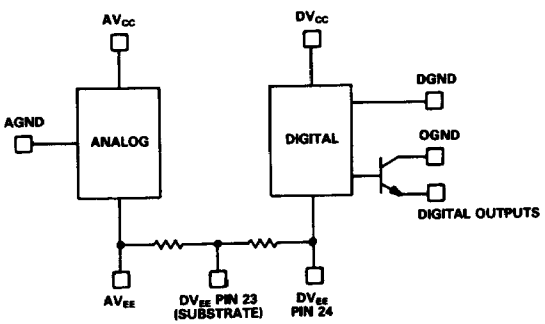
a. Reference Ladder



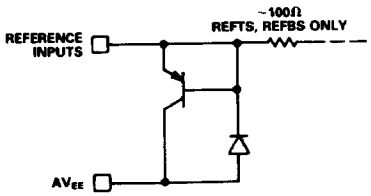
b. CLK, $\overline{CLK}$



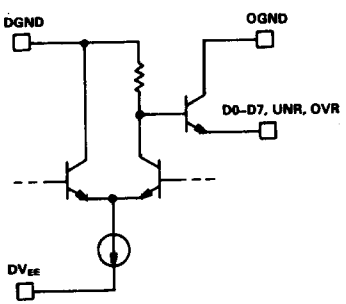
c. ORZ, V_{BB}



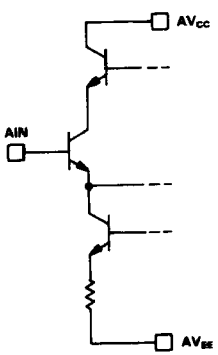
d. Internal Supply Connections



e. Reference Input Detail



f. Digital Outputs



g. Analog Input

Figure 21. Equivalent Circuits