1.1 Scope.

This specification covers the detail requirement for a signal conditioning ADC. The AD7710 is a complete analog front end for low frequency measurement applications.

1.2 Part Number.

The complete part number is:

Device	Part Number
−1	AD7710SQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip

1.3 Absolute Maximum Ratings. (T_A=+25°C unless otherwise noted)

AV_{DD} to V_{SS}	−0.3 V to +12 V
AV_{DD} to AGND	−0.3 V to +12 V
AV_{DD} to DGND	−0.3 V to +12 V
DV_{DD} to AGND	−0.3 V to +6 V
DV_{DD} to DGND	−0.3 V to +6 V
V_{SS} to AGND	+0.3 V to −6 V
V_{SS} to DGND	+0.3 V to −6 V
AGND to DGND	−0.3 V to AV_{DD} + 0.3 V
Analog Input Voltage to AGND	V_{SS} − 0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND	V_{SS} − 0.3 V to AV_{DD} + 0.3 V
REF OUT to AGND	−0.3 V to AV_{DD}
Digital Input Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Power Dissipation	
Up to +75°C	450 mW
Derates above +75°C	6 mW/°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C

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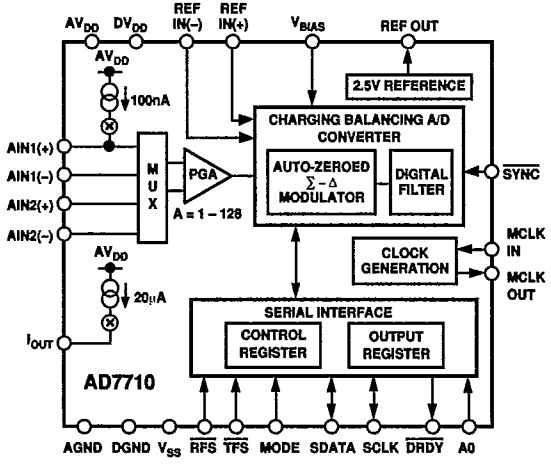
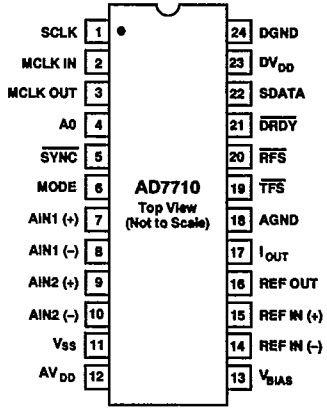
Table 1.

Test	Symbol	Device	Limits T_{MIN}	Limits T_{MAX}	Sub Groups	Test Condition	Unit
Resolution	RES	−1		21	1, 2, 3	Resolution for Which No Missing Codes Are Guaranteed	Bits
Integral Nonlinearity	INL	−1	−0.0015	+0.0015	1, 2, 3	Filter Notches ≤ 60 Hz	% of FSR
Full-Scale Drift		−1		1	13		μV/°C
Unipolar Offset Drift		−1		1	13		μV/°C
Bipolar Zero Drift		−1		1	13		μV/°C
Bipolar Negative Full-Scale Drift		−1		1	13	Excluding Reference	μV/°C
Common-Mode Rejection	CMR	−1	100		1, 2, 3	At DC	dB
50 Hz Rejection		−1	100		13	For Filter Notches of 10 Hz, 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$	dB
60 Hz Rejection		−1	100		13	For Filter Notches of 10 Hz, 30 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$	dB
DC Input Leakage Current		−1		1	13		nA
Sampling Capacitance		−1		20	13		pF
Source Impedance		−1		10	1, 2, 3		kΩ
Analog Input Unipolar Voltage Range		−1	0	V_{REF}	1, 2, 3		V
Analog Input Bipolar Voltage Range		−1	V_{REF}	V_{REF}	1, 2, 3		V
Reference Input Range		−1	2.5	5	1, 2, 3		V
Reference Output Initial Tolerance		−1	−1	+1	1, 2, 3		%
Reference Output Line Regulation		−1		1	1, 2, 3		mV/V
Reference Output Load Regulation		−1		1	1, 2, 3	Max Load Current 1 mA	mV/mA
Reference Output External Current		−1		1	1, 2, 3		mA
V_{BIAS} Input Voltage Range		−1	V_{SS} +0.85 × V_{REF}	AV_{DD} −0.85 (V_{REF})	1, 2, 3		V
Logic Input Current		−1	−10	+10	1, 2, 3		μA
All Logic Inputs (Except MCLK) Input Low Voltage	V_{INL}	−1		0.8	1, 2, 3		V
All Logic Inputs (Except MCLK) Input High Voltage	V_{INH}	−1	2.0		1, 2, 3		V
MCLK IN Only Input Low Voltage		−1		0.8	1, 2, 3		V
MCLK IN Only Input High Voltage		−1	3.5		1, 2, 3		V
Logic Outputs Low Voltage	V_{OL}	−1		0.4	1, 2, 3	I_{SINK} = 1.6 mA	V
Logic Outputs High Voltage	V_{OH}	−1	4.0		1, 2, 3	I_{SOURCE} = 100 μA	V
Floating State Leakage Current		−1	−10	+10	1, 2, 3		μA

Test	Symbol	Device	Limits T_{MIN}	Limits T_{MAX}	Sub Groups	Test Condition	Unit
Floating State Output Capacitance		−1		9	13		pF
Transducer Burn Out Initial Tolerance Compensation Output Current		−1 −1	−10	+10 20	13 1, 2, 3		% µA
Compensation Current Initial Tolerance		−1	−4	+4	1, 2, 3		µA
Compensation Current Line Regulation		−1		20	1, 2, 3		nA/V
Compensation Current Load Regulation		−1		20	1, 2, 3		nA/V
Positive Full-Scale Calibration Limit		−1		$(1.05 \times V_{REF})/GAIN$	1, 2, 3	Gain Is the Selected PGA Gain (Between 1 and 128)	V
Negative Full-Scale Calibration Limit		−1		$-(1.05 \times V_{REF})/GAIN$	1, 2, 3	Gain Is the Selected PGA Gain (Between 1 and 128)	V
Offset Calibration Limit		−1		$-(1.05 \times V_{REF})/GAIN$	1, 2, 3	Gain Is the Selected PGA Gain (Between 1 and 128)	V
Input Span		−1	$0.8 \times V_{REF}/GAIN$	$2.1 \times V_{REF}/GAIN$	1, 2, 3	Gain Is the Selected PGA Gain (Between 1 and 128)	V
Analog Supply Current		−1		3	1, 2, 3		mA
Digital Suppy Current		−1		4	1, 2, 3		mA
Negative Supply Current		−1		1.5	1, 2, 3		mA

3.2.1 Functional Block Diagram and Terminal Assignments.





3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).