

P-channel
enhancement mode MOS transistor

PHP112

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver, power management, synchronized rectifying, etc.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	n.c	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

DESCRIPTION

P-channel enhancement mode MOS transistor in an 8-pin plastic SO8 (SOT96-1) package.

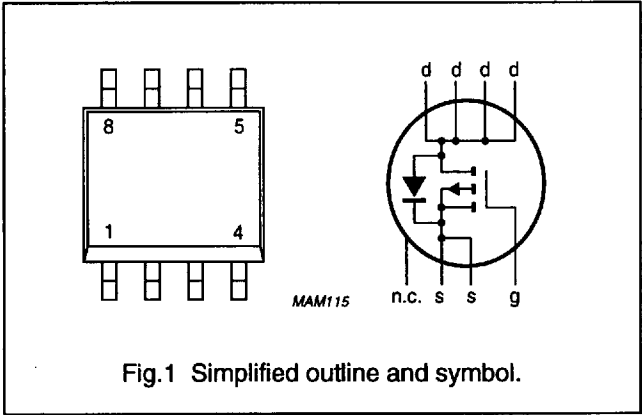


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–20	V
V_{SD}	source-drain diode forward voltage	$I_S = -1.25\text{ A}$	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	± 20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1\text{ mA}$; $V_{DS} = V_{GS}$	–1	–2.8	V
I_D	drain current (DC)		–	–3.1	A
R_{DSon}	drain-source on-state resistance	$I_D = -4\text{ A}$; $V_{GS} = -10\text{ V}$	–	0.12	Ω
P_{tot}	total power dissipation	up to $T_s = 80\text{ }^\circ\text{C}$;	–	2	W

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–20	V
V_{GSO}	gate-source voltage (DC)	open drain	–	± 20	V
I_D	drain current (DC)	$T_s \leq 80\text{ }^{\circ}\text{C}$	–	–3.1	A
I_{DM}	peak drain current	note 1	–	–14	A
P_{tot}	total power dissipation	up to $T_s = 80\text{ }^{\circ}\text{C}$	–	2	W
		up to $T_{amb} = 25\text{ }^{\circ}\text{C}$; note 2	–	2	W
		up to $T_{amb} = 25\text{ }^{\circ}\text{C}$; note 3	–	1.3	W
T_{stg}	storage temperature		–65	+150	$^{\circ}\text{C}$
T_j	operating junction temperature		–	150	$^{\circ}\text{C}$
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80\text{ }^{\circ}\text{C}$	–	–1.25	A
I_{SM}	peak pulsed source current	note 1	–	–10	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Value based on PCB with a $R_{th\text{ a-tp}}$ (ambient to tie-point) of 27.5 K/W.
3. Value based on PCB with a $R_{th\text{ a-tp}}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\text{ j-s}}$	thermal resistance from junction to soldering point	35	K/W

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CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0; I _D = -10 µA	-20	-	-	V
V _{GSth}	gate-source threshold voltage	V _{GS} = V _{DS} ; I _D = -1 mA	-1	-	-2.8	V
I _{DSS}	drain-source leakage current	V _{GS} = 0; V _{DS} = -15 V	-	-	-100	nA
I _{GSS}	gate leakage current	V _{GS} = ±20 V; V _{DS} = 0	-	-	±100	nA
I _{Don}	on-state drain current	V _{GS} = -10 V; V _{DS} = -5 V	-4.6	-	-	A
R _{DSon}	drain-source on-state resistance	V _{GS} = -4.5 V; I _D = -1 A	-	-	0.24	Ω
		V _{GS} = -10 V; I _D = -2 A	-	-	0.12	Ω
y _{fs}	forward transfer admittance	V _{DS} = -10 V; I _D = -2 A	tbf	-	-	S
C _{iss}	input capacitance	V _{GS} = 0; V _{DS} = -20 V; f = 1 MHz	-	-	tbf	pF
C _{Oss}	output capacitance	V _{GS} = 0; V _{DS} = -20 V; f = 1 MHz	-	-	tbf	pF
C _{rss}	reverse transfer capacitance	V _{GS} = 0; V _{DS} = -20 V; f = 1 MHz	-	-	tbf	pF
Q _g	total gate charge	V _{GS} = -10 V; V _{DS} = -10 V; I _D = -4 A	-	-	tbf	nC
Q _{gs}	gate-source charge	V _{GS} = -10 V; V _{DS} = -10 V; I _D = -4 A	-	-	tbf	nC
Q _{gd}	gate-drain charge	V _{GS} = -10 V; V _{DS} = -10 V; I _D = -4 A	-	-	tbf	nC
t _{on}	turn-on time	V _{GS} = 0 to -10 V; V _{DD} = -10 V; I _D = -1 A; R _L = 10 Ω	-	-	tbf	ns
t _{off}	turn-off time	V _{GS} = -10 to 0 V; V _{DD} = -10 V; I _D = -1 A; R _L = 10 Ω	-	-	tbf	ns
Source-drain diode						
V _{SD}	source drain diode forward voltage	V _{GS} = 0; I _S = -1.25 A	-	-	-1.6	V
t _{rr}	reverse recovery time	I _S = -1.25 A; di/dt = 100 A/µs	-	-	tbf	ns

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PACKAGE OUTLINE

