PERICOM

PI2C3000

# Token Ring Active Hub Chip

## Product Features:

- Complete physical layer interface for 4Mbps or 16Mbps Token Ring Active Concentrator applications
- Active retiming for each lobe port or Ring In/Out port for extended STP/UTP cabling
- Phantom voltage detection/generation for lobe port insertion and Ring In/Out port insertion
- Lobe bypass mechanism eliminating the need for relays
- Constant gain PLL design
- Selectable 4Mbps or 16Mbps data rate
- Receiver adaptive equalization to minimize data dependent correlated jitter
- Automatic Speed Detection During Lobe Test
- Energy Detect circuit for detection of valid received signals
- Selectable Jitter Attenuator PLL with auto centering elastic buffer for reduction of accumulated phase slope
- LED drivers for diagnostic status display
- 48-pin SSOP package
- Advanced 0.8μm BiCMOS technology

## Product Description:

The Pericom Semiconductor's Token Ring Active Hub chip is designed for IEEE 802.5 compliant Token Ring Active Concentrators. It provides signal retiming and conditioning for extended STP and UTP transmission media. It includes a receive adaptive equalizer, speed/energy detect circuit, a line driver, a phantom voltage detector/generator for lobe port and Ring In/Out insertion, and a retiming PLL. It also includes a lobe bypass mechanism, a jitter attenuator PLL with elastic buffer, and LED drivers for status display. It has speed select and jitter attenuator select.

### Receiver Section

The receiver section consists of the receiver equalizer, the energy detect circuit, and the retiming PLL. The receive equalizer is a two state adaptive equalizer. It operates in nonlinear region for large signals (short cable) thereby effectively disabling the equalization, and it operates in linear region for small signals (long cable) providing amplification for higher frequency signal components. External RC components are required to set the filtering characteristics of the equalizer. The Speed/Energy Detect Circuit checks for the transition density of the incoming signal. The speed is automatically determined during lobe test. When the required transition density is met, a signal valid indication is given to the retiming PLL so that the PLL can lock on to the incoming signal. The retiming PLL is frequency-locked to the local crystal in the absence of valid received signal. The retiming PLL bandwidth is set by an external loop filter.

### Retiming PLL Characteristics

| | 4Mbps | 16Mbps | |
|---|---|---|---|
| PLL Bandwidth | 90KHz | 360KHz | typ |
| Jitter Tolerance | 2.0ns/UI | 0.50ns/UI | min |
| Accu. Phase Slope | 1.0ns/UI | 0.25ns/UI | max |
| Static Alignment | — | 1ns | max |
| Phase Slope Overshoot | — | TBD | max |
| Mean Correlated Jitter | — | 2ns | max |

### Line Driver

The line driver takes the transmit clock and differential Manchester data of the upstream station and drives the cable in the normal lobe-inserted state. It takes the received clock and data from the retiming PLL during lobe test (prior to lobe insertion). The line driver is idle (no data transitions) in the absence of valid received signal or phantom voltage.

### Phantom Detector/Generation and Lobe Bypass

The phantom detector senses for the DC phantom voltage generated by the lobe station. The phantom voltage generated by the station is an indication to the concentrator that the station wants to be inserted in the ring. In the absence of phantom voltage, the lobe bypass circuit is in the lobe bypass state and the retiming PLL output is routed to the line driver for lobe test purposes. Upon receipt of the phantom voltage, transmit clock and data (TxC and TxD) of the upstream station are routed to the line driver, and the received clock and data (RxC and RxD) of the lobe station are routed to the downstream station.

For hub interconnection, the Ring Out port of the first hub generates the phantom voltage and the Ring In port of the second hub detects the phantom voltage in a similar manner that a lobe station is inserted in the ring. A wire good indication is provided in the Ring Out port of the first hub, and a phantom detect indication is provided in the Ring In port of the second hub to validate the integrity of the connection.

### Jitter Attenuator PLL

The jitter attenuator PLL is an extremely low bandwidth PLL to attenuate the phase slope of the incoming signal. A 32 bit (64 clocks) elastic buffer is provided to accommodate the accumulated phase jitter in the ring. The recovered clock from the retiming PLL is used to clock the recovered data into the elastic buffer, and the dejittered recovered clock from the jitter attenuator PLL is used to clock the recovered data out of the elastic buffer. The elastic buffer is autocentering and does not rely on the Token for recentering.

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### LED Drivers and Control Logic

The LED drivers provide status for the following signals: Phantom Detect for Ring In (phantom detect enabled), valid received signal, PLL phase-locked, and Wire Good for Ring Out (phantom generate enabled). The Control Logic sets the speed of the retiming PLL and the selection of the Jitter Attenuator.

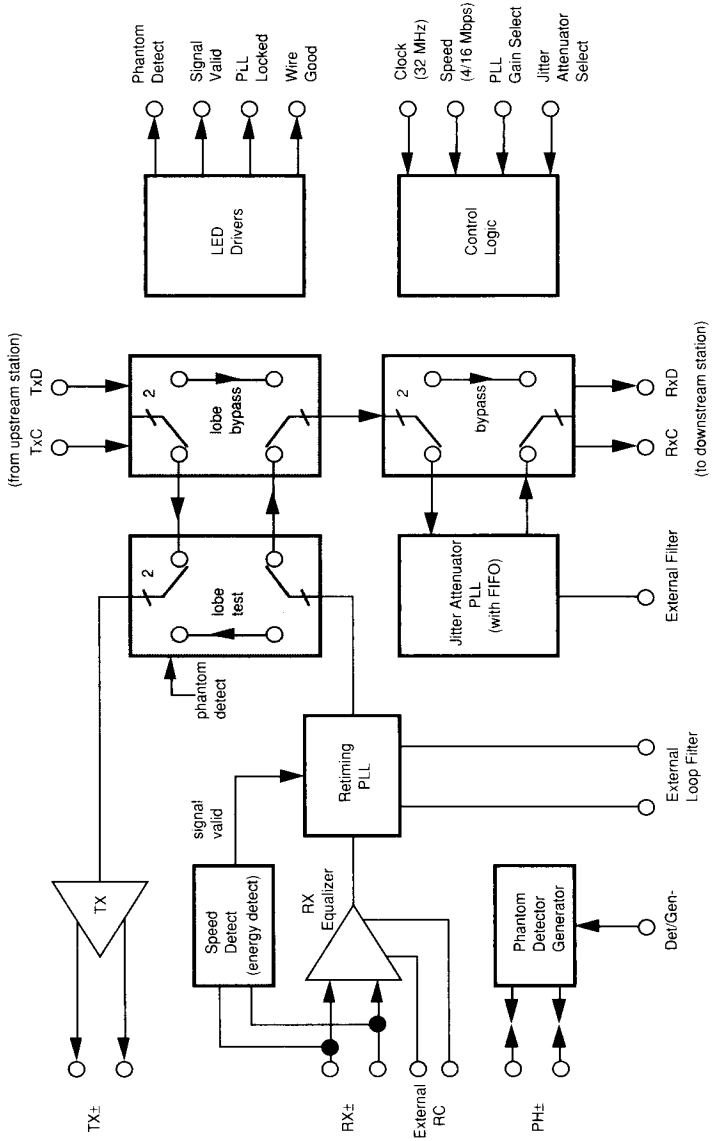


**Fig 1. Token Ring Active Hub Chip**

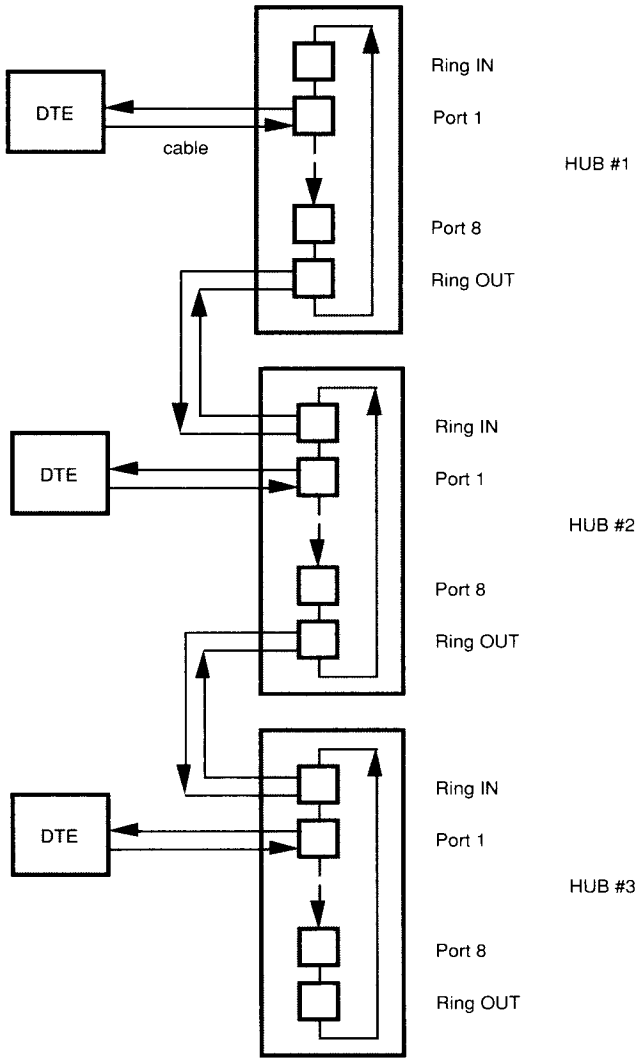


**Fig 2. Token Ring Active Hub Chip**
**Typical Hub Application**