



LC²MOS

16-Bit D/A Converter

ANALOG DEVICES INC

AD7846

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 16-bit, voltage output, multiplying DAC, with a readback facility.

1.2 Part Number.

The complete part number is as follows:

Device	Part Number
-1	AD7846S(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin Side-Brazed Ceramic
E	E-28A	28-Terminal Leadless Ceramic Chip Carrier

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to DGND	-0.3 V to +17 V
V_{CC} to DGND	-0.3 V to +7 V
V_{SS} to DGND	+3 V to -17 V
V_{REF+} to DGND	± 25 V
V_{REF-} to DGND	± 25 V
V_{OUT} to DGND ¹	± 25 V
R_{IN} to DGND	± 25 V
Digital Input Voltage to DGND	-0.3 V to V_{CC} to +0.3 V
Digital Output Voltage to DGND	-0.3 V to V_{CC} to +0.3 V
Power Dissipation (Any Package)	
to +75°C	1000 mW
Derates Above +75°C	10 mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

NOTE

¹ V_{OUT} may be shorted to DGND, V_{DD} , V_{SS} , V_{CC} provided that the power dissipation of the package is not exceeded.

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for D-28 and E-28A
 $\theta_{JA} = 120^\circ\text{C/W}$ for D-28 and E-28A

Table 1.

Test	Symbol	Device	Design Limits $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 7, 8	Sub Group 9	Sub Group 10, 11	Sub Group 13, 14, 15	Test Condition ¹	Units
Relative Accuracy	R_A	1, 2	16	16	16					Unipolar Output ²	$\pm$ LSB
Differential Nonlinearity ³	DNL	1, 2	1	1	1						$\pm$ LSB
Gain Error ⁴	A_E	1, 2	16	16	24						$\pm$ LSB
Offset Error	O_E	1, 2	16	16	24						$\pm$ LSB
Relative Accuracy	R_A	1, 2	8	8	8					Bipolar Output ⁵	$\pm$ LSB
Differential Nonlinearity ³	DNL	1, 2	1	1	1						$\pm$ LSB
Gain Error ⁴	A_E	1, 2	8	16	16						$\pm$ LSB
Offset Error	O_E	1, 2	8	16	16						$\pm$ LSB
Bipolar Zero Error	BIP _E	1, 2	8	16	16						$\pm$ LSB
Reference Input Resistance	V_{REFIN}	1, 2	20/40	20/40	20/40					Resistance from V_{REF-} to V_{REF+}	k Ω min/ max
V_{REF+} Range	V_{REF+}	1, 2	6					6			$\pm$ V
V_{REF-} Range	V_{REF-}	1, 2	6					6			$\pm$ V
Output Voltage Swing	V_{SWING}	1, 2	+4					+4	$V_{SS} + 4.0$		V
			-3					-3	$V_{DD} - 3.0$		
Input Voltage High Level	V_{IH}	1, 2	2.4	2.4	2.4						V
Input Voltage Low Level	V_{IL}	1, 2	0.8	0.8	0.8						V
Logical Input Current	I_{IN}	1, 2	10	10	10						$\pm\mu$ A
Logical Input Capacitance	C_{IN}	1, 2	10					10			pF max
Output Voltage High Level	V_{OH}	1, 2	4.0	4.0	4.0				$I_{SOURCE} = 400 \mu A$		V min
Output Voltage Low Level	V_{OL}	1, 2	0.4	0.4	0.4				$I_{SINK} = 1.6 \text{ mA}$		V max
Floating State Leakage Current		1, 2	10	10	10					DB0-DB15 = 0 to V_{CC}	$\pm\mu$ A
Floating State Output Capacitance		1, 2	10					10			pF max
Positive Power Supply Current	I_{DD}	1, 2	5	5	5				V_{OUT} Unloaded ⁶		mA max
Negative Power Supply Current	I_{SS}	1, 2	5	5	5						mA max
Positive Logic Supply Current	I_{CC}	1, 2	1	1	1						mA max
Power Supply Sensitivity ⁷	PSS	1, 2	2	2	2						LSB/V
Functional Test R/W to CS Setup Time	t_1	1, 2	50				40	50		See Figure 2 ⁸	ns
CS Pulse Width (Write Cycle)	t_2	1, 2	140				150	190			ns
R/W to CS Hold Time	t_3	1, 2	50				40	50			ns
Data Setup Time	t_4	1, 2	120				110	120			ns
Data Hold Time	t_5	1, 2	0				0	0			ns
Data Access Time ⁹	t_6	1, 2	320				230	320			ns
Bus Relinquish ¹⁰	t_7	1, 2	90				80	90			ns
CLR Setup Time	t_8	1, 2	20				20	20		See Figure 2	ns
CLR Pulse Width	t_9	1, 2	150				150	150			ns
CLR Hold Time	t_{10}	1, 2	0				0	0			ns
LDAC Pulse Width	t_{11}	1, 2	100				80	100			ns
CS Pulse Width (Read Cycle)	t_{12}	1, 2	330				240	330			ns

NOTES

¹Unless otherwise specified, 14.25 V dc $\leq V_{DD} \leq 15.75$ V dc, -14.25 V dc $\leq V_{SS} \leq -15.75$ V dc and 4.75 V dc $\leq V_{CC} \leq 5.25$ V dc. V_{OUT} loaded with 3 k Ω , 1000 pF to 0 V. $V_{REF+} = 5.0$ V dc. R_{IN} connected to 0 V. Parameters in subgroups 13, 14 15 are characterized at the initial design stage and after any subsequent redesigns.

² $V_{REF} = 0\text{ V}$, $V_{OUT} = 0\text{ V to } 10\text{ V}$, 1 LSB = 153 μV .³Monotonicity is guaranteed over full temperature range.⁴V_{OUT} load = 10 MΩ.⁵ $V_{\text{REF}} = -5.0 \text{ V}$, $V_{\text{OUT}} = -10 \text{ V}$ to $+10 \text{ V}$, 1 LSB = 305 μV .

⁶The device is functional with a power supply of ± 12 V.

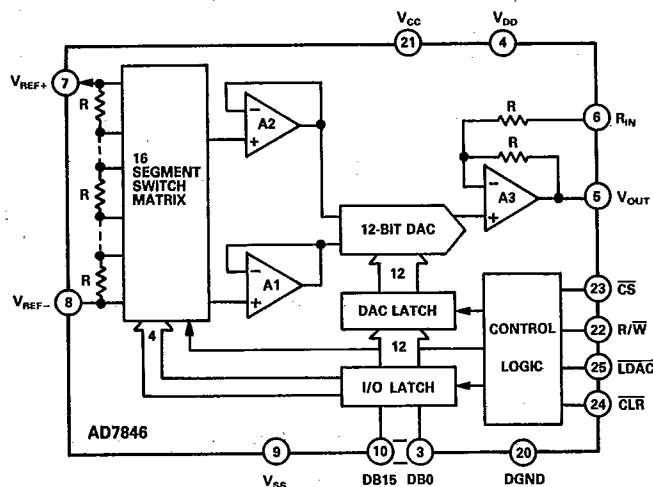
⁷Sensitivity of gain error, offset error and bipolar zero error to V_{DD} , V_{SS} variations.

*All input control signals are specified with $t_R = t_F = 5.0$ ns (10% to 90% of +5.0 V) and timed from a voltage level of 1.6 V.

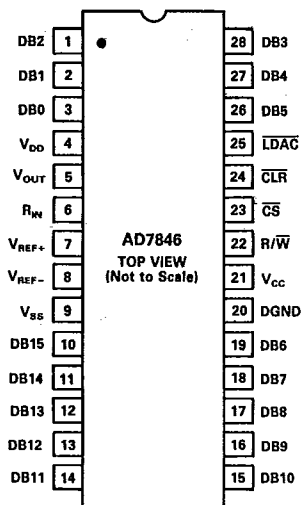
⁹ t_r is measured with the load circuits of Figure 1a and defined as the time required for an output to cross 0.8 V or 2.4 V.

¹⁰ t_2 is defined as the time required for an output to change 0.5 V when loaded with the circuits of Figure 1b.

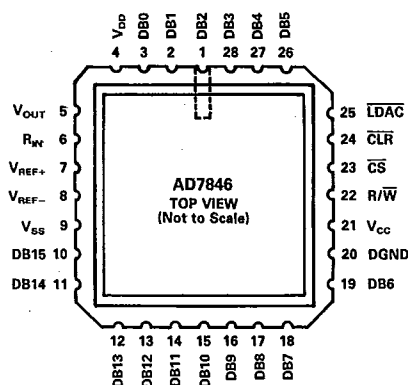
3.2.1 Functional Block Diagram and Terminal Assignments.



D Package (DIP)



E Package (LCC)



Terminal Connections

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Device Type Case Outline Terminal Number	01 X Terminal Symbol	Device Type Case Outline Terminal Number	01 X Terminal Symbol
1	DB2	15	DB10
2	DB1	16	DB9
3	DB0	17	DB8
4	V _{DD}	18	DB7
5	V _{OUT}	19	DB6
6	R _{IN}	20	DGND
7	V _{REF} ⁺	21	V _{CC}
8	V _{REF} ⁻	22	R/ $\overline{W}$
9	V _{SS}	23	$\overline{CS}$
10	DB15	24	$\overline{CLR}$
11	DB14	25	$\overline{LDAC}$
12	DB13	26	DB5
13	DB12	27	DB4
14	DB11	28	DB3

Pin Descriptions

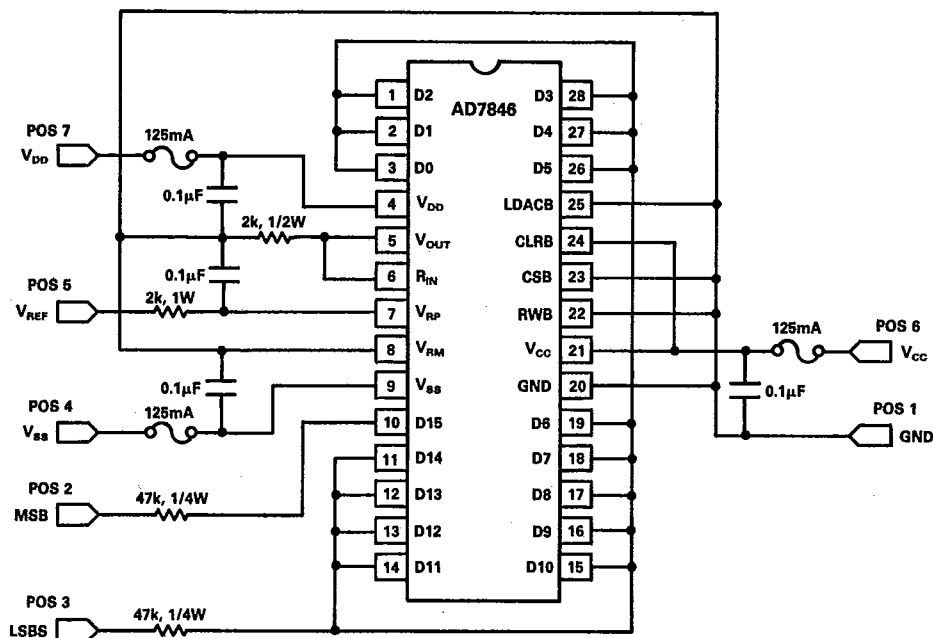
Pin	Description
DB2-DB0	Data I/O pins. DB0 is LSB.
V _{DD}	Positive supply for analog circuitry. This is a +15 V nominal.
V _{OUT}	DAC output voltage pin.
R _{IN}	Input to summing resistor of DAC output amplifier. This is used to select output voltage ranges. See Tables 2 and 3.
V _{REF} ⁺	V _{REF} ⁺ input. The DAC is specified for V _{REF} ⁺ = 5.0 V.
V _{REF} ⁻	V _{REF} ⁻ input. For unipolar operation connect it to -5.0 V. The device is specified for both conditions.
V _{SS}	Negative supply for analog circuitry. This is -15 V nominal.
DB15-DB6	Data I/O pins. DB15 is MSB.
DGND	Ground pin for logic circuitry.
V _{CC}	Positive supply for logic circuitry. This is +5.0 V nominal.
R/ $\overline{W}$	R/ $\overline{W}$ input. This can be used to load data to the DAC or read back the DAC latch contents.
$\overline{CS}$	Chip select input. This selects the device.
$\overline{CLR}$	Clear input. The DAC can be cleared to 000 . . . 000 or 100 . . . 000. See Tables 2 and 3.
$\overline{LDAC}$	Asynchronous load input to DAC.
DB5-DB3	Data I/O pins.

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

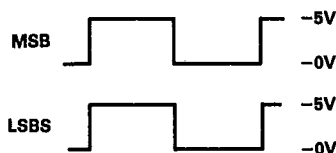
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



- Each AD7846 socket has associated with it the four resistors shown, four 0.1 μ F ceramic type capacitors and three 125 mA pico fuses.
- Each burn-in board has the following seven external signals supplied:

Signal	Voltage
V_{DD}	+15 V
V_{REF}	+0 V
V_{CC}	+5 V
GND	0 V
V_{SS}	-15 V
MSB	See Below
LSBs	See Below

- For static burn-in MSB and LSBs are both tied to +5 V.
- For dynamic burn-in MSB and LSBs are driven with 20 kHz square waves as shown:



5. For static burn-in and power-up sequences is

1. V_{DD}
2. V_{SS}
3. V_{CC} , MSB, LSBs (together)
4. V_{REF}

6. For dynamic burn-in the power sequence is

1. V_{DD}
2. V_{SS}
3. V_{CC}
4. MSB, LSBs (together)
5. V_{REF}

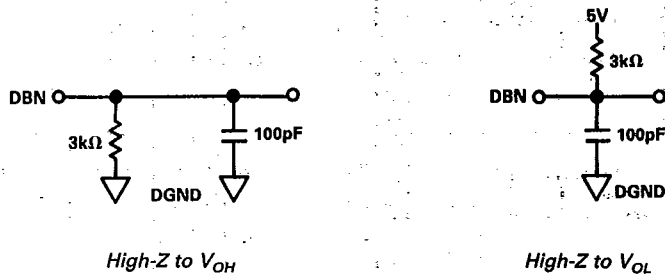


Figure 1a. Load Circuits for Access Time (t_a)

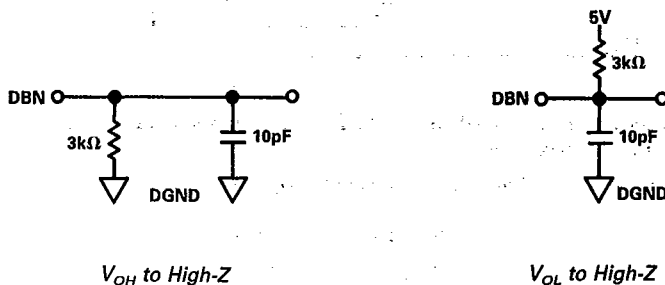


Figure 1b. Load Circuits for Bus Relinquish Time (t_r)

Figure 1. Load Circuits

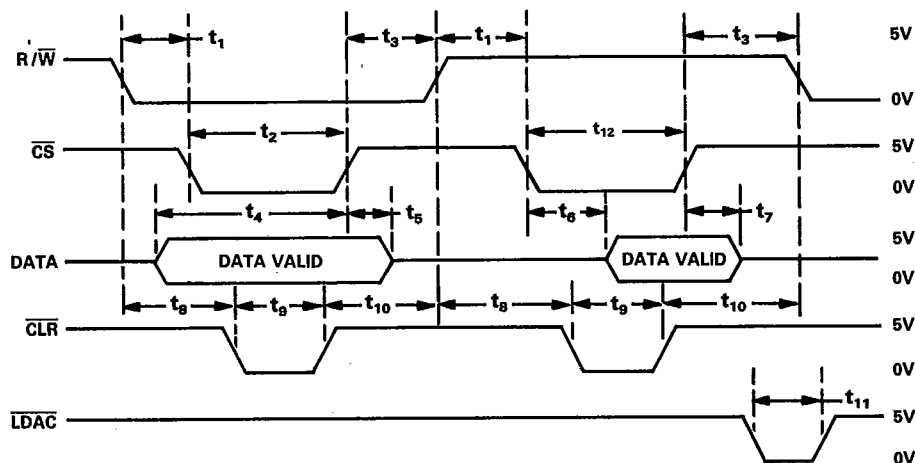


Figure 2. Switching Characteristics

Table 2. Truth Table

$\overline{CS}$	$\overline{R/W}$	$\overline{LDAC}$	$\overline{CLR}$	Function
1	X	X	X	3-State DAC I/O Latch in High Z-State
0	0	X	X	DAC I/O Latch Loaded with DB15-DB0
0	1	X	X	Contents of DAC I/O Latch Available on DB15-DB0
X	X	0	1	Contents of DAC I/O Latch Transferred to DAC Latch
X	0	X	0	DAC Latch Loaded with 000 . . . 000
X	1	X	0	DAC Latch Loaded with 100 . . . 000

0 = Low
 1 = High
 X = Don't Care

Table 3. Output Voltage Ranges

Output Range	V_{REF+}	V_{REF-}	R_{IN}
0 V to +5 V	+5 V	0 V	V_{OUT}
0 V to +10 V	+5 V	0 V	0 V
+5 V to -5 V	+5 V	-5 V	V_{OUT}
+5 V to -5 V	+5 V	+5 V	+5 V
+10 V to -10 V	+5 V	-5 V	0 V