LC²MOS 4-Channel, 12-Bit Simultaneous Sampling Data Acquisition System

AD7874

1.1 Scope.

This specification covers the detail requirement for a 12-bit data acquisition system that contains a high speed 12-bit ADC, on-chip reference, on-chip clock and four track/hold amplifiers. Track/hold acquisition time is 2 μs and the conversion time per channel is 8 μs, allowing 29 kHz sample rate for all four channels.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD7874S(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-28	28-Pin Cerdip
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Positive Supply Voltage Range (V_{DD}) to AGND ..... −0.3 V dc to +7.0 V dc
Positive Supply Voltage Range (V_{DD}) to DGND ..... −0.3 V dc to +7.0 V dc
Negative Supply Voltage Range (V_{SS}) to AGND ..... +0.3 V dc to −7.0 V dc
AGND to DGND ..... −0.3 V dc to V_{DD} + 0.3 V dc
Analog Input Range (V_{IN}) ..... −15.0 V dc to +15.0 V dc
Voltage Reference Output (REF OUT) to Analog Ground Range (AGND) ..... 0 V dc to V_{DD}
Logic Input Voltage Range ..... −0.3 V dc to V_{DD} + 0.3 V dc
Logic Output Voltage Range ..... −0.3 V dc to V_{DD} + 0.3 V dc
Maximum Power Dissipation ..... 1000 mW
Lead Temperature (Soldering 10 sec) ..... +300°C
Storage Temperature Range ..... −65°C to +150°C

1.4 Recommended Operating Conditions.

Positive Supply Voltage Range (V_{DD}) ..... +4.75 V dc to +5.25 V dc
Negative Supply Voltage Range (V_{SS}) ..... −4.75 V dc to −5.25 V dc
Analog Input Voltage Range ..... −10.0 V dc to +10.0 V dc
Ambient Operating Temperature Range ..... −55°C to +125°C
Reference Input Voltage Range (V_{IN}) ..... +2.85 V dc to +3.15 V dc

AD7874—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Limits[2] Min	Limits[2] Max	Sub Groups	Test Conditions[1] ($-55°C \le T_A \le +125°C$ $+4.75\ V \le V_{DD} \le +5.25\ V$, $-5.25\ V \le V_{SS} \le -4.75$ unless otherwise noted)	Unit
Acquisition Time to 0.01%[3, 4]	t_{ACQ}	−1		2.0	9, 10, 11	See Timing Diagram	μs
Aperture Delay	t_{AU}	−1	0	40	9, 10, 11		ns
Aperture Delay Matching	ADM	−1		4.0	9, 10, 11		ns
Signal-to-Noise Ratio	SNR	−1	70		1, 2, 3	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 29 kHz	dB
Total Harmonic Distortion	THD	−1		−78	1, 2, 3		dB
Peak Harmonic	PH	−1		−78	1, 2, 3		dB
Intermodulation Distortion 2nd Order Terms	IMD2	−1		−78	1, 2, 3		dB
3rd Order Terms	IMD3			−78			
Channel-to-Channel Isolation	ISO	−1		−78			dB
Relative Accuracy[4]	INL	−1		±1	1, 2, 3		LSB
Differential Nonlinearity[4]	DNL	−1		±1	1, 2, 3	No Missing Codes Guaranteed	LSB
Positive Full-Scale Error[5]	PFSE	−1		±5	1, 2, 3	Any Channel	LSB
Negative Full-Scale Error[5]	NFSE	−1		±5	1, 2, 3	Any Channel	LSB
Full-Scale Error Match	FSEM	−1		5	1, 2, 3	Between Channels	LSB
Bipolar Zero Error	BZE	−1		±5	1, 2, 3	Any Channel	LSB
Bipolar Zero Error Match	BZEM	−1		4	1, 2, 3	Between Channels	LSB
Analog Input Current	AIN	−1		±600	1, 2, 3		μA
Reference Output Voltage Error[6]	ROVE	−1		±0.33	1		%
				±1.0	2, 3		
Reference Output Load Change	ROLC	−1		±2.0	1, 2, 3	Reference Load Current Change (0 μA–500 μA)	mV
Reference Input Current	RIC	−1		±1.0	1, 2, 3	V_{REF} = +3 V	μA
Reference Input Capacitance	C_{REF}	−1		10	4	T_A = ±25°C	pF
High Level Logic Input Voltage[7]	V_{INH}	−1	2.4		7, 8	See Note 7	V
Low Level Logic Input Voltage[7]	V_{INL}	−1		0.8	7, 8	See Note 7	V
Logic Input Current	I_{IN}	−1		±10	1, 2, 3	V_{IN} = 0 V to V_{DD}, V_{DD} = +5.2 V, V_{SS} = −5.2 V	μA
Logic Input Capacitance	C_{IN}	−1		10	4	T_A = ±25°C	pF
High Level Logic Output Voltage	V_{OH}	−1	4.0		1, 2, 3		V
Low Level Logic Output Voltage	V_{OL}	−1		0.4	1, 2, 3		V
Logic Output Floating-State Leakage Current	LOFSLC	−1		±10	1, 2, 3	V_{IN} = 0 V to V_{DD}; DB0–DB11, V_{DD} = +5.25 V, V_{SS} = −5.25 V	μA
Logic Output Floating-State Output Capacitance	C_{OUT}	−1		10	4	T_A = +25°C	pF
Positive Supply Current	I_{DD}	−1		18	1, 2, 3	$\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = +5.0 V	mA
Negative Supply Current	I_{SS}	−1		12	1, 2, 3	$\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = +5.0 V	mA
Power Dissipation	P_D	−1		150	1, 2, 3	V_{DD} = +5 V, V_{SS} = −5 V	mW
$\overline{CONVST}$ Pulse Width	t_1	−1	50		9	T_A = +25°C[8, 9]	ns
$\overline{CS}$ to $\overline{RD}$ Setup	t_2	−1	0		9	T_A = +25°C[8, 9]	ns
$\overline{RD}$ Pulse Width	t_3	−1	70		9, 10, 11		ns
$\overline{CS}$ to $\overline{RD}$ Hold	t_4	−1	0		9	T_A = +25°C[8, 9]	ns

Test	Symbol	Device	Limits[2] Min	Max	Sub Groups	Test Conditions[1] (−55°C ≤ T_A ≤ +125°C +4.75 V ≤ V_{DD} ≤ +5.25 V, −5.25 V ≤ V_{SS} ≤ −4.75 unless otherwise noted)	Unit
$\overline{RD}$ to $\overline{INT}$ Delay	t_5	−1		60	9	T_A = +25°C[8, 9]	ns
Data Access Time after $\overline{RD}$	t_6	−1	70		9, 10, 11	See Notes 8 and 10	ns
Bus Relinquish Time after $\overline{RD}$	t_7	−1	5	50	9, 10, 11	See Notes 8 and 11	ns
Delay Time Between Reads	t_8	−1	150		9	T_A = +25°C[8, 9]	ns
$\overline{CONVST}$ to $\overline{INT}$, External Clock = 2.5 MHz	t_{CONV}	−1	31.0	32.5	9	T_A = +25°C[8, 9]	µs
$\overline{CONVST}$ to $\overline{INT}$, Internal Clock	t_{CONV}	−1	31.0	35.0	9	T_A = +25°C[8, 9]	µs
Minimum Input Clock Period	t_{CLK}	−1		10	9	T_A = +25°C[8, 9]	µs

NOTES

[1] V_{REF} = +3 V, AGND = DGND = 0 V. All tests are guaranteed over a supply voltage range of V_{DD} = 5 V ± 5%, V_{SS} = −5 V ± 5%; however, all measurements are made at V_{DD} = +4.75 V, V_{SS} = −4.75 V unless otherwise specified.

[2] The limiting terms "min" (minimum) and "max" (maximum) shall be considered to apply to magnitudes only. Negative current shall be defined as conventional current flow out of a device terminal.

[3] S/H acquisition time is tested by performing an FFT test using an acquisition time equal to the test limit value. This same test is used to determine SNR and THD. Acquisition time is guaranteed by an SNR value which meets the test limit for that specification.

[4] Tested on one channel only. The channel used for testing is that which shows the worst performance in device characterization.

[5] Measured with respect to REF IN voltage and includes bipolar offset error.

[6] For capacitive loads greater than 50 pF, a series resistor is required.

[7] These tests are performed by using the test limits as setup conditions. Part functionality guarantees that the tested parameters meet specification.

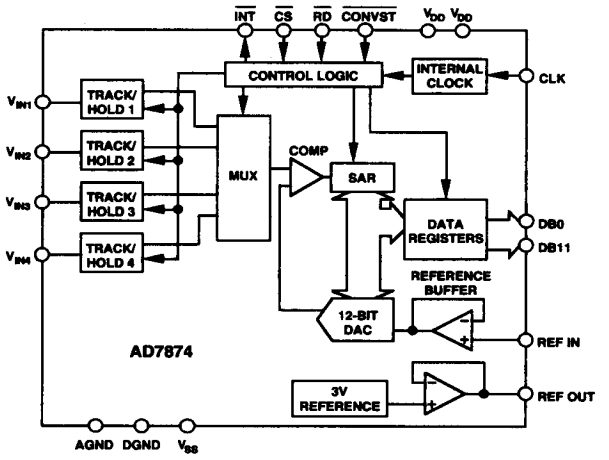
[8] All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[9] Measured only for initial qualification and after any process or design changes which may affect these parameters.

[10] t_6 is measured with the load circuit of Figure 4 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[11] t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7 quoted in the timing characteristics, is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

4.2.1 Life Test/Burn-In Circuit

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

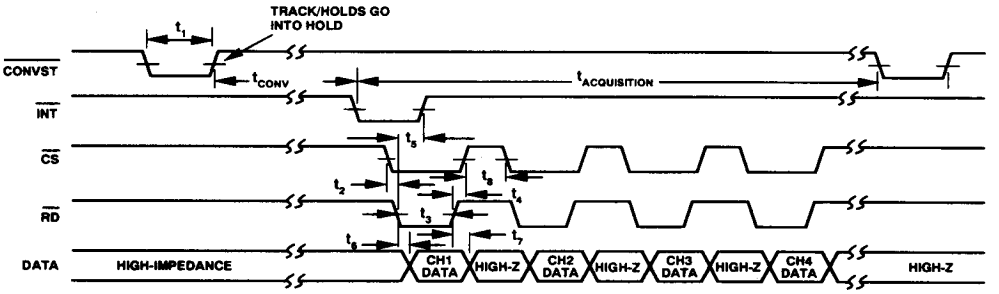


Figure 1. Timing Diagram