

1-10 Clock Buffer for Networking Applications

Product Features

- High Frequency >150 MHz
- High-speed, low-noise, non-inverting 1-10 buffer
- Low-skew (<150ps) between any two output clocks
- Low duty cycle distortion <300ps
- Low propagation delay <3.5ns
- Multiple V_{DD}, GND pins for noise reduction
- 2.5V supply voltage
- Available in SOIC, SSOP, and QSOP packages

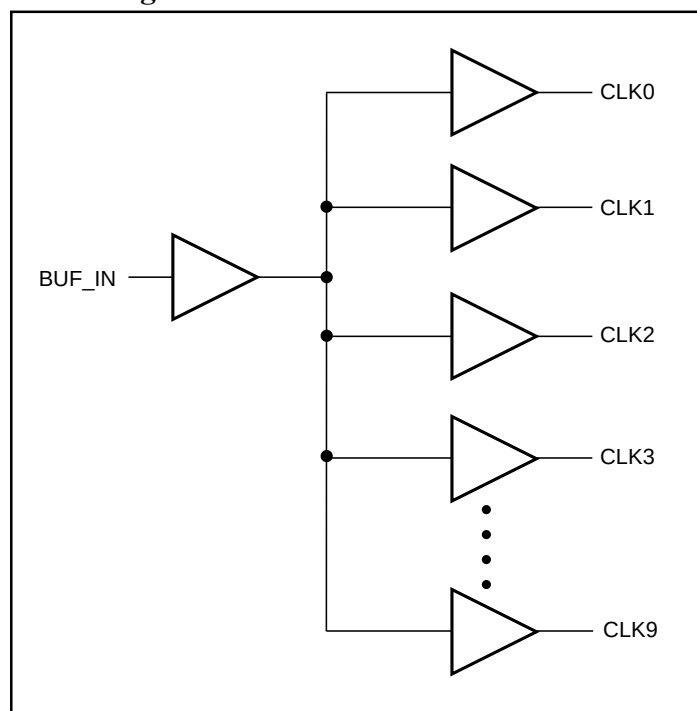
Description

The PI49FCT20807, a 2.5V compatible, high-speed, low-noise 1-10 non-inverting clock buffer, is designed to target networking applications that require low-skew, low-jitter, and high-frequency clock distribution. Providing output-to-output skew as low as 150ps, the PI49FCT20807 is an ideal clock distribution device for synchronous systems. Designing synchronous networking systems requires a tight level of skew from a large number of outputs.

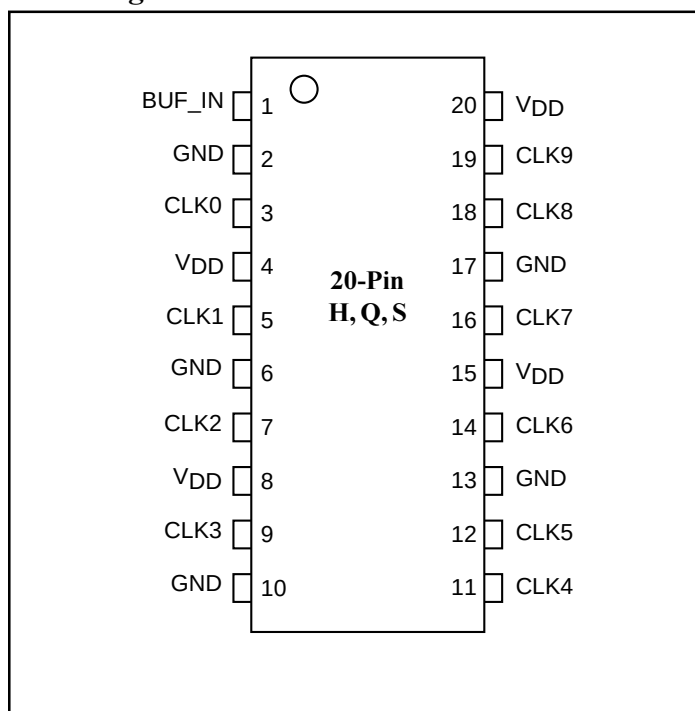
Product Pin Description

Pin Name	Description
BUF_IN	Input
CLK [0:9]	Outputs
GND	Ground
V _{DD}	Power

Block Diagram



Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
V _{DD} Voltage	–0.5V to +3.6V
Output Voltage ⁽⁴⁾	–0.5V to V _{DD} +0.5V
Input Voltage ⁽⁴⁾	–0.5V to V _{DD} +0.5V
DC Output Current	–60mA to +60mA
Power Dissipation	500mW

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

V _{DD} Voltage	2.5V ± 0.2V
Industrial Temperature	–40°C to +85°C
Input Frequency	DC to 150 MHz
Capacitive Loading	10pF to 25pF

DC Electrical Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level (Input Pins)		1.7	—		V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level (Input Pins)			—	0.7	
I _I	Input Current	V _{DD} = Max., V _{IN} = V _{DD} or GND	V _{IN} = V _{DD}	—	—	±1	mA
V _{IK}	Clamp Diode Voltage	V _{DD} = Min., I _{IN} = –18mA		—	–0.7	–1	V
V _{OH}	Output HIGH Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = –1mA	2	—	—	
			I _{OH} = –8mA	1.8 ⁽³⁾	—	—	
V _{OL}	Output LOW Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 1mA	—	—	0.4	
			I _{OL} = 8mA	—	—	0.6	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{DD} = 2.5V, +25°C ambient and maximum loading.
- V_{OH} = V_{DD} – 0.6V at rated current.
- This value is limited to 3.6V maximum.

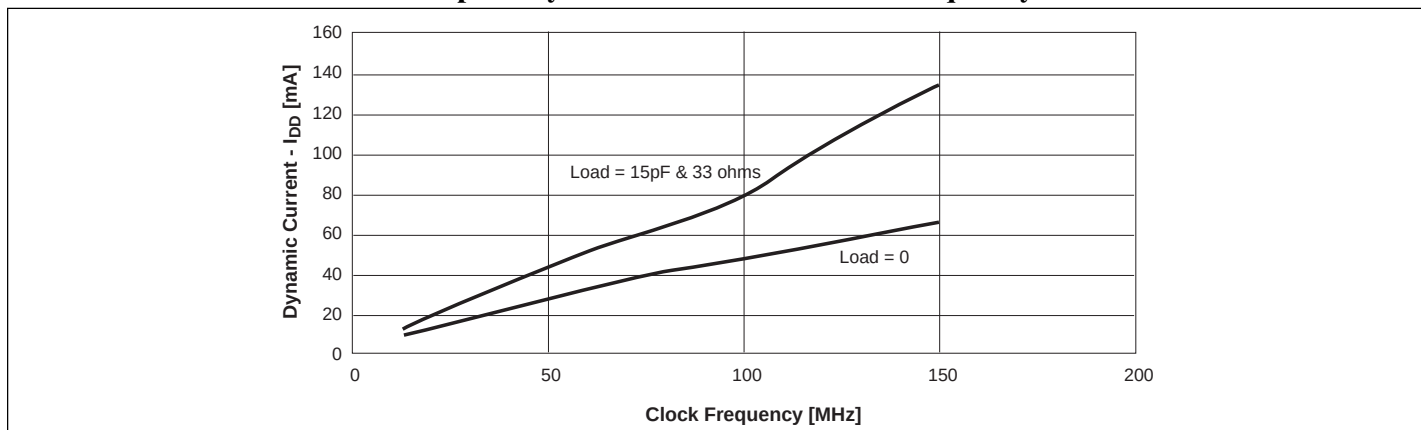
Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
I _{DDQ}	Quiescent Power Supply Current	V _{DD} = Max.	V _{IN} = GND or V _{DD}	—	0.1	20	μA
ΔI _{DD}	Supply Current per Inputs @ TTL HIGH	V _{DD} = Max.	V _{IN} = V _{DD} – 0.6V ⁽³⁾	—	47	300	
I _{DD}	Dynamic Supply Current (See Graph 1)	V _{DD} = 2.7V, 15pF & 33-ohm load	150 MHz	—	136	—	mA

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{DD} = 2.5V, +25°C ambient.
- Per TTL driven input (V_{IN} = V_{DD} – 0.6V); all other inputs at V_{DD} or GND.

Graph 1. Dynamic Current vs. Clock Frequency



Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameters ⁽¹⁾	Description	Test Conditions	Typ ⁽⁵⁾	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	3	4	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$		6	

Note:

1. This parameter is determined by device characterization but is not production tested.

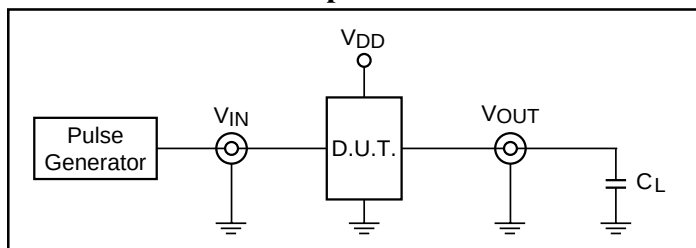
Switching Characteristics ($V_{DD} = 2.5\text{V} \pm 0.2\text{V}$, $T_A = 85^\circ\text{C}$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ.	Max.	Units
t_R/t_F	CLKn Rise/Fall Time 0.7V ~ 1.7 V	$C_L = 22\text{pF}$, 100 MHz	—	1.0	1.25	ns
		$C_L = 12\text{pF}$, 150 MHz	—	1.0	1.2	
t_{PLH} t_{PHL}	Propagation Delay BUF_IN to CLKn	$C_L = 22\text{pF}$, 100 MHz	—	3.0	3.5	
		$C_L = 12\text{pF}$, 150 MHz	—	2.4	2.7	
$t_{SK(o)}^{(2)}$	Skew between two outputs of the same package (same transition)	$C_L = 22\text{pF}$, 100 MHz	—	100	150	ps
		$C_L = 12\text{pF}$, 150 MHz	—	100	150	
$t_{SK(p)}^{(2)}$	Skew between opposite transitions ($t_{PHL} - t_{PLH}$) of the same output	$C_L = 22\text{pF}$, 100 MHz	—	250	300	
		$C_L = 12\text{pF}$, 150 MHz	—	250	300	
$t_{SK(t)}^{(2)}$	Skew between two outputs of different package ⁽⁴⁾	$C_L = 12\text{pF}$, 150 MHz	—	400	600	

Notes:

1. See test circuit and waveforms.
2. Skew measured at worse cast temperature (max. temp).

Test Circuits for All Outputs

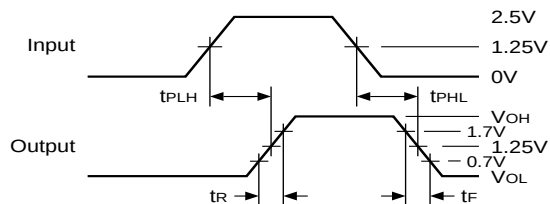


Definitions:

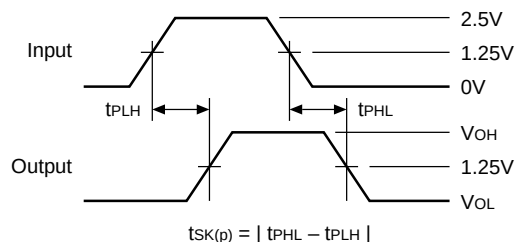
C_L = Load capacitance: includes jig and probe capacitance.

Switching Waveforms

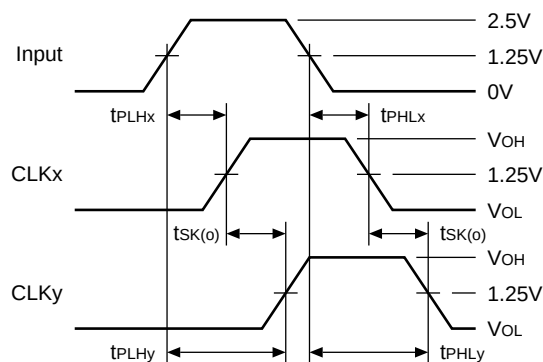
Propagation Delay



Pulse Skew – $t_{SK(P)}$

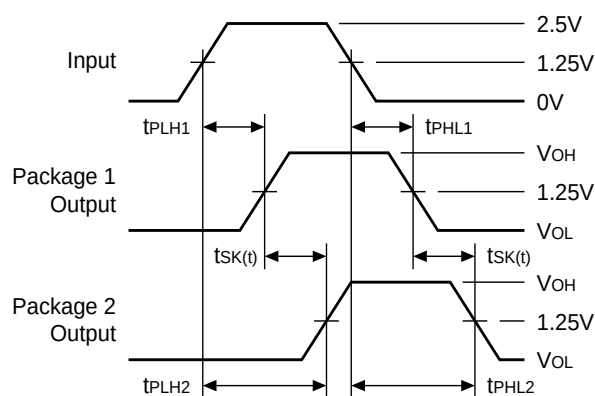


Output Skew – $t_{SK(O)}$



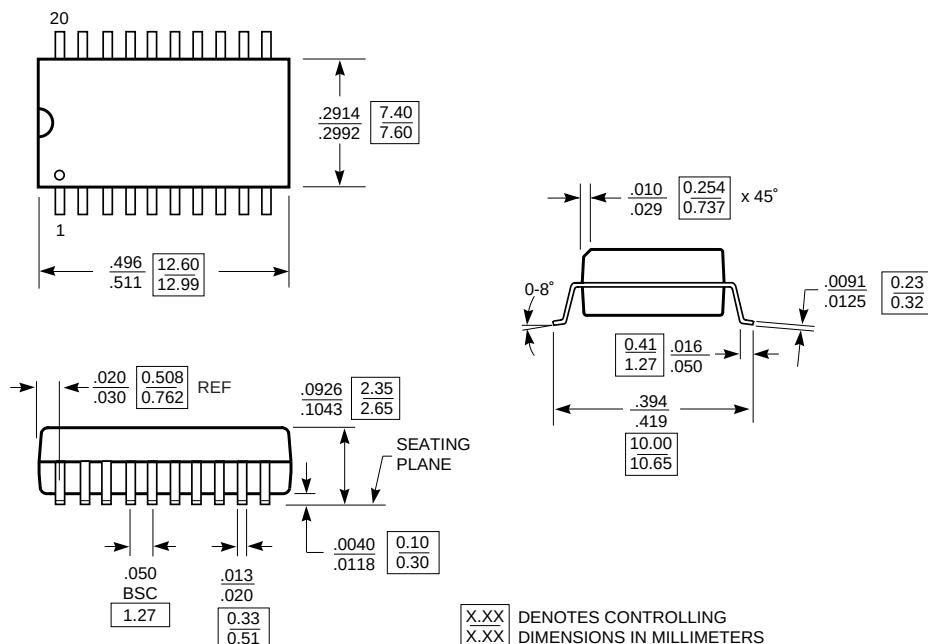
$$t_{SK(O)} = t_{PLHx} - t_{PLHy} \text{ or } t_{PHLx} - t_{PHLy}$$

Package Skew – $t_{SK(T)}$

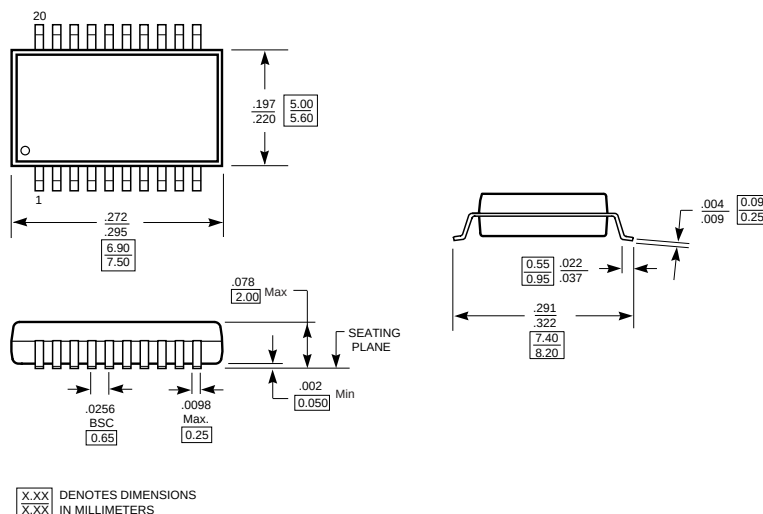


$$t_{SK(T)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

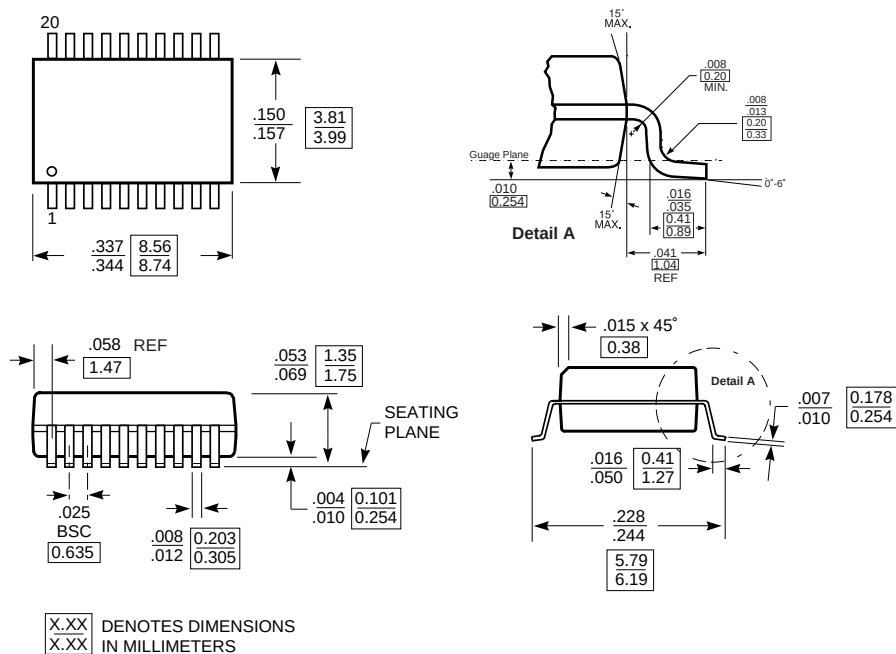
20-Pin SOIC (S) Package



20-Pin SSOP (H) Package



20-Pin QSOP (Q) Package



Ordering Information

Ordering Code	Package Type	Operating Range
PI49FCT20807S	20-pin 300 mil wide SOIC	Industrial
PI49FCT20807Q	20-pin 150 mil wide QSOP	
PI49FCT20807H	20-pin 209 mil wide SSOP	