



LC²MOS Complete 12-Bit, 100 kHz Sampling ADC with DSP Interface

ANALOG DEVICES INC

AD7878

1.1 Scope.

This specification covers the detail requirement for a fast, complete 12-bit A/D converter with a versatile DSP interface consisting of an 8-word, first in, first out (FIFO) memory and associated control logic.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD7878S(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X) Package	Description
Q	Q-28 28-Pin Cerdip
E	E-28A 28-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to DGND	 -0.3 V dc to +7.0 V dc
V_{CC} to DGND	 -0.3 V dc to +7.0 V dc
V_{SS} to DGND	 +0.3 V dc to -7.0 V dc
V_{DD} to V_{CC}	 -0.3 V dc to +0.3 V dc
AGND to DGND	 -0.3 V dc to $V_{DD} + 0.3$ V dc
V_{IN} to AGND	 -15.0 V dc to +15.0 V dc
REF OUT to AGND	 0 V dc to V_{DD}
Digital Inputs to DGND, CLKIN, $\overline{\text{DMWR}}$, $\overline{\text{DMRD}}$, RESET, CS, $\overline{\text{CONVST}}$, ADD0	 -0.3 V dc to $V_{DD} + 0.3$ V dc
Digital Outputs to DGND, $\overline{\text{ALFL}}$, $\overline{\text{BUSY}}$	 -0.3 V dc to $V_{DD} + 0.3$ V dc
Data Pin DB11-DB0	 -0.3 V dc to $V_{DD} + 0.3$ V dc
Power Dissipation	 1000 mW
Storage Temperature Range	 -65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10 sec)	 $+300^\circ\text{C}$

1.4 Recommended Operating Conditions.

Supply Voltage

V_{DD}	 +4.75 V dc to +5.25 V dc
V_{CC}	 +4.75 V dc to +5.25 V dc
V_{SS}	 -4.75 V dc to -5.25 V dc
Ambient Operating Temperature Range, T_A	 -55°C to $+125^\circ\text{C}$

Table 1.

Test	Symbol	Device	Limits		Sub Groups	Test Conditions ^{1, 2} -55°C ≤ T _A ≤ +125°C unless otherwise noted	Unit
			Min	Max			
Signal-to-Noise Ratio ³	SNR	-1	70		4, 5, 6	10 kHz Sine Wave Applied to V _{IN} , V _{IN} = ±3.0 V, f _{SAMPLE} = 100 kHz, V _{DD} = V _{CC} = 5.0 V, V _{SS} = -5.0 V	dB
Total Harmonic Distortion	THD	-1		-78	4, 5, 6		dB
Peak Harmonic or Spurious Noise	PHN	-1		-78	4, 5, 6		dB
Intermodulation Distortion 2nd Order Terms	IMD ₂	-1		-78	4, 5, 6	f _a = 9.0 kHz, f _b = 9.5 kHz, f _{SAMPLE} = 50 kHz V _{DD} = V _{CC} = 5.0 V; V _{SS} = 5.0 V	dB
3rd Order Terms	IMD ₃	-1		-78	4, 5, 6		dB
Track/Hold Acquisition Time	t _{ACQ}	-1		2.0	9, 10, 11		μs
Resolution	RES	-1	12		1, 2, 3		Bits
Bipolar Zero Error	BZE	-1		±6.0	1, 2, 3	V _{DD} = V _{CC} = 5.0 V; V _{SS} = -5.0 V	LSB
Positive Full-Scale Error ⁴	+FSE	-1		±6.0	1, 2, 3	V _{DD} = V _{CC} = 5.0 V; V _{SS} = -5.0 V	LSB
Negative Full-Scale Error ⁴	-FSE	-1		±6.0	1, 2, 3	V _{DD} = V _{CC} = 5.0 V; V _{SS} = -5.0 V	LSB
Analog Input Current	I _{IN}	-1		±1	1, 2, 3	V _{DD} = V _{CC} = 5.0 V; V _{SS} = -5.0 V	mA
REF OUT Voltage	V _{RO}	-1	2.97	3.03	1	V _{DD} = V _{CC} = 5.0 V; V _{SS} = -5.0 V	V
REF OUT Error	ROE	-1		±10	1	V _{DD} = V _{CC} = 5.0 V; V _{SS} = -5.0 V	mV
				±15	2, 3		
Reference Load Sensitivity ⁶	ΔV _{RO} /ΔI	-1		±1.0	1, 2, 3	Reference Load Current Change (0 μA-500 μA) V _{DD} = V _{CC} = 5 V; V _{SS} = -5 V	mV
Input Logic High Voltage	V _{INH}	-1	2.4		7, 8	V _{DD} = V _{CC} = 5.0, 5.25 V; V _{SS} = -5.0, -5.25 V	V
Input Logic Low Voltage	V _{INL}	-1		0.8	7, 8	V _{DD} = V _{CC} = 5.0, 5.25 V; V _{SS} = -5.0, -5.25 V	V
Logic Input Current	I _{IN}	-1		±10	1, 2, 3	V _{DD} = V _{CC} = 5.0 V; V _{SS} = -5.0 V, V _{IN} = 0 to V _{CC}	μA
Input Capacitance Logic Inputs	C _{IN}	-1		10	4		pF
Output Logic High Voltage	V _{OH}	-1	2.7		1, 2, 3	V _{DD} = V _{CC} = +5.2 V, V _{SS} = -5.0 V I _{SOURCE} = 40 μA	V
Output Logic Low Voltage	V _{OL}	-1		0.4	1, 2, 3	V _{DD} = V _{CC} = +4.75 V, V _{SS} = -5.0 V I _{SINK} = 1.6 mA	V
DB11-DB0 Output Floating-State Leakage Current	I _{FSL} (DB11-DB0)	-1		±10	1, 2, 3	V _{DD} = V _{CC} = 5.0 V V _{SS} = -5.0 V	μA
DB11-DB0 Floating-State Output Capacitance	C _{OUT}	-1		15	4		pF
Conversion Time ⁷	t _{CONV}	-1	7.000	7.125	7, 8	Assuming No External Read/Write Operations	μs
			7.000	9.250		Assuming 17 External Read/Write Operations	
Positive Supply Current	I _{DD}	-1		13	1, 2, 3	CS = DMWR = DMRD = +5.0 V V _{DD} , V _{CC} = -5.25 V, V _{SS} = -5.25 V	mA
	I _{CC}			100			μA
	I _{SS}			6.0			mA
Propagation Delay Time CLK IN to BUSY Low ⁵	t ₁	-1		75	9, 10, 11	See Note 8	ns
Propagation Delay Time CLK IN to BUSY High ⁵	t ₂	-1		75	9, 10, 11	See Note 8	ns
CONVST Pulse Width ⁵	t ₃	-1	2.0		9, 10, 11	See Note 8	CLK IN Cycles
Setup Time CS to DMRD/ REGISTER ENABLE ⁵	t ₄	-1	0		9, 10, 11	See Note 8	ns

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Test	Symbol	Device	Limits		Sub Groups	Test Conditions ^{1, 2} $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ unless otherwise noted	Unit
			Min	Max			
Hold Time $\overline{\text{CS}}$ to DMRD/ REGISTER ENABLE ⁵	t_5	-1	0		9, 10, 11	See Note 8	ns
DMRD Pulse Width ⁷	t_6	-1	60		7, 8	See Note 8	ns
				50 ⁵			μs
Setup Time, ADD0 to DMRD/ REGISTER ENABLE ⁷	t_7	-1	16		7, 8	See Note 8	ns
Hold Time, ADD0 to DMRD/ REGISTER ENABLE ⁵	t_8	-1	0		9, 10, 11	See Note 8	ns
Data Access Time after DMRD ¹⁰	t_9	-1	57		9, 10, 11	See Note 8	ns
Bus Relinquish Time ^{7, 9}	t_{10}	-1	5.0	45	7, 8	See Note 8	ns
REGISTER ENABLE Pulse Width ⁹	t_{11}	-1	55		7, 8	See Note 8	ns
				50 ⁵			μs
Setup Time Data Valid to REGISTER ENABLE ⁷	t_{12}	-1	30		7, 8	See Note 8	ns
Data Hold Time after REGISTER ENABLE ⁵	t_{13}	-1	10		9, 10, 11	See Note 8	ns
Data Access Time after BUSY ^{5, 10}	t_{14}	-1	57		9, 10, 11	See Note 8	ns

NOTES

¹ $V_{DD} = +4.75\text{ V}$ to $+5.25\text{ V}$, $V_{CC} = +4.75$ to $+5.25\text{ V}$, $V_{SS} = -4.75$ to -5.25 V , $\text{AGND} = \text{DGND} = 0\text{ V}$, $f_{CLK} = 8.0\text{ MHz}$.

²Timing Tests at $V_{DD} = V_{CC} = 4.75\text{ V}$, $V_{SS} = -5.0\text{ V}$.

³SNR Calculation includes distortion and noise components.

⁴Measured with respect to the Internal Reference.

⁵If not tested, shall be guaranteed to the limits specified in Table 1.

⁶Reference load current should not be changed during conversion. The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for external use, it should be decoupled with a 200 Ω resistor in series with a parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor. These decoupling components are required to remove voltage spikes caused by the devices internal operation.

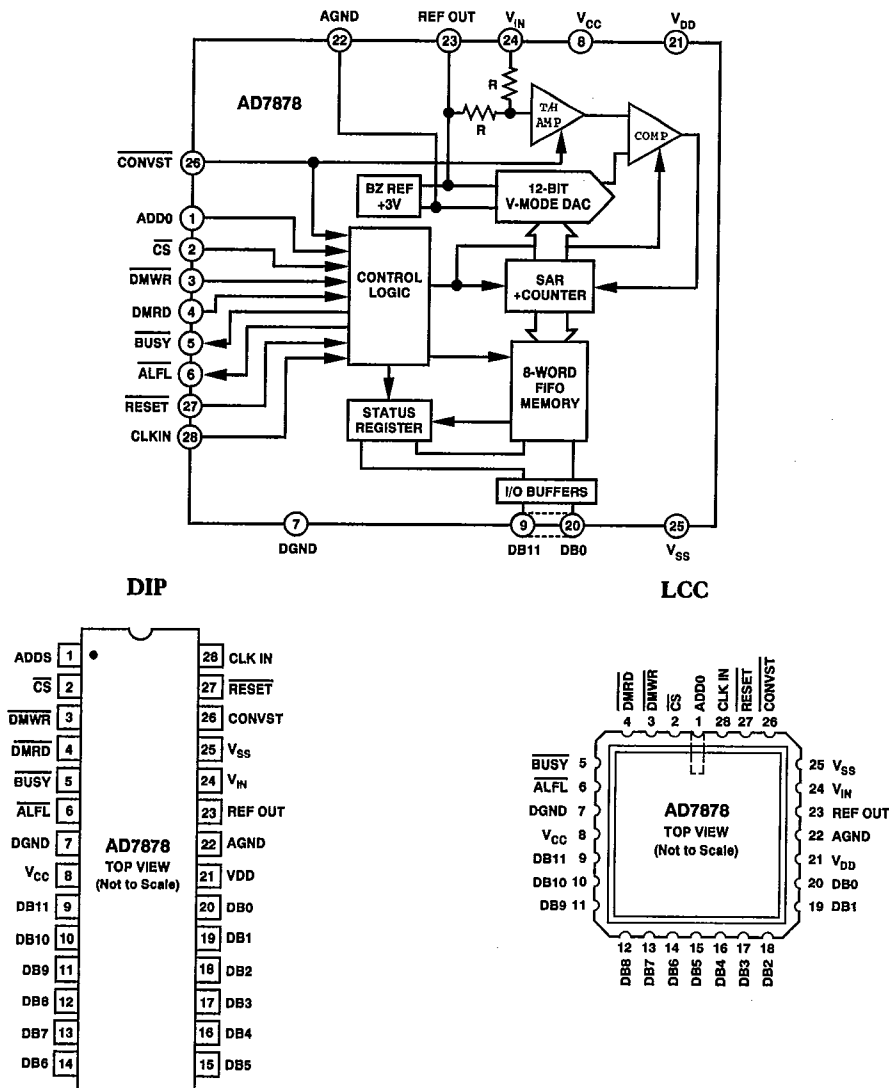
⁷These parameters are functionally tested on a pass/fail basis using the appropriate limits.

⁸All input signals are specified with tr and tf = 5.0 ns (10% to 90% of 5.0 V), timed from a voltage level of 1.6 V.

⁹ t_{10} is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figures 1c and 1d.

¹⁰ t_9 and t_{14} are measured with the load circuits of Figures 3a and 3b and defined as the time required for an output to cross 0.8 V and 2.4 V.

3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

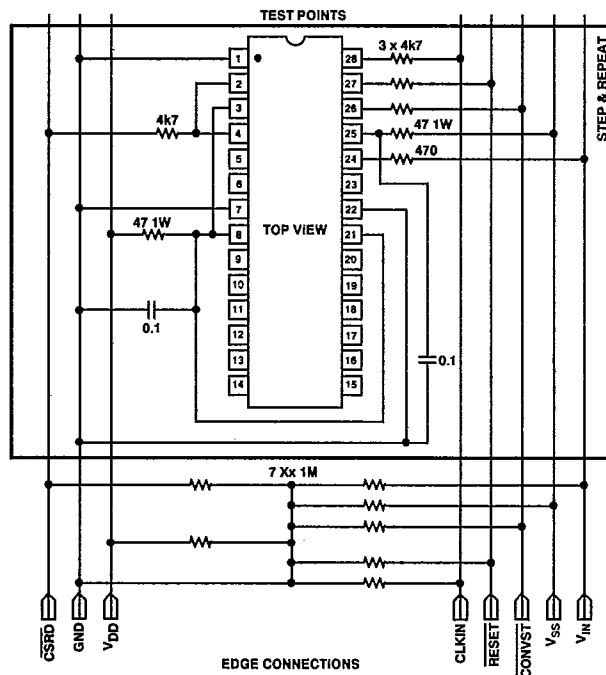
This microcircuit is covered by technology group (81).

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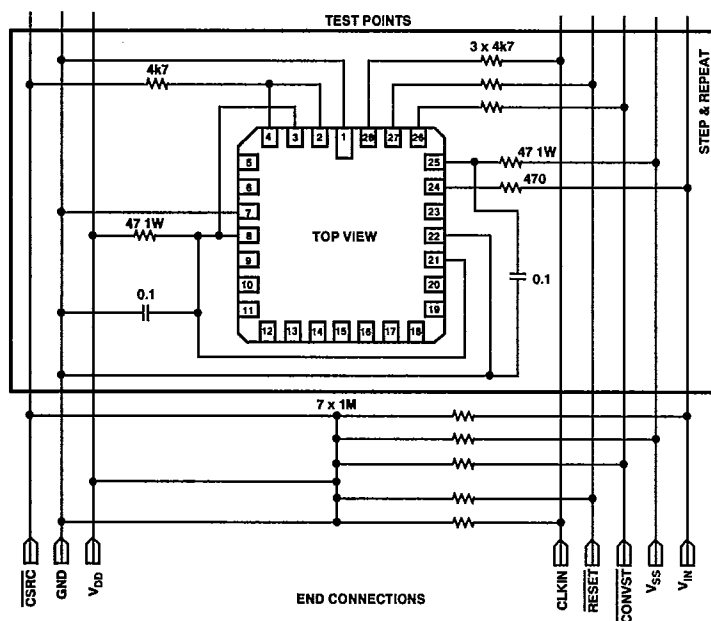
4.2.1 Life Test Burn-In Circuit

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

Cerdip



LCC



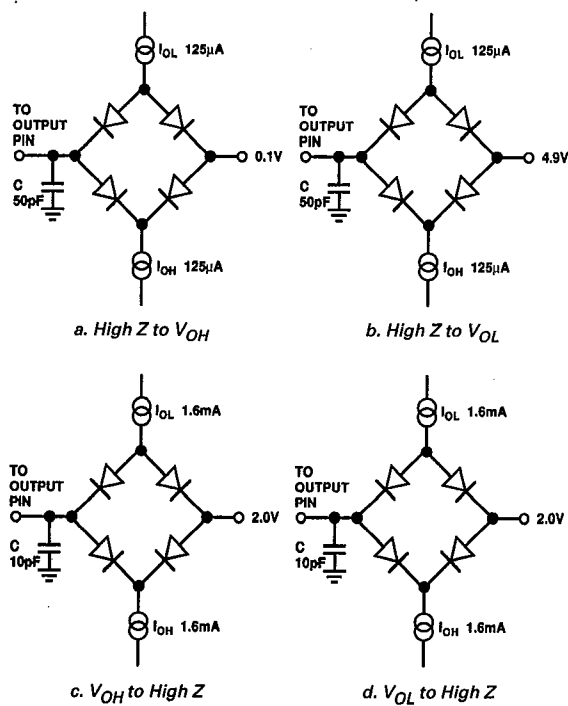


Figure 1. Output Load Circuits and Waveforms