Fast CMOS Clock Driver

Product Features:

- Guaranteed low skew: 0.5 ns
- Low input capacitance
- Minimum duty cycle distortion
- 1:10 fanout
- High speed: 3.5 ns propagation delay
- TTL input and output compatible
  - — V_{OH} = 3.3V (typ.)
  - — V_{OL} = 0.3V (typ.)
- Radiation Tolerant and Radiation Enhanced versions of product also available
- Packaged in 20-pin plastic DIP, surface mount SOIC, or the industry's new "1/4 size" surface mount QSOP

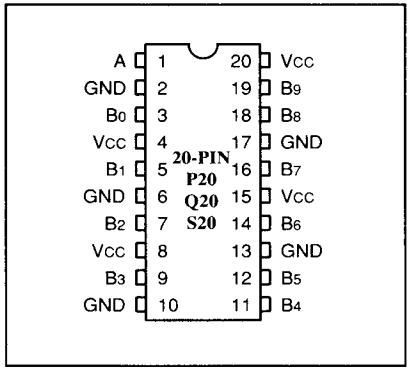
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

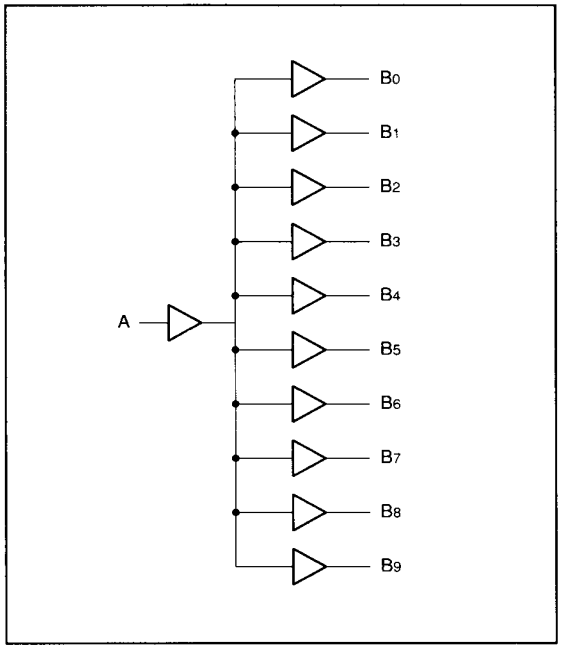
This low skew clock driver features one input and ten outputs fanout. The large fanout from a single input line reduces loading on input clock. TTL level outputs reduce noise levels on the part. Typical applications are clock and signal distribution.

This product is available in three package types: 20-pin, 300 mil wide plastic DIP, 300 mil wide plastic SOIC, and the industry's new 150 mil wide QSOP (one quarter the size of an SOIC).

Product Pin Configuration



Logic Block Diagram



Product Pin Description

Pin Name	Description
A	Input
B0 – B9	Outputs
GND	Ground
VCC	Power

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to Vcc
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15.0 mA	2.4	3.3		V
			I_{OH} = –32.0 mA	2.0	3.0		V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48 mA		0.2	0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = 2.7 V			5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = 0.5 V			–5	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_{OUT} = 2.7 V			+10	µA
I_{OZL}	Output Current		V_{OUT} = 0.5 V			–10	µA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC} (Max.)				20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–60	–120	–225	mA
I_{OFF}	Power Down Disable	V_{CC} = GND, V_{OUT} = 4.5 V		—	—	100	µA
V_H	Input Hysteresis				150		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	6.0	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF

Notes:
1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.2	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.,	V_{IN} = 3.4 V[3]		0.5	1.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open 50% Duty Cycle, One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND		0.4	0.6	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 50 MHz,	V_{IN} = V_{CC} V_{IN} = GND		20	30[5]	mA
		50% Duty Cycle, One Bit toggling at fi = 5 MHz	V_{IN} = 3.4 V V_{IN} = GND		20.7	33[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0 V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4 V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4 V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	FCT807T Com. Min	FCT807T Com. Max	FCT807BT Com. Min	FCT807BT Com. Max	FCT807CT Com. Min	FCT807CT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay A to B_N	Z_O = 50Ω with Thevenin	1.5	4.5	1.5	3.5	1.5	3.5	ns
$t_{SK(o)}$	Skew between two outputs of same package[3]	termination (See Figure c)		0.5		0.5		0.25	ns
$t_{SK(p)}$	Skew between opposite transitions of same output ($\lvert t_{PHL} - t_{PLH} \rvert$)[3]	or with AC termination (See Figure d)		0.5		0.5		0.35	ns
$t_{SK(t)}$	Skew between outputs of different package at same power supply, temperature and speed grade[3]	f ≤ 100MHz Outputs ganged in groups of two	—	1.0	—	1.0		0.75	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	FCT807T Com. Min	FCT807T Com. Max	FCT807BT Com. Min	FCT807BT Com. Max	FCT807CT Com. Min	FCT807CT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay A TO BN	C_L = 30 pF t ≤ 67MHz	1.5	4.5	1.5	3.8	1.5	3.5	ns
$t_{SK(o)}$	Skew between two outputs of same package[3]	(See Figure b)		0.5		0.5		0.25	ns
$t_{SK(p)}$	Skew between opposite transitions of same output ($\lvert t_{PHL} - t_{PLH} \rvert$)[3]			0.5		0.5		0.35	ns
$t_{SK(t)}$	Skew between outputs of different package at same power supply, temperature and speed grade[3]		—	1.0	—	0.9		0.75	ns

Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	FCT807T Com. Min	FCT807T Com. Max	FCT807BT Com. Min	FCT807BT Com. Max	FCT807CT Com. Min	FCT807CT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay A TO BN	C_L = 50 pF t ≤ 40MHz	1.5	4.5	1.5	3.8	1.5	3.5	ns
$t_{SK(o)}$	Skew between two outputs of same package[3]	(See Figure a)		0.5		0.5		0.25	ns
$t_{SK(p)}$	Skew between opposite transitions of same output ($\lvert t_{PHL} - t_{PLH} \rvert$)[3]			0.5		0.5		0.35	ns
$t_{SK(t)}$	Skew between outputs of different package at same power supply, temperature and speed grade[3]		—	1.0	—	1.0		0.75	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

Test Circuits and Waveforms

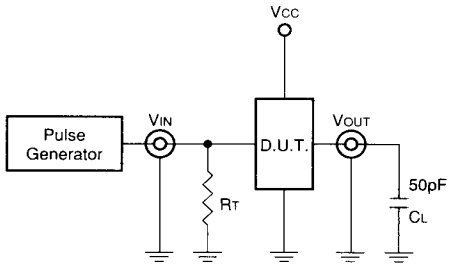


Figure a

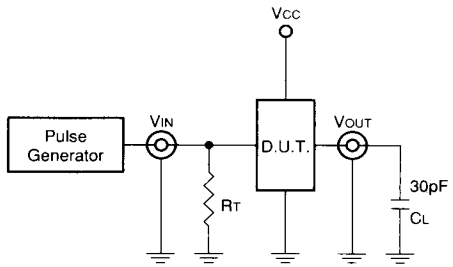


Figure b

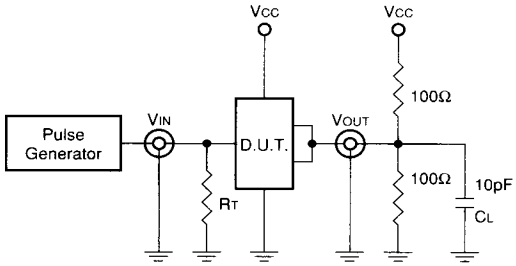
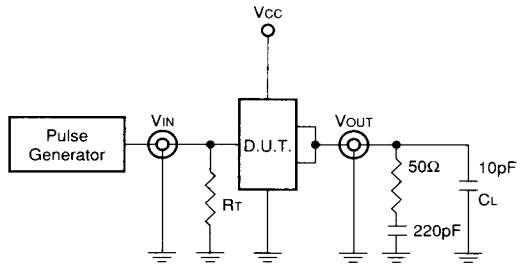


Figure c



The capacitor value for AC termination is determined by the operation frequency. For very low frequencies a higher capacitor value should be selected.

Figure d

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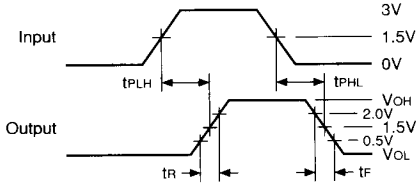
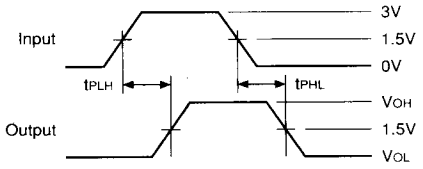
Test Circuits and Waveforms (Continued)

Propagation Delay

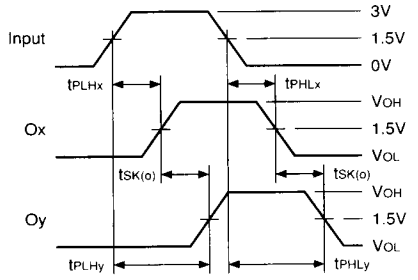


Pulse Skew – tSK(p)



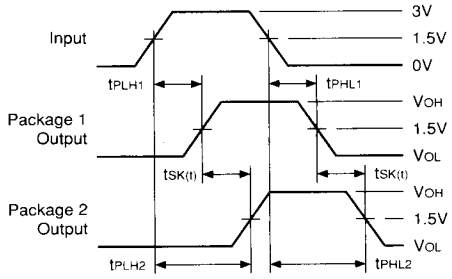
$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

Output Skew – tSK(o)



$t_{SK(o)} = |t_{PLHy} - t_{PLHx}|$ or $|t_{PHLy} - t_{PHLx}|$

Package Skew – tSK(t)



$t_{SK(t)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$