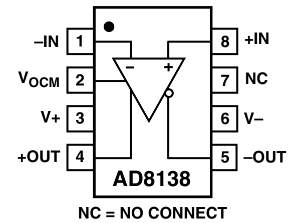
Low Distortion Differential ADC Driver

AD8138

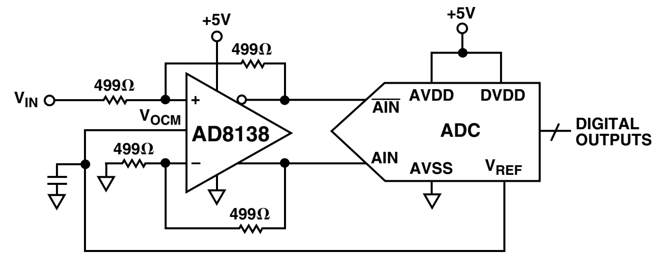
FEATURES
Easy to Use Single-Ended-to-Differential Conversion
Adjustable Output Common-Mode Voltage
Externally Adjustable Gain
Low Harmonic Distortion
–94 dBc—Second, <–114 dBc—Third @ 5 MHz into 800 Ω Load
–87 dBc—Second, –85 dBc—Third @ 20 MHz into 800 Ω Load
–3 dB Bandwidth of 320 MHz, G = +1
Fast Settling to 0.01% of 16 ns
Slew Rate 1150 V/μs
Fast Overdrive Recovery of 4 ns
Low Input Voltage Noise of 5 nV/√Hz
1 mV Typical Offset Voltage
Wide Supply Range +3 V to ±5 V
Low Power 90 mW on 5 V
0.1 dB Gain Flatness to 40 MHz
Available in 8-Lead SOIC and MICRO_SOIC

APPLICATIONS
ADC Driver
Single-Ended-to-Differential Converter
IF and Baseband Gain Block
Differential Buffer
Line Driver

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



PRODUCT DESCRIPTION

AD8138 is a major advancement over op amps for differential signal processing. The AD8138 can be used as a single-ended-to-differential amplifier or as a differential-to-differential amplifier. The AD8138 is as easy to use as an op amp, and greatly simplifies differential signal amplification and driving.

Manufactured on ADI's proprietary XFCB bipolar process, the AD8138 has a –3 dB bandwidth of 320 MHz and delivers a differential signal with the lowest harmonic distortion available in a differential amplifier. The AD8138 has a unique internal feedback feature that provides output gain and phase matching that are balanced, suppressing even order harmonics. The internal feedback circuit also minimizes any gain error that would be associated with the mismatches in the external gain setting resistors.

The AD8138's differential output helps balance the input-to-differential ADCs, maximizing the performance of the ADC. The AD8138 eliminates the need for a transformer with high performance ADCs, preserving the low frequency and dc information. The common-mode level of the differential output is adjustable by a voltage on the V_{OCM} pin, easily level-shifting the input signals for driving single supply ADCs. Fast overload recovery preserves sampling accuracy.

The AD8138 distortion performance makes it an ideal ADC driver for communication systems, with distortion performance good enough to drive state-of-the-art 10- to 16-bit converters at high frequencies. The AD8138's high bandwidth and IP3 also make it appropriate for use as a gain block in IF and baseband signal chains. The AD8138 offset and dynamic performance make it well suited for a wide variety of signal processing and data acquisition applications.

The AD8138 is available in both SOIC and MICRO_SOIC packages for operation over –40°C to +85°C temperatures.

REV. C

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AD8138–SPECIFICATIONS (@ 25°C, V_S = ±5 V, V_{OCM} = 0, G = +1, $R_{L,dm}$ = 500 Ω, unless otherwise noted. Refer to Figure 1 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs unless otherwise noted.)

Parameter	Conditions	AD8138 Min	AD8138 Typ	AD8138 Max	Unit
$\pm D_{IN}$ to ±OUT Specifications					
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	V_{OUT} = 0.5 V p-p, C_F = 0 pF	290	320		MHz
	V_{OUT} = 0.5 V p-p, C_F = 1 pF		225		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.5 V p-p, C_F = 0 pF		30		MHz
Large Signal Bandwidth	V_{OUT} = 2 V p-p, C_F = 0 pF		265		MHz
Slew Rate	V_{OUT} = 2 V p-p, C_F = 0 pF		1150		V/µs
Settling Time	0.01%, V_{OUT} = 2 V p-p, C_F = 1 pF		16		ns
Overdrive Recovery Time	V_{IN} = 5 V to 0 V Step, G = +2		4		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 800 Ω		–94		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 800 Ω		–87		dBc
	V_{OUT} = 2 V p-p, 70 MHz, $R_{L,dm}$ = 800 Ω		–62		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 800 Ω		–114		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 800 Ω		–85		dBc
	V_{OUT} = 2 V p-p, 70 MHz, $R_{L,dm}$ = 800 Ω		–57		dBc
IMD	20 MHz		–77		dBc
IP3	20 MHz		37		dBm
Voltage Noise (RTI)	f = 100 kHz to 40 MHz		5		$nV/\sqrt{Hz}$
Input Current Noise	f = 100 kHz to 40 MHz		2		$pA/\sqrt{Hz}$
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS,dm} = V_{OUT,dm}/2$; $V_{DIN+} = V_{DIN–} = V_{OCM}$ = 0 V	–2.5	±1	+2.5	mV
	T_{MIN}–T_{MAX} Variation		±4		µV/°C
Input Bias Current			3.5	7	µA
	T_{MIN}–T_{MAX} Variation		–0.01		µA/°C
Input Resistance	Differential		6		MΩ
	Common Mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			–4.7 to +3.4		V
CMRR	$\Delta V_{OUT,dm}/\Delta V_{IN,cm}$; $\Delta V_{IN,cm}$ = ±1 V		–77	–70	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; Single-Ended Output		7.75		V p-p
Output Current			95		mA
Output Balance Error	$\Delta V_{OUT,cm}/\Delta V_{OUT,dm}$; $\Delta V_{OUT,dm}$ = 1 V		–66		dB
V_{OCM} to ±OUT Specifications					
DYNAMIC PERFORMANCE					
–3 dB Bandwidth			250		MHz
Slew Rate			330		V/µs
DC PERFORMANCE					
Input Voltage Range			±3.8		V
Input Resistance			200		kΩ
Input Offset Voltage	$V_{OS,cm} = V_{OUT,cm}$; $V_{DIN+} = V_{DIN–} = V_{OCM}$ = 0 V	–3.5	±1	+3.5	mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$[\Delta V_{OUT,dm}/\Delta V_{OCM}]$; ΔV_{OCM} = ±1 V		–75		dB
Gain	$\Delta V_{OUT,cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V	0.9955	1	1.0045	V/V
POWER SUPPLY					
Operating Range		±1.4		±5.5	V
Quiescent Current		18	20	23	mA
	T_{MIN} to T_{MAX} Variation		40		µA/°C
Power Supply Rejection Ratio	$\Delta V_{OUT,dm}/\Delta V_S$; ΔV_S = ±1 V		–90	–70	dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

NOTES

Harmonic Distortion Performance is equal or slightly worse with higher values of $R_{L,dm}$. See TPCs 13 and 14 for more information.

Specifications subject to change without notice.

SPECIFICATIONS (@ 25°C, V_S = 5 V, V_{OCM} = 2.5 V, G = +1, $R_{L,dm}$ = 500 Ω, unless otherwise noted. Refer to Figure 1 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs unless otherwise noted.)

Parameter	Conditions	AD8138 Min	AD8138 Typ	AD8138 Max	Unit
±D_{IN} to ±OUT Specifications					
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	V_{OUT} = 0.5 V p-p, C_F = 0 pF	280	310		MHz
	V_{OUT} = 0.5 V p-p, C_F = 1 pF		225		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.5 V p-p, C_F = 0 pF		29		MHz
Large Signal Bandwidth	V_{OUT} = 2 V p-p, C_F = 0 pF		265		MHz
Slew Rate	V_{OUT} = 2 V p-p, C_F = 0 pF		950		V/µs
Settling Time	0.01%, V_{OUT} = 2 V p-p, C_F = 1 pF		16		ns
Overdrive Recovery Time	V_{IN} = 2.5 V to 0 V Step, G = +2		4		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 800 Ω		–90		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 800 Ω		–79		dBc
	V_{OUT} = 2 V p-p, 70 MHz, $R_{L,dm}$ = 800 Ω		–60		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 800 Ω		–100		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 800 Ω		–82		dBc
	V_{OUT} = 2 V p-p, 70 MHz, $R_{L,dm}$ = 800 Ω		–53		dBc
IMD	20 MHz		–74		dBc
IP3	20 MHz		35		dBm
Voltage Noise (RTI)	f = 100 kHz to 40 MHz		5		nV/√Hz
Input Current Noise	f = 100 kHz to 40 MHz		2		pA/√Hz
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS,dm} = V_{OUT,dm}/2$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 2.5 V	–2.5	±1	+2.5	mV
	T_{MIN}–T_{MAX} Variation		±4		µV/°C
Input Bias Current			3.5	7	µA
	T_{MIN}–T_{MAX} Variation		–0.01		µA/°C
Input Resistance	Differential		6		MΩ
	Common Mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			0.3 to 3.2		V
CMRR	$\Delta V_{OUT,dm}/\Delta V_{IN,cm}$; $\Delta V_{IN,cm}$ = 1 V		–77	–70	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; Single-Ended Output		2.9		V p-p
Output Current			95		mA
Output Balance Error	$\Delta V_{OUT,cm}/\Delta V_{OUT,dm}$; $\Delta V_{OUT,dm}$ = 1 V		–65		dB
V_{OCM} to ±OUT Specifications					
DYNAMIC PERFORMANCE					
–3 dB Bandwidth			220		MHz
Slew Rate			250		V/µs
DC PERFORMANCE					
Input Voltage Range			1.0 to 3.8		V
Input Resistance			100		kΩ
Input Offset Voltage	$V_{OS,cm} = V_{OUT,cm}$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 2.5 V	–5	±1	+5	mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$[\Delta V_{OUT,dm}/\Delta V_{OCM}]$; ΔV_{OCM} = 2.5 ± 1 V		–70		dB
Gain	$\Delta V_{OUT,cm}/\Delta V_{OCM}$; ΔV_{OCM} = 2.5 ± 1 V	0.9968	1	1.0032	V/V
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current		15	20	21	mA
	T_{MIN} to T_{MAX} Variation		40		µA/°C
Power Supply Rejection Ratio	$\Delta V_{OUT,dm}/\Delta V_S$; ΔV_S = ±1 V		–90	–70	dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

NOTES

Harmonic Distortion Performance is equal or slightly worse with higher values of $R_{L,dm}$. See Figures TPC 13 and 14 for more information.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±5.5 V
V_{OCM}	$\pm V_S$
Internal Power Dissipation	550 mW
θ_{JA}[2] (SOIC)	155°C/W
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10 sec)	300°C

NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above listed in the operational section of this specification is not implied. Exposure to Absolute Maximum Ratings for any extended periods may affect device reliability.
[2] Thermal resistance measured on SEMI standard 4-layer board.

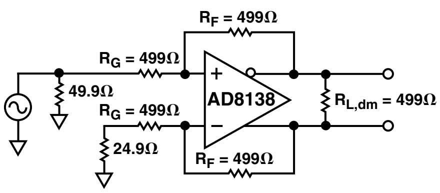
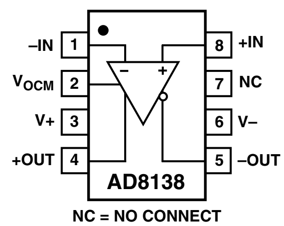


Figure 1. Basic Test Circuit

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1	–IN	Negative Input Summing Node
2	V_{OCM}	Voltage applied to this pin sets the common-mode output voltage with a ratio of 1:1. For example, 1 V dc on V_{OCM} will set the dc bias level on +OUT and –OUT to 1 V.
3	V+	Positive Supply Voltage
4	+OUT	Positive Output. Note: the voltage at $–D_{IN}$ is inverted at +OUT.
5	–OUT	Negative Output. Note: the voltage at $+D_{IN}$ is inverted at –OUT.
6	V–	Negative Supply Voltage
7	NC	No Connect
8	+IN	Positive Input Summing Node

PIN CONFIGURATION



ORDERING GUIDE

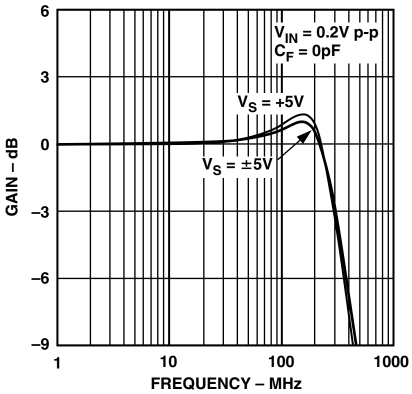
Model	Temperature Range	Package Descriptions	Package Options	Branding Information
AD8138AR	–40°C to +85°C	8-Lead SOIC	SO-8	
AD8138AR-REEL[1]	–40°C to +85°C	8-Lead SOIC	13" Tape and Reel	
AD8138AR-REEL7[2]	–40°C to +85°C	8-Lead SOIC	7" Tape and Reel	
AD8138ARM	–40°C to +85°C	8-Lead MICRO_SOIC	RM-8	HBA
AD8138ARM-REEL[3]	–40°C to +85°C	8-Lead SOIC	13" Tape and Reel	HBA
AD8138ARM-REEL7[2]	–40°C to +85°C	8-Lead SOIC	7" Tape and Reel	HBA
AD8138-EVAL		Evaluation Board	SOIC	

NOTES
[1]13" Reels of 2500 each.
[2]7" Reels of 1000 each.
[3]13" Reels of 3000 each.

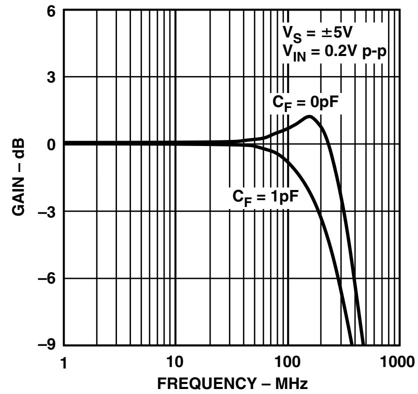
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8138 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

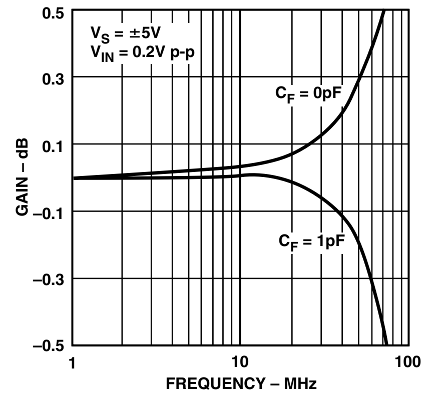
Unless otherwise noted, GAIN = 1, $R_G = R_F = R_{L,dm}$ = 499 Ω, T_A = 25°C; Refer to Figure 1 for test setup.



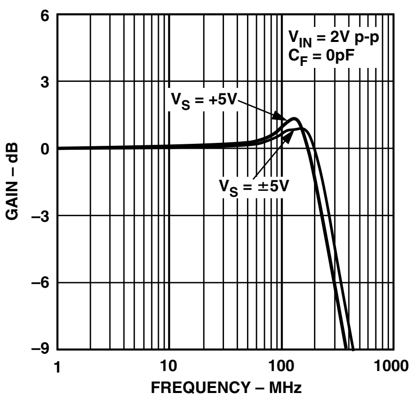
TPC 1. Small Signal Frequency Response



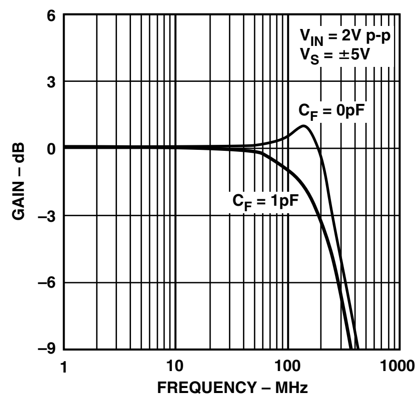
TPC 2. Small Signal Frequency Response



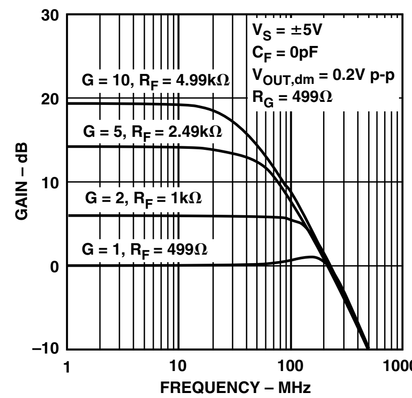
TPC 3. 0.1 dB Flatness vs. Frequency



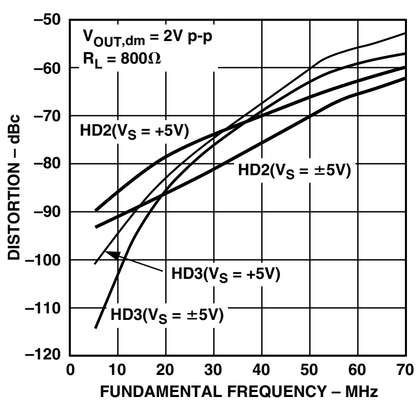
TPC 4. Large Signal Frequency Response



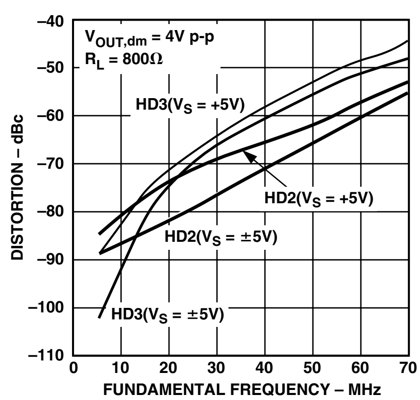
TPC 5. Large Signal Frequency Response



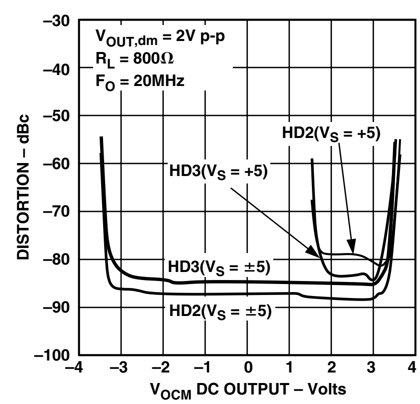
TPC 6. Small Signal Frequency Response for Various Gains



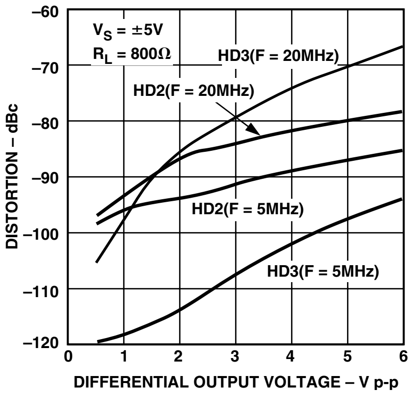
TPC 7. Harmonic Distortion vs. Frequency



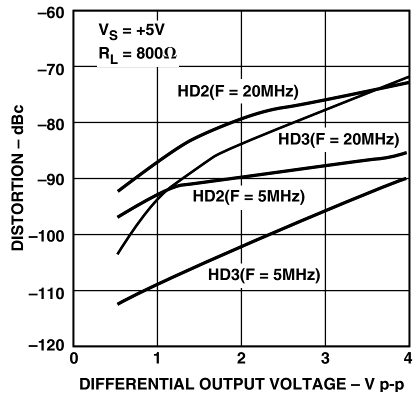
TPC 8. Harmonic Distortion vs. Frequency



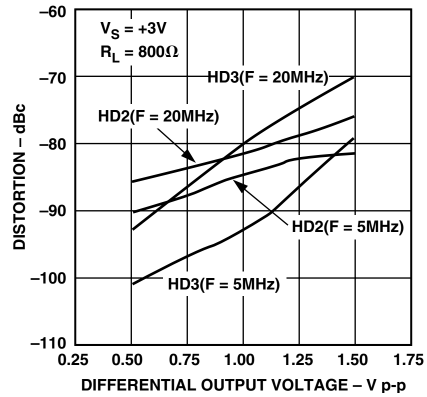
TPC 9. Harmonic Distortion vs. V_{OCM}



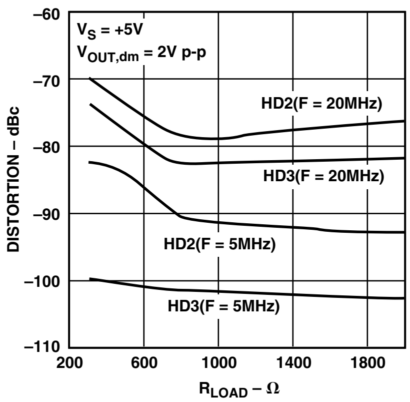
TPC 10. Harmonic Distortion vs. Differential Output Voltage



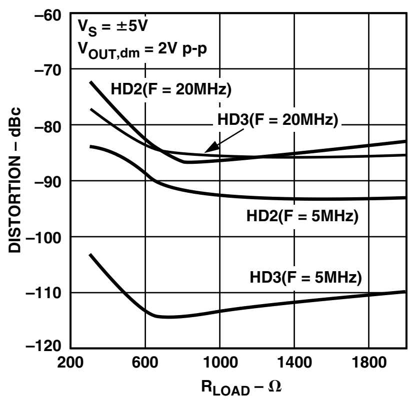
TPC 11. Harmonic Distortion vs. Differential Output Voltage



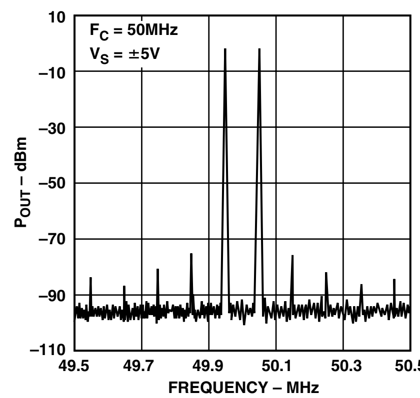
TPC 12. Harmonic Distortion vs. Differential Output Voltage



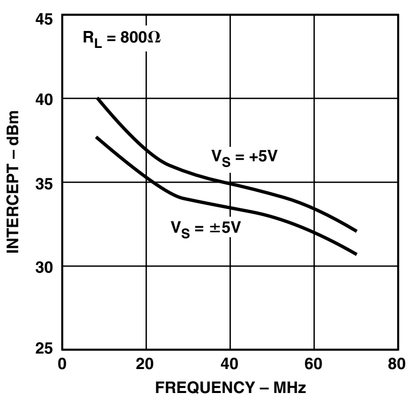
TPC 13. Harmonic Distortion vs. R_{LOAD}



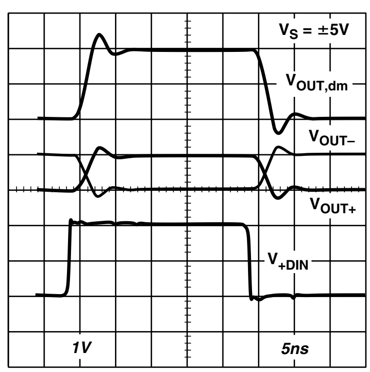
TPC 14. Harmonic Distortion vs. R_{LOAD}



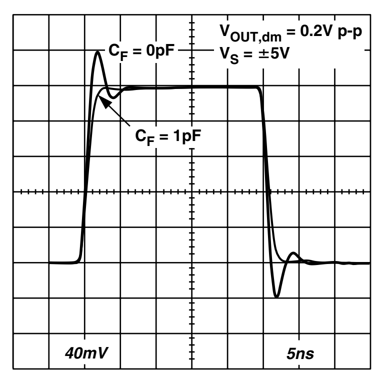
TPC 15. Intermodulation Distortion



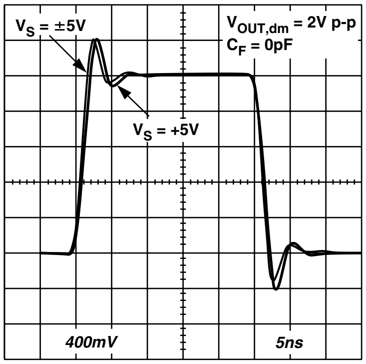
TPC 16. Third Order Intercept vs. Frequency



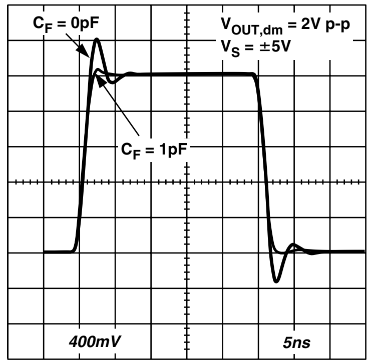
TPC 17. Large Signal Transient Response



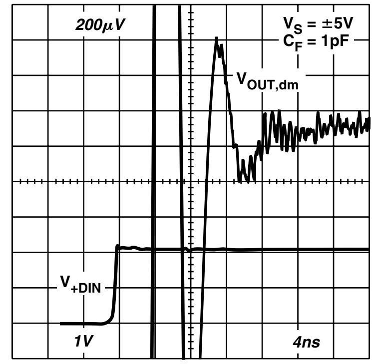
TPC 18. Small Signal Transient Response



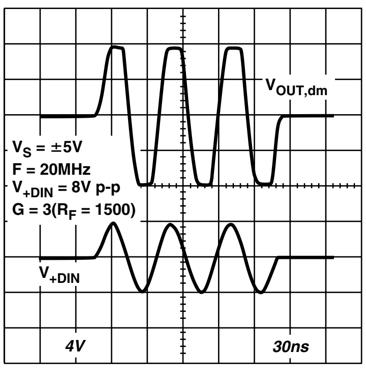
TPC 19. Large Signal Transient Response



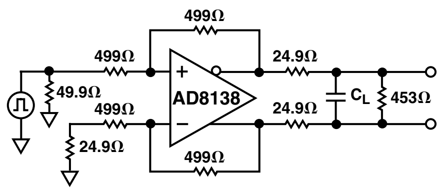
TPC 20. Large Signal Transient Response



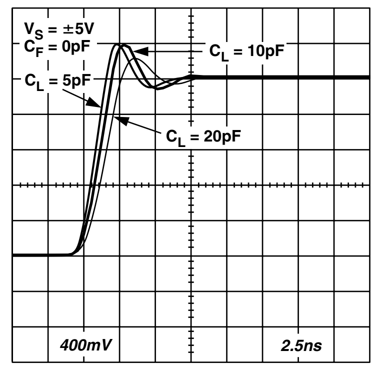
TPC 21. Settling Time



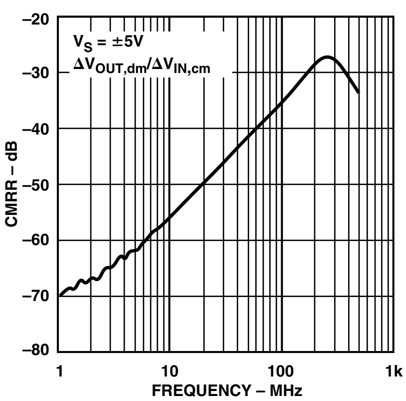
TPC 22. Output Overdrive



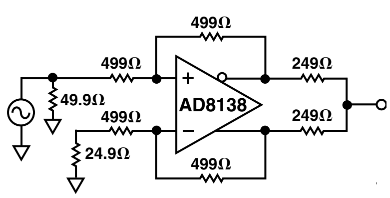
TPC 23. Test Circuit for Cap Load Drive



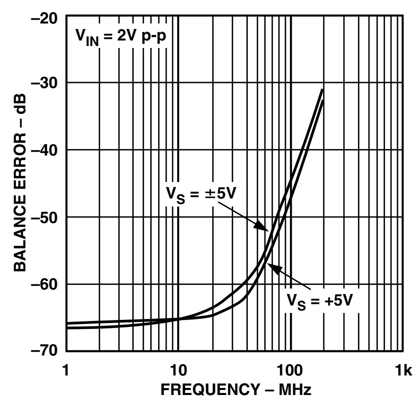
TPC 24. Large Signal Transient Response for Various Cap Loads



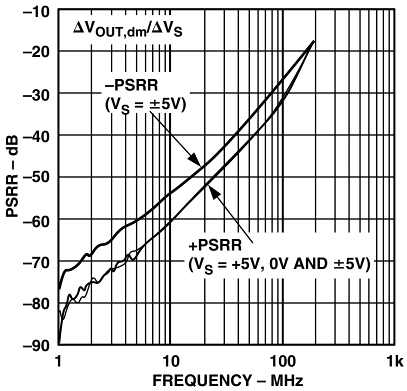
TPC 25. CMRR vs. Frequency



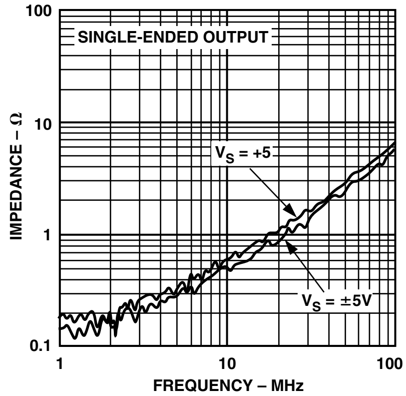
TPC 26. Test Circuit for Output Balance



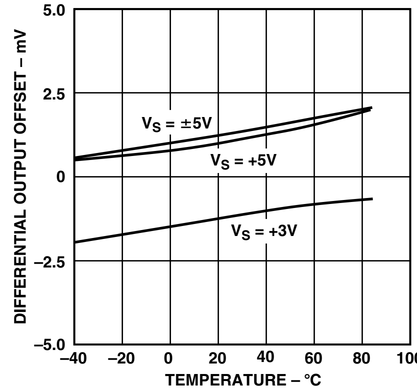
TPC 27. Output Balance Error vs. Frequency



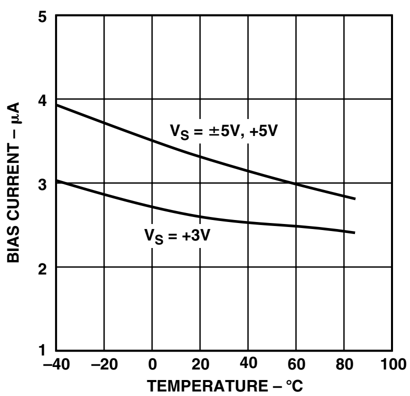
TPC 28. PSRR vs. Frequency



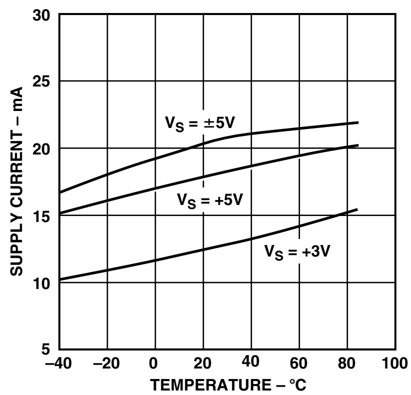
TPC 29. Output Impedance vs. Frequency



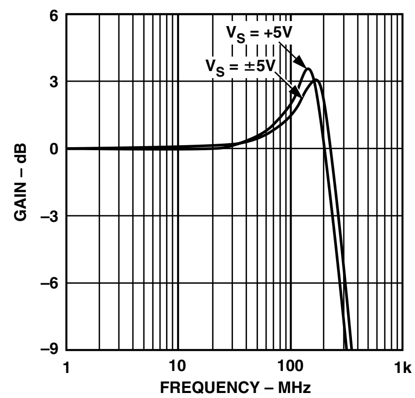
TPC 30. Output Referred Differential Offset Voltage vs. Temperature



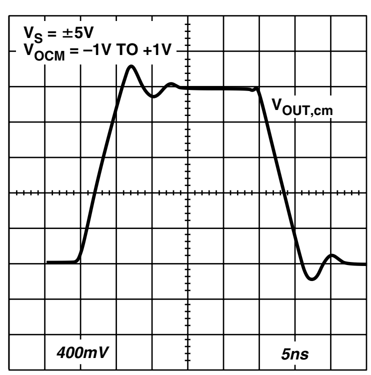
TPC 31. Input Bias Current vs. Temperature



TPC 32. Supply Current vs. Temperature



TPC 33. V_{OCM} Frequency Response



TPC 34. V_{OCM} Transient Response

OPERATIONAL DESCRIPTION

Definition of Terms

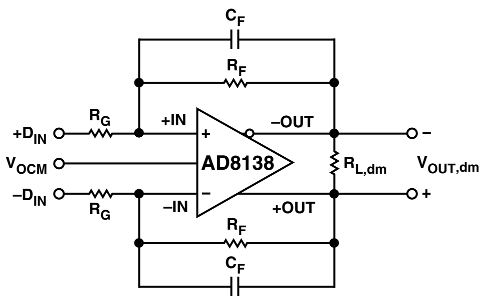


Figure 2. Circuit Definitions

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently output differential-mode voltage) is defined as:

$$V_{OUT,dm} = (V_{+OUT} - V_{-OUT})$$

V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and –OUT terminals with respect to a common reference.

Common-mode voltage refers to the average of two node voltages. The output common-mode voltage is defined as:

$$V_{OUT,cm} = (V_{+OUT} + V_{-OUT})/2$$

Balance is a measure of how well differential signals are matched in amplitude and exactly 180 degrees apart in phase. Balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the divider's midpoint with the magnitude of the differential signal. (See TPC 26.) By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential-mode voltage:

$$Output\ Balance\ Error = \left| \frac{V_{OUT,cm}}{V_{OUT,dm}} \right|$$

THEORY OF OPERATION

The AD8138 differs from conventional op amps in that it has two outputs whose voltages move in opposite directions. Like an op amp, it relies on high open loop gain and negative feedback to force these outputs to the desired voltages. The AD8138 behaves much like a standard voltage feedback op amp and makes it easy to perform single-ended-to-differential conversion, common-mode level-shifting, and amplification of differential signals. Also like an op amp, the AD8138 has high input impedance and low output impedance.

Previous differential drivers, both discrete and integrated designs, have been based on using two independent amplifiers, and two independent feedback loops, one to control each of the outputs. When these circuits are driven from a single-ended source, the resulting outputs are typically not well balanced. Achieving a balanced output has typically required exceptional matching of the amplifiers and feedback networks.

DC common-mode level-shifting has also been difficult with previous differential drivers. Level-shifting has required the use of a third amplifier and feedback loop to control the output common-mode level. Sometimes the third amplifier has also been used to attempt to correct an inherently unbalanced circuit. Excellent performance over a wide frequency range has proven difficult with this approach.

The AD8138 uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to arbitrarily set the output common-mode level. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the V_{OCM} input, without affecting the differential output voltage.

The AD8138 architecture results in outputs that are very highly balanced over a wide frequency range without requiring tightly matched external components. The common-mode feedback loop forces the signal component of the output common-mode voltage to be zeroed. The result is nearly perfectly balanced differential outputs, of identical amplitude and exactly 180 degrees apart in phase.

Analyzing an Application Circuit

The AD8138 uses high open-loop gain and negative feedback to force its differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and –IN in Figure 2. For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

Setting the Closed Loop Gain

Neglecting the capacitors C_F, the differential mode gain of the circuit in Figure 2 can be determined to be described by the following equation:

$$\left| \frac{V_{OUT,dm}}{V_{IN,dm}} \right| = \frac{R_F{}^S}{R_G{}^S}$$

This assumes the input resistors, $R_G{}^S$ and feedback resistors, $R_F{}^S$ on each side are equal.

Estimating the Output Noise Voltage

Similar to the case of a conventional op amp, the differential output errors (noise and offset voltages) can be estimated by multiplying the input referred terms, at +IN and –IN, by the circuit noise gain. The noise gain is defined as:

$$G_N = 1 + \left(\frac{R_F}{R_G} \right)$$

To compute the total output referred noise for the circuit of Figure 2, consideration must also be given to the contribution of the resistors R_F and R_G. Refer to Table I for estimated output noise voltage densities at various closed-loop gains.

Table I

Gain	R_G (Ω)	R_F (Ω)	Bandwidth –3 dB	Output Noise 8138 Only	Output Noise 8138 + R_G, R_F
1	499	499	320 MHz	10 nV/$\sqrt{Hz}$	11.5 nV/$\sqrt{Hz}$
2	499	1.0 k	180 MHz	15 nV/$\sqrt{Hz}$	16.6 nV/$\sqrt{Hz}$
5	499	2.49 k	70 MHz	30 nV/$\sqrt{Hz}$	31.6 nV/$\sqrt{Hz}$
10	499	4.99 k	30 MHz	55 nV/$\sqrt{Hz}$	56.6 nV/$\sqrt{Hz}$

The Impact of Mismatches in the Feedback Networks

As mentioned previously, even if the external feedback networks (R_F/R_G) are mismatched, the internal common-mode feedback loop will still force the outputs to remain balanced. The amplitudes of the signals at each output will remain equal and 180 degrees out of phase. The input-to-output differential-mode gain will vary proportionately to the feedback mismatch, but the output balance will be unaffected.

Ratio matching errors in the external resistors will result in a degradation of the circuit's ability to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional op amp.

Also, if the dc levels of the input and output common-mode voltages are different, matching errors will result in a small differential-mode output offset voltage. For G = 1 case, with a ground referenced input signal and the output common-mode level set for 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance will result in a worst case input CMRR of about 40 dB, worst-case differential mode output offset of 25 mV due to 2.5 V level-shift, and no significant degradation in output balance error.

Calculating an Application Circuit's Input Impedance

The effective input impedance of a circuit such as that in Figure 2, at $+D_{IN}$ and $-D_{IN}$, will depend on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the input impedance (R_{IN},dm) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply:

$$R_{IN,dm} = 2 \times R_G$$

In the case of a single-ended input signal (for example if $-D_{IN}$ is grounded and the input signal is applied to $+D_{IN}$), the input impedance becomes:

$$R_{IN,dm} = \left(\frac{R_G}{1 - \dfrac{R_F}{2 \times \left(R_G + R_F\right)}} \right)$$

The circuit's input impedance is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G.

Input Common-Mode Voltage Range in Single Supply Applications

The AD8138 is optimized for level-shifting "ground" referenced input signals. For a single-ended input this would imply, for example, that the voltage at $-D_{IN}$ in Figure 1 would be zero volts when the amplifier's negative power supply voltage (at V–) was also set to zero volts.

Setting the Output Common-Mode Voltage

The AD8138's V_{OCM} pin is internally biased at a voltage approximately equal to the midsupply point (average value of the voltages on V+ and V–). Relying on this internal bias will result in an output common-mode voltage that is within about 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (made up of 10 kΩ resistors), be used. The output common-mode offset specified on pages 2 and 3 assume the V_{OCM} input is driven by a low impedance voltage source.

Driving a Capacitive Load

A purely capacitive load can react with the pin and bondwire inductance of the AD8138 resulting in high frequency ringing in the pulse response. One way to minimize this effect is to place a small capacitor across each of the feedback resistors. The added capacitance should be small to avoid destabilizing the amplifier. An alternative technique is to place a small resistor in series with the amplifier's outputs as shown in TPC 23.

LAYOUT, GROUNDING AND BYPASSING

As a high speed part, the AD8138 is sensitive to the PCB environment in which it has to operate. Realizing its superior specifications requires attention to various details of good high speed PCB design.

The first requirement is for a good solid ground plane that covers as much of the board area around the AD8138 as possible. The only exception to this is that the two input pins (Pins 1 and 8) should be kept a few mm from the ground plane, and ground should be removed from inner layers and the opposite side of the board under the input pins. This will minimize the stray capacitance on these nodes and help preserve the gain flatness versus frequency.

The power supply pins should be bypassed as close as possible to the device to the nearby ground plane. Good high frequency ceramic chip capacitors should be used. This bypassing should be done with a capacitance value of 0.01 µF to 0.1 µF for each supply. Further away, low frequency bypassing should be provided with 10 µF tantalum capacitors from each supply to ground.

The signal routing should be short and direct in order to avoid parasitic effects. Wherever there are complementary signals, a symmetrical layout should be provided to the extent possible to maximize the balance performance. When running differential signals over a long distance, the traces on PCB should be close together or any differential wiring should be twisted together to minimize the area of the loop that is formed. This will reduce the radiated energy and make the circuit less susceptible to interference.

BALANCED TRANSFORMER DRIVER

Transformers are among the oldest devices that have been used to perform a single-ended-to-differential conversion (and vice versa). Transformers also can perform the additional functions of galvanic isolation, step-up or step-down of voltages and impedance transformation. For these reasons, transformers will always find uses in certain applications.

However, when driving a transformer single-endedly and then looking at its output, there is a fundamental imbalance due to the parasitics inherent in the transformer. The primary (or driven) side of the transformer has one side at dc potential (usually ground), while the other side is driven. This can cause problems in systems that require good balance of the transformer's differential output signals.

If the interwinding capacitance (C_{STRAY}) is assumed to be uniformly distributed, a signal from the driving source will couple to the secondary output terminal that is closest to the primary's driven side. On the other hand, no signal will be coupled to the opposite terminal of the secondary, because its nearest primary terminal is not driven. (See Figure 3.) The exact amount of this imbalance will depend on the particular parasitics of the transformer, but will mostly be a problem at higher frequencies.

The balance of a differential circuit can be measured by connecting an equal-valued resistive voltage divider across the differential outputs and then measuring the center point of the circuit with respect ground. Since the two differential outputs are supposed to be of equal amplitude, but 180 degrees opposite phase, there should be no signal present for perfectly balanced outputs.

The circuit in Figure 3 shows a Minicircuits T1-6T transformer connected with its primary driven single-endedly and the secondary connected with a precision voltage divider across its terminals. The voltage divider is made up of two 500 Ω, 0.005% precision resistors. The voltage V_{UNBAL}, which is also equal to the ac common-mode voltage, is a measure of how closely the outputs are balanced.

The plots in Figure 5 show a comparison between the case where the transformer is driven single-endedly by a signal generator and driven differentially using an AD8138. The top signal trace of Figure 5 shows the balance of the single-ended configuration, while the bottom shows the differentially driven balance response. The 100 MHz balance is 35 dB better when using the AD8138.

The well-balanced outputs of the AD8138 will provide a drive signal to each of the transformer's primary inputs that are of equal amplitude and 180 degrees out of phase. Thus, depending on how the polarity of the secondary is connected, the signals that conduct across the interwinding capacitance will either both assist the transformer's secondary signal equally, or both buck the secondary signals. In either case, the parasitic effect will be symmetrical and provide a well-balanced transformer output. (See Figure 5.)

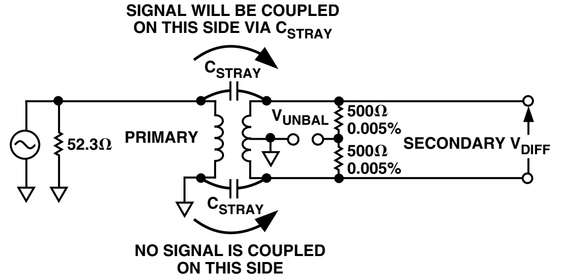


Figure 3. Transformer Single-Ended-to-Differential Converter Is Inherently Imbalanced

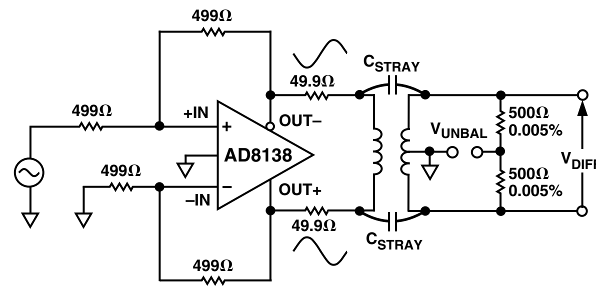


Figure 4. AD8138 Forms a Balanced Transformer Driver

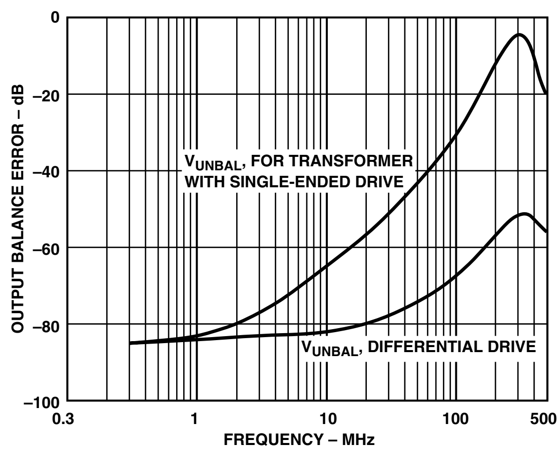


Figure 5. Output Balance Error for Circuits of Figures 3 and 4

HIGH-PERFORMANCE ADC DRIVING

The circuit in Figure 6 shows a simplified front-end connection for an AD8138 driving an AD9224, a 12-bit, 40 MSPS A/D converter. The A/D works best when driven differentially, which minimizes its distortion as described in its data sheet. The AD8138 eliminates the need for a transformer to drive the ADC and performs single-ended-to-differential conversion, common-mode level-shifting and buffering of the driving signal.

The positive and negative outputs of the AD8138 are connected to the respective differential inputs of the AD9224 via a pair of 49.9 Ω resistors to minimize the effects of the switched-capacitor front-end of the AD9224. For best distortion performance it is run from supplies of ±5 V.

The AD8138 is configured with unity gain for a single-ended input-to-differential output. The additional 23 Ω, 523 Ω total, at the input to –IN is to balance the parallel impedance of the 50 Ω source and its 50 Ω termination that drives the noninverting input.

The signal generator has a ground-referenced, bipolar output, i.e., it drives symmetrically above and below ground. Connecting V_{OCM} to the CML pin of the AD9224 sets the output common-mode of the AD8138 at 2.5 V, which is the midsupply level for the AD9224. This voltage is bypassed by a 0.1 μF capacitor.

The full-scale analog input range of the AD9224 is set to 4 V p-p, by shorting the SENSE terminal to AVSS. This has been determined to be the scaling to provide minimum harmonic distortion.

For the AD8138 to swing a 4 V p-p, each output swings 2 V p-p, while providing signals that are 180 degrees out of phase. With a common-mode voltage at the output of 2.5 V, this means that each AD8138 output will swing between 1.5 V and 3.5 V.

A ground-referenced 4 V p-p, 5 MHz signal at D_{IN}+ was used to test the circuit in Figure 6. When the combined-device circuit was run with a sampling rate of 20 MHz MSPS, the SFDR (spurious free dynamic range) was measured at –85 dBc.

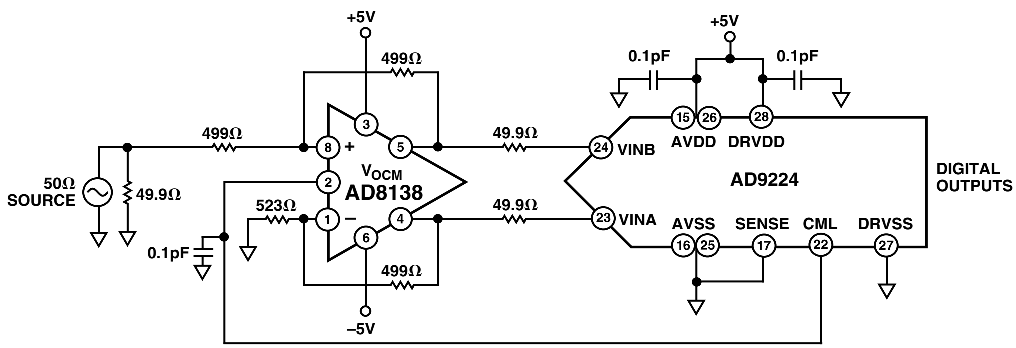


Figure 6. AD8138 Driving an AD9224, a 12-Bit, 40 MSPS A/D Converter

3 V OPERATION

The circuit in Figure 7 shows a simplified front end connection for an AD8138 driving an AD9203, a 10-bit, 40 MSPS A/D converter that is specified to work on a single 3 V supply. The A/D works best when driven differentially to make the best use of the signal swing available within the 3 V supply. The appropriate outputs of the AD8138 are connected to the appropriate differential inputs of the AD9203 via a low-pass filter.

The AD8138 is configured for unity gain for a single-ended input to differential output. The additional 23 Ω at the input to –IN is to balance the impedance of the 50 Ω source and its 50 Ω termination that drives the noninverting input.

The signal generator has ground-referenced, bipolar output, i.e., it can drive symmetrically above and below ground. Even though the AD8138 has ground as its negative supply, it can still function as a level-shifter with such an input signal.

The output common-mode is raised up to midsupply by the voltage divider that biases V_{OCM}. In this way, the AD8138 provides dc-coupling and level-shifting of a bipolar signal, without inverting the input signal.

The low-pass filter between the AD8138 and the AD9203 provides filtering that helps to improve the signal-to-noise ratio. Lower noise can be realized by lowering the pole frequency, but the bandwidth of the circuit will be lowered.

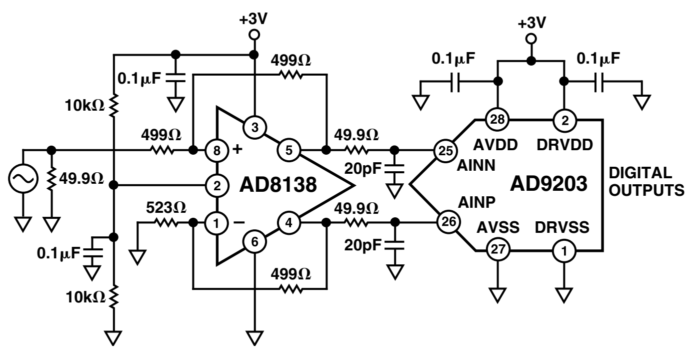


Figure 7. AD8138 Driving an AD9203, a 10-Bit, 40 MSPS A/D Converter

The circuit was tested with a –0.5 dBFS signal at various frequencies. Figure 8 shows a plot of the total harmonic distortion (THD) vs. frequency at signal amplitudes of 1 V and 2 V differential drive levels.

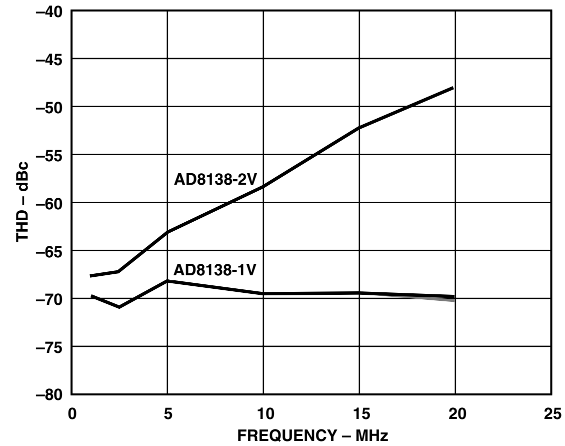


Figure 8. AD9203 THD @ –0.5 dBFS AD8138

Figure 9 shows the signal to noise plus distortion (SINAD) under the same conditions as above. For the smaller signal swing, the AD8138 performance is quite good, but its performance degrades when trying to swing too close to the supply rails.

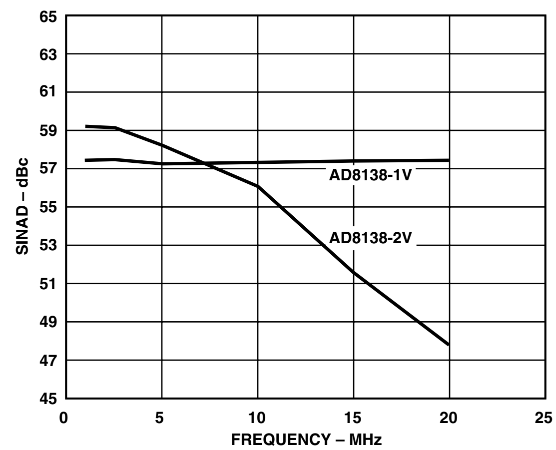
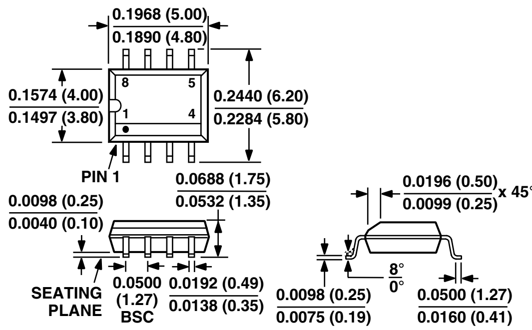


Figure 9. AD9203 SINAD @ –0.5 dBFS AD8138

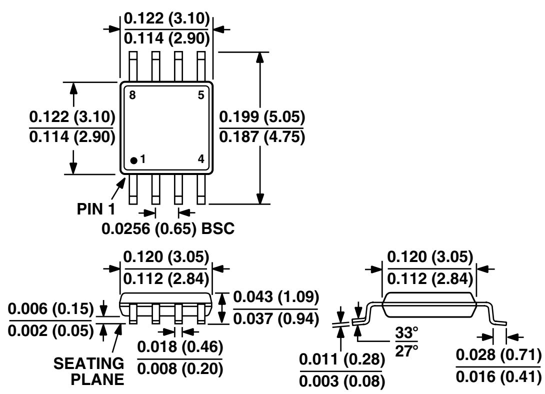
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SOIC (SO-8)



8-Lead MICRO_SOIC (RM-8)



AD8138–Revision History

Location	Page
Data Sheet changed from REV. B to REV. C.	
Edits to SPECIFICATIONS	2–3
Edits to ORDERING GUIDE	4

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