# PI6C991

## 5V High-Speed Programmable Skew Clock Buffer - *SuperClock*®

### Product Features

- Four pairs of programmable skew outputs
- 3.75 to 80 MHz output operation
- User-selectable output functions:
  - Selectable skews
  - Inverted and noninverted
  - Operation at ½ and ¼ input frequency
  - Operation at 2X and 4X input frequency
- Low skew <100ps typical, same pair. 250ps max.
- Allow REF clock input to have Spread Spectrum modulation for EMI reduction
- 2X, 4X, ½ and ¼ outputs
- 3-level inputs for skew and output frequency control
- External feedback, internal loop filter
- Low cycle-to-cycle Jitter: <25ps RMS
- Duty cycle of output clock signals: 45% min. 55% max.
- Compatible with Pentium based processor
- Same pinout as Cypress CY7B991
- Packaged in Plastic 32-pin PLCC Package

### Description

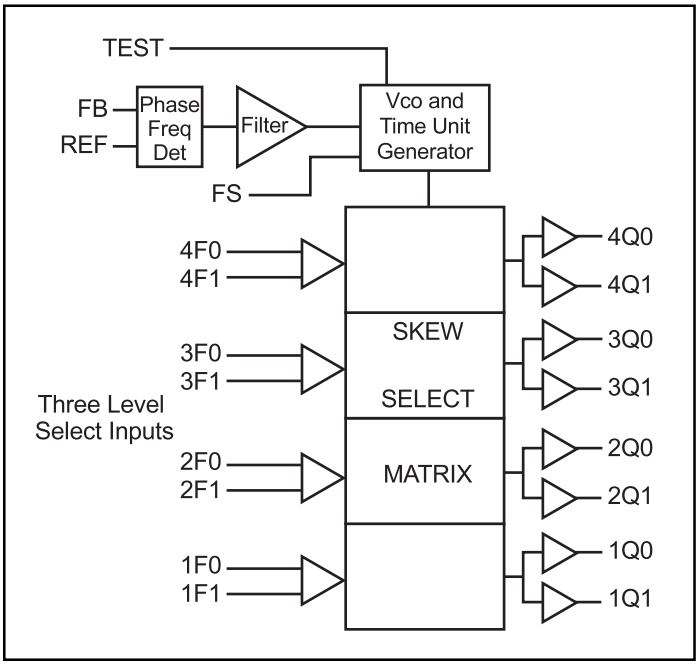
The PI6C991 is a low-skew, low jitter, 5V phase-lock loop (PLL) programmable skew clock driver, for high performance computing and networking applications. This part offers user selectable skew-control of 4 output pairs, providing the timing delays necessary to optimize high performance clock distribution circuits.

Each output can be hardwired to one of nine delay or function configurations. Delay increments are determined by the input clock frequency and the configurations selected by the user.

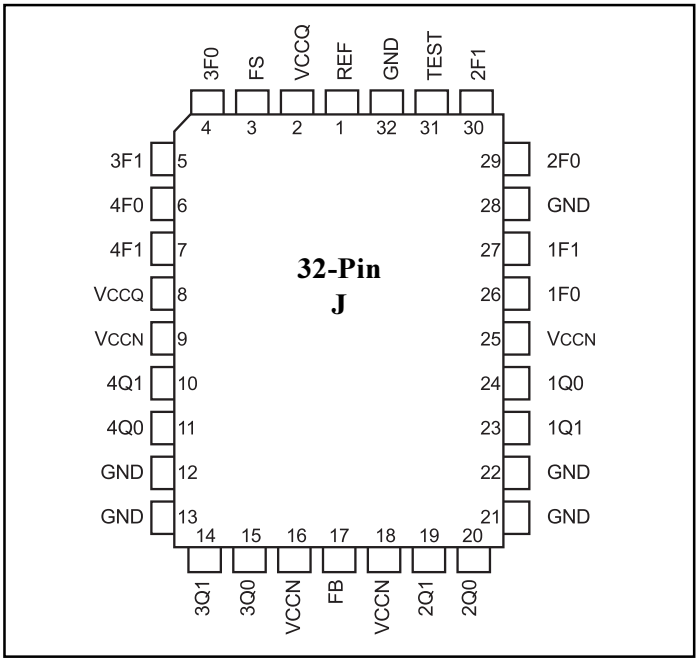
The PI6C991 allows the REF clock input to have Spread Spectrum modulation for EMI reduction.

The PI6C991 is pin-compatible with Cypress RoboClock CY7B991, with improved AC/DC characteristics.

### Logic Block Diagram




### Pin Configuration



## Pin Definitions

| Signal Name | I/O | Description |
|---|---|---|
| REF | I | Reference frequency input. This input supplies the frequency and timing reference which all functional variation is measured. |
| FB | | PLL feedback input (typically connected to one of the eight outputs). |
| FS | | Three-level frequency range select. See Table 1. |
| 1F0, 1F1 | | Three-level function select inputs for output pair 1 (1Q0, 1Q1). See Table 2. |
| 2F0, 2F1 | | Three-level function select inputs for output pair 2 (2Q0, 2Q1). See Table 2. |
| 3F0, 3F1 | | Three-level function select inputs for output pair 3 (3Q0, 3Q1). See Table 2. |
| 4F0, 4F1 | | Three-level function select inputs for output pair 4 (4Q0, 4Q1). See Table 2. |
| TEST | | Three-level select. See test mode section under the block diagram descriptions. |
| 1Q0, 1Q1 | O | Output pair 1. See Table 2. |
| 2Q0, 2Q1 | | Output pair 2. See Table 2. |
| 3Q0, 3Q1 | | Output pair 3. See Table 2. |
| 4Q0, 4Q1 | | Output pair 4. See Table 2. |
| $V_{CCN}$ | PWR | Power supply for output drivers. |
| $V_{CCQ}$ | | Power supply for internal circuitry. |
| GND | | Ground |

## Block Diagram Description

### Phase Frequency Detector and Filter

These two blocks accept input signals from the reference frequency (REF) input and the feedback (FB) input and generate correction information to control the frequency of the Voltage-Controlled Oscillator (VCO). These blocks, along with the VCO, form a Phase-Locked Loop (PLL) that tracks the incoming REF signal.

### VCO and Time Unit Generator

The VCO accepts analog control inputs from the PLL filter block and generates a frequency that is used by the time unit generator to create discrete time units that are selected in the skew mix matrix. The operational range of the VCO is determined by the FS control pin. The time unit ($t_U$) is determined by the operating frequency of the device and the level of the FS pin as shown in Table 1.

### Skew Select Matrix

The skew select matrix is comprised of four independent sections. Each section has two low-skew, high-fanout drivers (xQ0, xQ1), and two corresponding three-level function select (xF0, xF1) inputs. Table 2 shows the nine possible output functions for each section as determined by the function select inputs. All times are measured with respect to the REF input assuming that the output connected to the FB input has $0t_U$ selected.

**Table 1. Frequency Range Select and $t_U$ Calculation(1)**

| FS(2,3) | $f_{NOM}$(MHz) | | $t_U = \frac{1}{f_{NOM} \times N}$ where N= | Approximate Frequency (MHz) at which $t_U$ = 1.0ns |
|---|---|---|---|---|
| | Min. | Max. | | |
| LOW | 15 | 30 | 44 | 22.7 |
| MID | 25 | 50 | 26 | 38.5 |
| HIGH | 40 | 100 | 16 | 62.5 |

**Table 2. Programmable Skew Configurations(1)**

| Function Selects | | Output Functions | | |
|---|---|---|---|---|
| 1F1, 2F1, 3F1, 4F1 | 1F0, 2F0, 3F0, 4F0 | 1Q0, 1Q1, 2Q0, 2Q1 | 3Q0, 3Q1 | 4Q0, 4Q1 |
| LOW | LOW | $-4t_U$ | Divide by 2 | |
| | MID | $-3t_U$ | $-6t_U$ | |
| | HIGH | $-2t_U$ | $-4t_U$ | |
| MID | LOW | $-1t_U$ | $-2t_U$ | |
| | MID | $-0t_U$ | | |
| | HIGH | $+1t_U$ | $+2t_U$ | |
| HIGH | LOW | $+2t_U$ | $+4t_U$ | |
| | MID | $+3t_U$ | $+6t_U$ | |
| | HIGH | $+4t_U$ | Divide by 4 | Inverted |

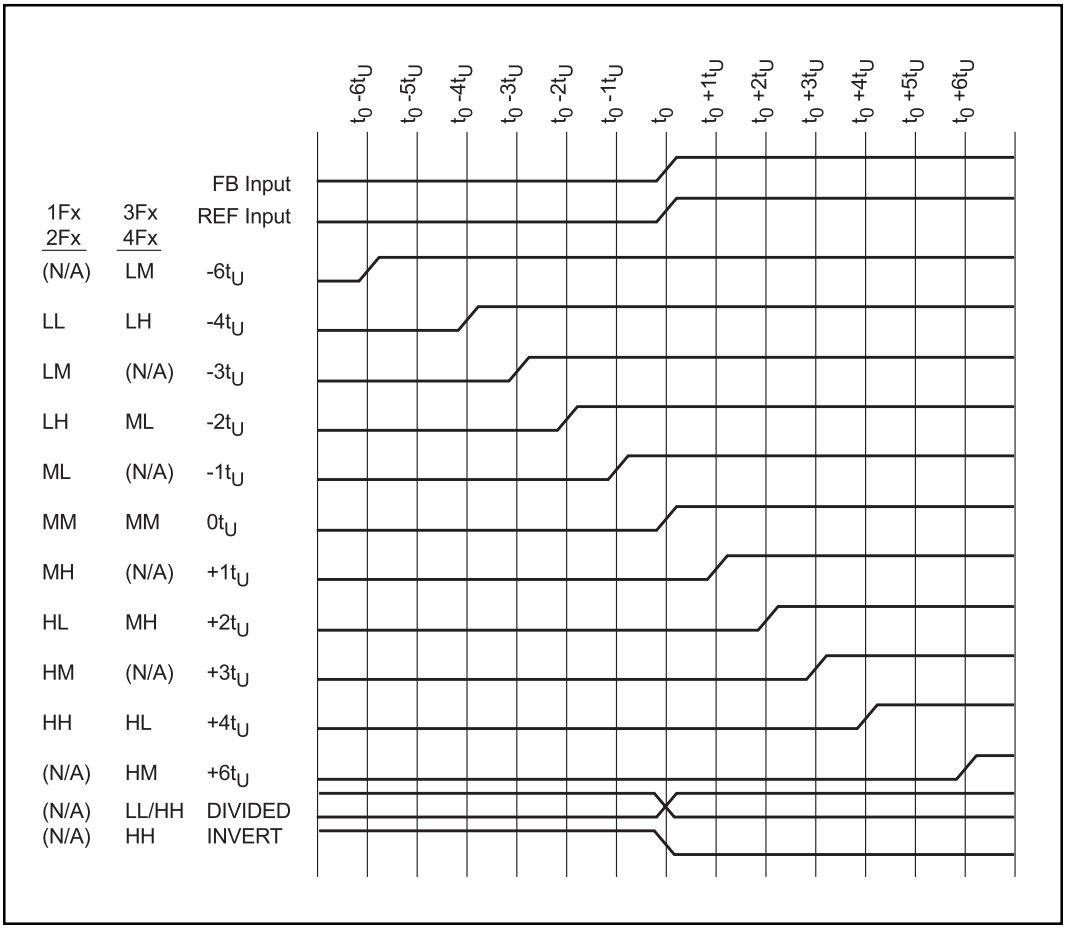



**Figure 1. Typical Outputs with FB Connected to a Zero-Skew Output(4)**

## Test Mode

The TEST input is a three-level input. In normal system operation, this pin is connected to ground, allowing the PI6C991 to operate as explained briefly above (for testing purposes, any of the three-level inputs can have a removable jumper to ground, or be tied LOW through a 100Ω resistor. This will allow an external tester to change the state of these pins).

If the TEST input is forced to its MID or HIGH state, the device will operate with its internal phase locked loop disconnected, and input levels supplied to REF will directly control all outputs. Relative output to output functions are the same as in normal mode.

In contrast with normal operation (TEST tied LOW). All outputs will function based only on the connection of their own function select inputs (xF0 and xF1) and the waveform characteristics of the REF input.

## Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... –65ºC to +150ºC
Ambient Temperature
with Power Applied ..... –55ºC to +125ºC
Supply Voltage to Ground Potential ..... –0.5V to +7.0V
DC Input Voltage ..... –0.5V to +7.0V
Output Current into Outputs (LOW) ..... 64mA
Static Discharge Voltage
(per MIL-STD-883, Method 3015) ..... >2001V
Latch-Up Current ..... >200mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0ºC to +70ºC | 5V ±10% |
| Industrial | –40ºC to +85ºC | 5V ±10% |

**Notes for Tables on Pages 3 through 7:**

1. For all three-state inputs, HIGH indicates a connection to $V_{CC}$, LOW indicates a connections to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
2. The level to be set on FS is determined by the "normal" operating frequency ($f_{NOM}$) of the $V_{CO}$ and the Time Unit Generator (see Logic Block Diagram). Nominal frequency ($f_{NOM}$) always appears at 1Q0 and the other outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the REF and FB inputs will be $f_{NOM}$ when the output connected to FB is undivided. The frequency of the REF and FB inputs will be $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication by using a divided output as the FB input.
3. When the FS pin is selected HIGH, the REF input must not transition upon power-up until $V_{CC}$ has reached 2.8V.
4. FB connected to an output selected for "zero" skew (ie., xF1 = xF0 = MID).
6. These inputs are normally wired to $V_{CC}$, GND, or left unconnected (actual threshold voltages vary as a percentage of $V_{CC}$). Internal termination resistors holds unconnected inputs at $V_{CC}/2$. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional $t_{LOCK}$ time before all datasheet limits are achieved.
7. The part should be tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only.
11. Test measurement levels are TTL levels (1.5V to 1.5V). Test conditions assume signal transition times of 2ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
12. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
13. Skew is defined as the time between the earliest and the latest output transition among all outputs for which the same $t_U$ delay has been selected when all are loaded with 30pF and terminated with 50Ω to 2.06V.
14. $t_{SKEWPR}$ is defined as the skew between a pair of outputs (xQ0 and xQ1) when all eight outputs are selected for $0t_U$.
15. $t_{SKEW0}$ is defined as the skew between outputs when they are selected for $0t_U$. Other outputs are divided or inverted but not shifted.
16. $C_L$ = 0pF. For $C_L$ = 30pF, $t_{SKEW0}$ = 0.35ns
17. There are three classes of outputs: Nominal (multiple of $t_U$ delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
18. $t_{DEV}$ is the output-to-output skew between any two devices operating under the same conditions ($V_{CC}$ ambient temperature, air flow, etc.).
19. $t_{ODCV}$ is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in $t_{SKEW2}$ and $t_{SKEW4}$ specifications.
20. $t_{PWH}$ is measured at 2.0V. $t_{PWL}$ is measured at 0.8V.
21. $t_{ORISE}$ and $t_{OFALL}$ measured between 0.8V and 2.0V.
22. $t_{LOCK}$ is the time that is required before synchronization is achieved. This specification is valid only after $V_{CC}$ is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until $t_{PD}$ is within specified limits.

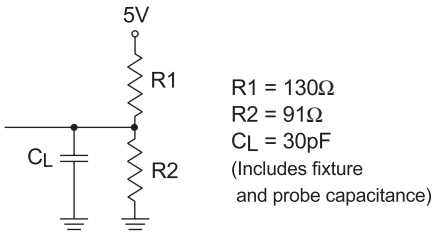
## DC Characteristics Over the Operating Range

| Symbol | Parameter | Test Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = –16mA | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 46mA | | 0.45 | |
| $V_{IH}$ | Input HIGH Voltage of REF, FB inputs | | 2.0 | $V_{CC}$ | |
| $V_{IL}$ | Input LOW Voltage of REF, FB inputs | | –0.5 | 0.8 | |
| $V_{IH3}$ | Input HIGH Voltage of 3-level inputs TEST, FS, xFn(6) | MIN ≤ $V_{CC}$ ≤ Max | $V_{CC}$ –0.85 | $V_{CC}$ | |
| $V_{IM3}$ | Input MID Voltage of 3-level inputs TEST, FS, xFn(6) | | $V_{CC}$/2 –0.5 | $V_{CC}$/2 +0.5 | |
| $V_{IL3}$ | Input LOW Voltage of 3-level inputs TEST, FS, xFn(6) | | | 0.85 | |
| $\|I_{IN}\|$ | Input Leakage Current of REF, FB inputs | $V_{IN}$ = $V_{CC}$ or 0.4V<br>$V_{CC}$ = Max | | 10 | µA |
| $\|I_3\|$ | 3-level Input DC Current (TEST, FS, nF1:0) | $V_{IN}$ = $V_{CC}$ (HIGH level) | | 200 | |
| | | $V_{IN}$ = $V_{CC}$/2 (MID level) | | 50 | |
| | | $V_{IN}$ = GND (LOW level) | | 200 | |
| $I_{OS}$ | Short Circuit Current(7) | $V_{CC}$ = Max, $V_{OUT}$ = GND (25° only) | | –250 | mA |
| $I_{CCQ}$ | Operating Current used by Internal Circuitry | $V_{CCN}$ = $V_{CCQ}$ = Max, All Input Selects Open | | 85 | |
| $I_{CCN}$ | Output Buffer Current per Output Pair | $V_{CCN}$ = $V_{CCQ}$ = Max, $I_{OUT}$ = 0mA Input Selects Open, $f_{MAX}$ | | 14 | |
| PD | Power Dissipation per Output Pair | | | 78 | |

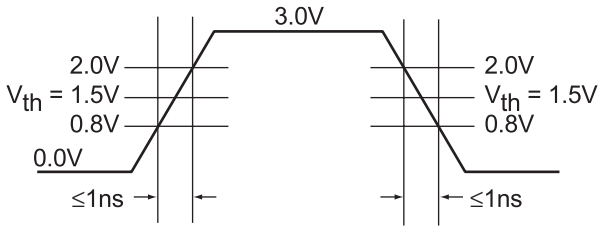
## Capacitance at REF and FB

| Parameter | Description | Test Conditions | Max. | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5.0V | 10 | pF |

## AC Test Loads and Waveforms (PI6C991)




TTL AC Test Load(16)

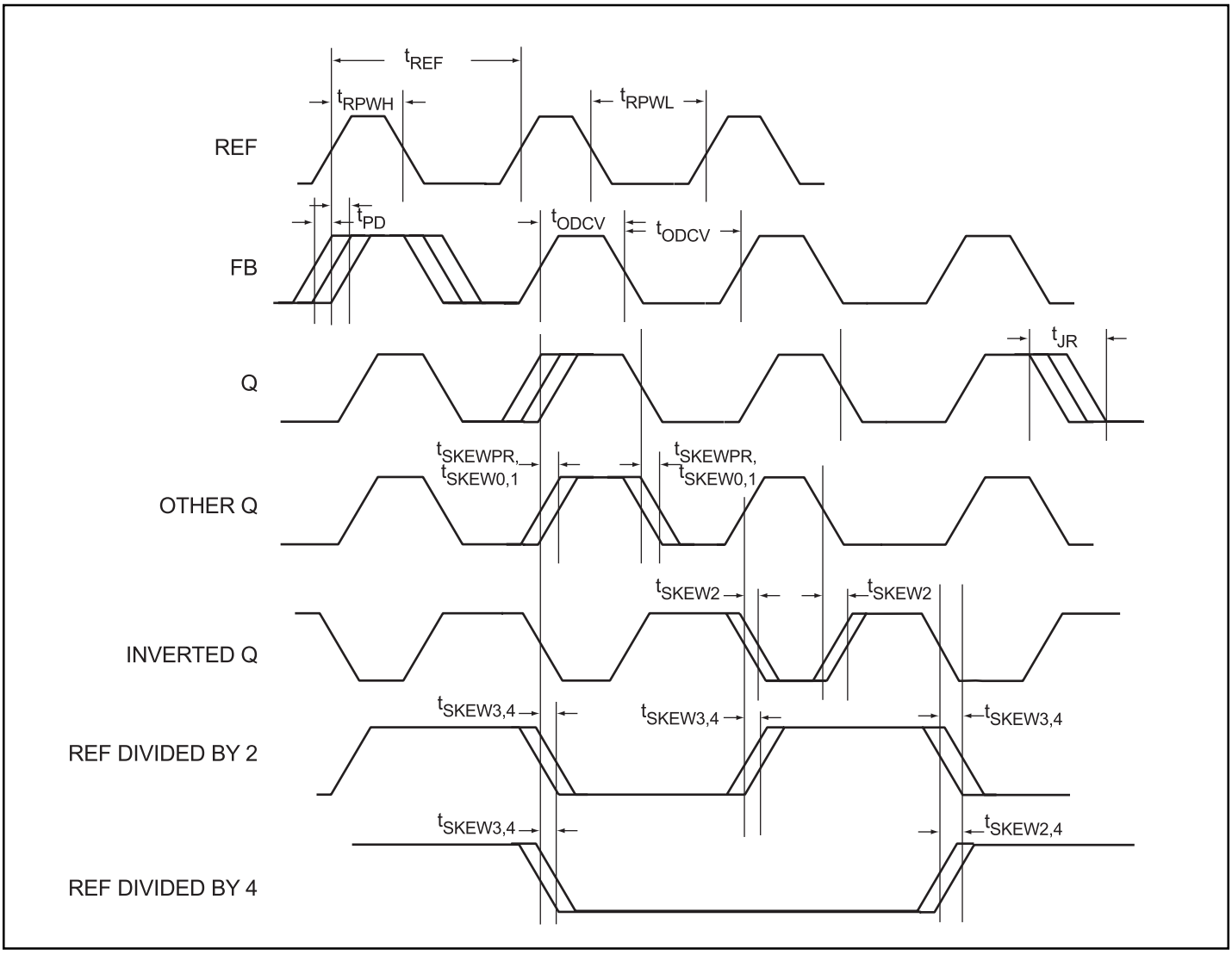



TTL Input Test Waveform

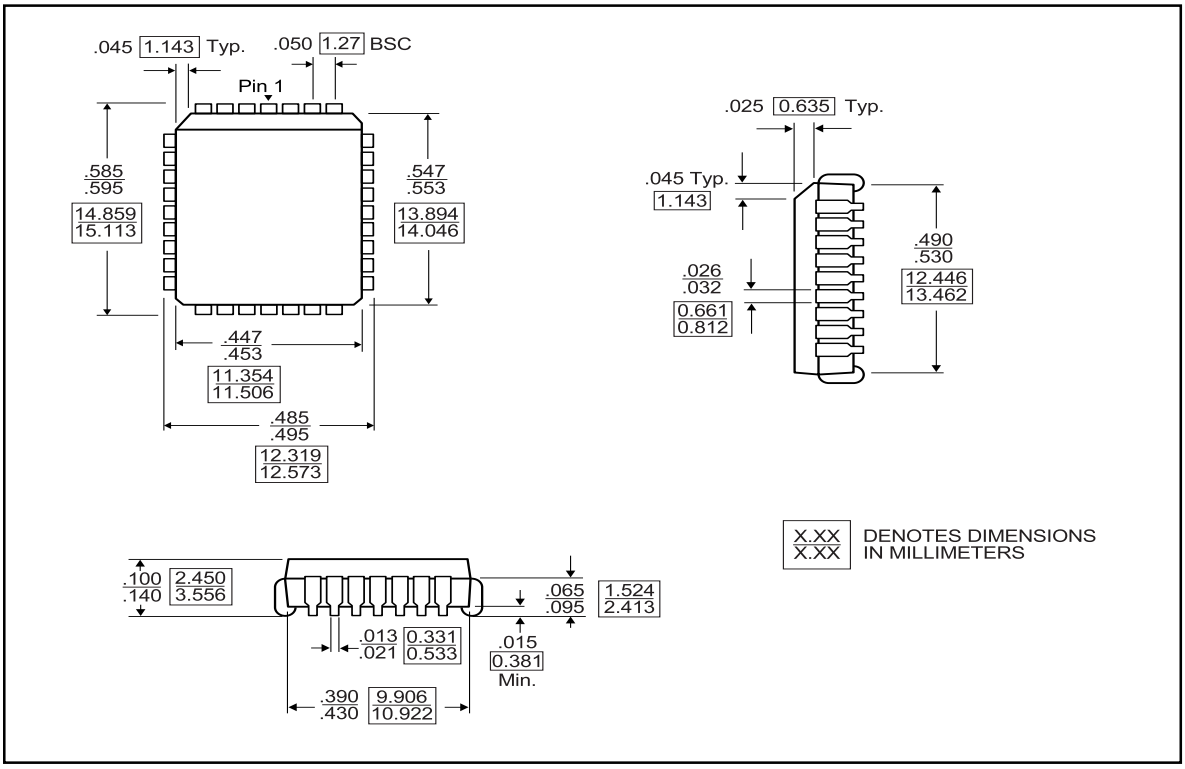
## Switching Characteristics over the Operating Range[2,11]

| Parameter | Description | | PI6C991-2 | | | PI6C991-5 | | | PI6C991 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. |
| $F_{NOM}$ | Operating clock Frequency in MHz | FS = LOW[1,2] | 15 | | 30 | 15 | | 30 | 15 | | 30 |
| | | FS = MID[1,2] | 25 | | 50 | 25 | | 50 | 25 | | 50 |
| | | FS = HIGH[1,2,3] | 40 | | 80 | 40 | | 80 | 40 | | 80 |
| $t_{RPWH}$ | REF Pulse Width HIGH | | 5.0 | | | 5.0 | | | 5.0 | | |
| $t_{RPWL}$ | REF Pulse Width LOW | | | | | | | | | | |
| $t_U$ | Programmable Skew Unit | | See Table 1 | | | | | | | | |
| $t_{SKEWPR}$ | Zero Output Matched-Pair Skew (xQ0, xQ1)[13,14] | | | 0.05 | 0.20 | | 0.1 | 0.25 | | 0.1 | 0.25 |
| $t_{SKEW0}$ | Zero Output Skew (All Outputs)[13,15] | | | 0.10 | 0.25 | | 0.25 | 0.5 | | 0.3 | 0.75 |
| $t_{SKEW1}$ | Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)[13,17] | | | 0.25 | 0.5 | | 0.6 | 0.7 | | 0.6 | 1.0 |
| $t_{SKEW2}$ | Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)[13,17] | | | 0.30 | 0.5 | | 0.50 | 1.0 | | 1.0 | 1.5 |
| $t_{SKEW3}$ | Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[13,17] | | | 0.25 | 0.5 | | 0.50 | 0.7 | | 0.7 | 1.2 |
| $t_{SKEW4}$ | Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)[13,17] | | | 0.50 | 0.9 | | 0.50 | 1.0 | | 1.2 | 1.7 |
| $t_{DEV}$ | Device-to-Device Skew[12,18] | | | | 0.75 | | | 1.25 | | | 1.65 |
| $t_{PD}$ | Propagation Delay, REF Rise to FB Rise | | –0.25 | 0 | 0.25 | –0.5 | 0 | 0.5 | –0.7 | 0.0 | +0.7 |
| $t_{ODCV}$ | Output Duty Cycle Variation[19] | | –0.65 | 0 | 0.65 | –1.0 | 0 | 1.0 | –1.2 | 0.0 | +1.2 |
| $t_{PWH}$ | Output HIGH Time Deviation from 50%[20] | | | | 2.0 | | | 2.0 | | | 3.0 |
| $t_{PWL}$ | Output LOW Time Deviation from 50%[20] | | | | 1.5 | | | 2.5 | | | 3.5 |
| $t_{ORISE}$ | Output Rise Time[21] | | 0.15 | 1.0 | 1.2 | 0.15 | 1.0 | 1.5 | 0.15 | 1.5 | 2.5 |
| $t_{OFALL}$ | Output Fall Time[21] | | 0.15 | 1.0 | 1.2 | 0.15 | 1.0 | 1.5 | 0.15 | 1.5 | 2.5 |
| $t_{LOCK}$ | PLL Lock Time[22] | | | | 0.5 | | | 0.5 | | | 0.5 |
| $t_{JR}$ | Cycle-to Cycle Output Jitter | RMS[12] | | | 25 | | | 25 | | | 25 |
| | | Peak-to-Peak[12] | | | 200 | | | 200 | | | 200 |

## AC Timing Diagrams



## Package Diagram 32-Pin PLCC (J32)




## Ordering Information

| Accuracy (ps) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 250 | PI6C991-2J | J32 | 32-Lead Plastic Leaded Chip Carrier (PLCC) | Commercial |
| 500 | PI6C991-5J | | | |
| | PI6C991-5IJ | | | Industrial |
| 750 | PI6C991J | | | Commercial |
| | PI6C991-IJ | | | Industrial |