PI74FCT16511T
PI74FCT162511T

Fast CMOS 16-Bit Registered/Latched Transceiver With Parity

Product Features

Common Features

- PI74FCT16511 and PI74FCT162511 are high-speed, low power devices with high current drive.
- Vcc = 5V ±10%
- Typical tsk(o) (Output Skew) < 250ps, clocked mode
- Extended range of –40°C to +85°C
- Hysteresis on all inputs
- Packages available:
  – 56-pin 240 mil wide TSSOP (A)
  – 56-pin 300 mil wide SSOP (V)

PI74FCT16511T Features

- High output drive: I_{OH} = –32mA; I_{OL} = 64mA
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C

PI74FCT162511T Features

- High output drive: I_{OL}/I_{OH} = 24mA
- Open drain parity error allows wire-OR
- Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- Balanced output drivers: ±24mA
- Series current limiting resistors

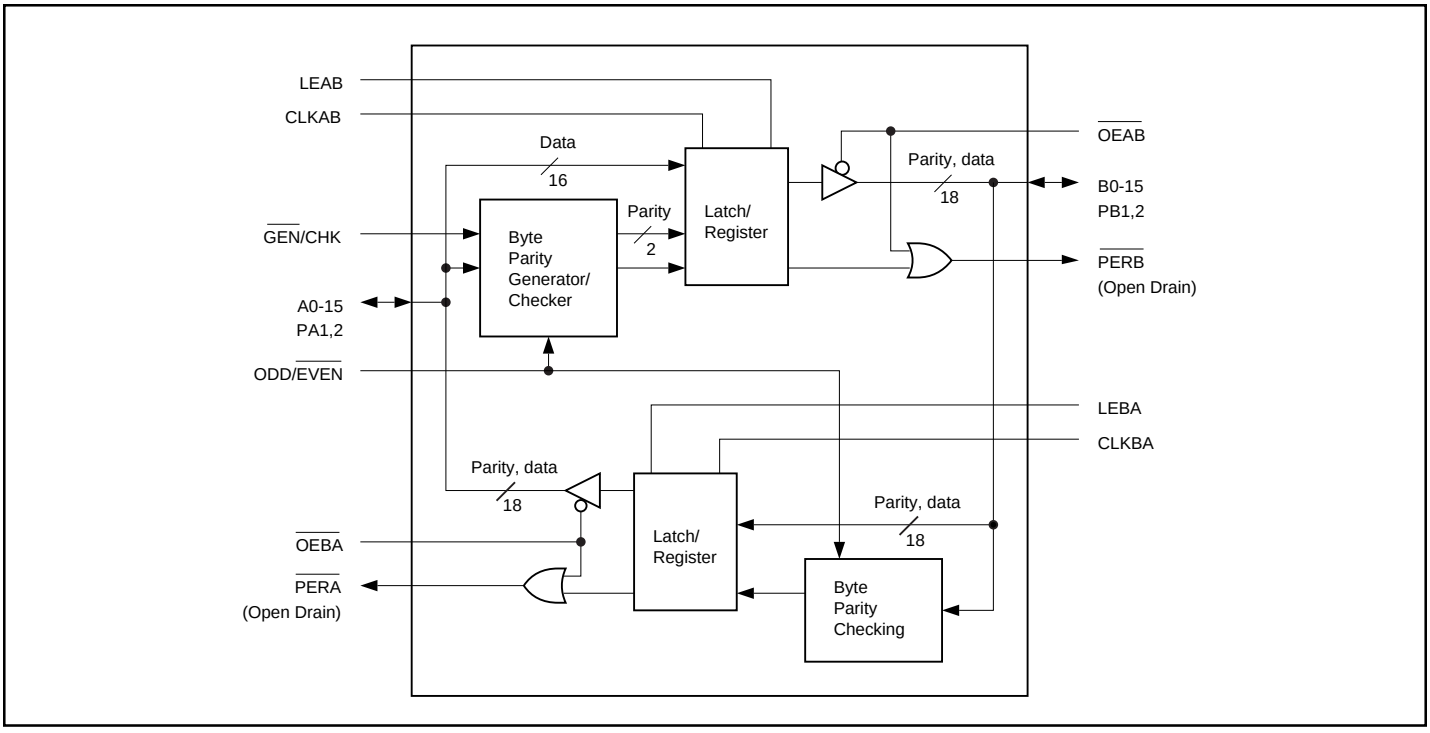
Product Description

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT16511T and PI74FCT162511T are high-speed, low-power 16-bit registered/latched transceiver with parity which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched or clocked modes. It has a parity generator/checker in the A-to-B direction and a parity checker in the B-to-A direction. Error checking is done at the byte level with separate parity bits for each byte. One error flag for each direction (A-to-B or B-to-A) exists to indicate an error for either byte in either direction. The parity error flags which are open drain outputs, can be tied together and/or tied with flags from other devices to form a single error flag or interrupt. To disable the error flag during combinational transitions, a designer can disable the parity error flag by the $\overline{OExx}$ control pins.

The operation in A-to-B direction is controlled by LEAB, CLKAB and $\overline{OEAB}$ control pins, and the operation in B-to-A direction is controlled by LEBA, CLKBA and $\overline{OEBA}$ control pins. $\overline{GEN}$/CHK is used to select the operation of A-to-B direction, while B-to-A direction is always in checking mode. The ODD/$\overline{EVEN}$ select is common between the two directions. Independent operation can be achieved between the two directions by using the corresponding control lines except for the ODD/$\overline{EVEN}$ control.

Simplified Logic Block Diagram



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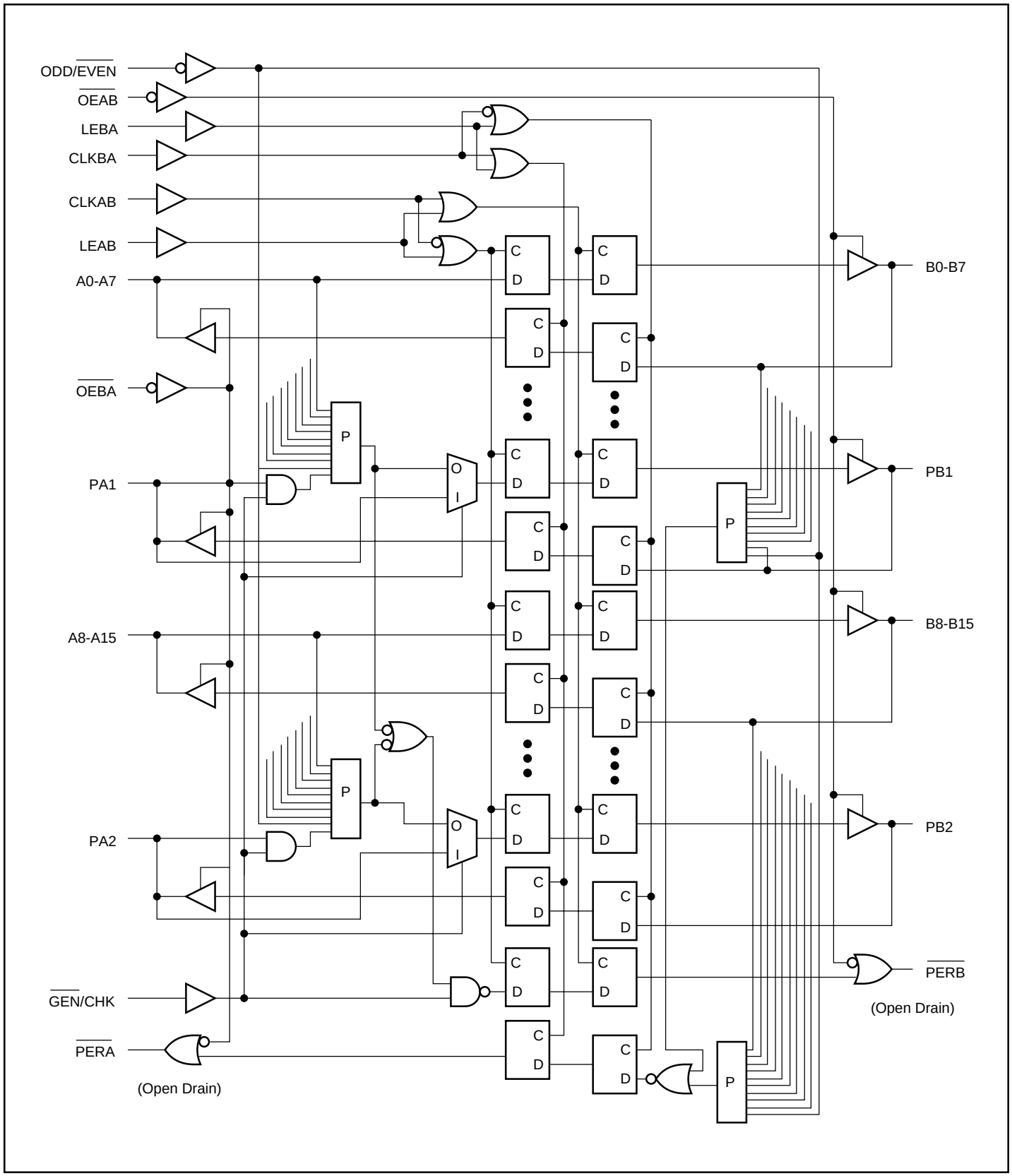
Logic Block Diagram

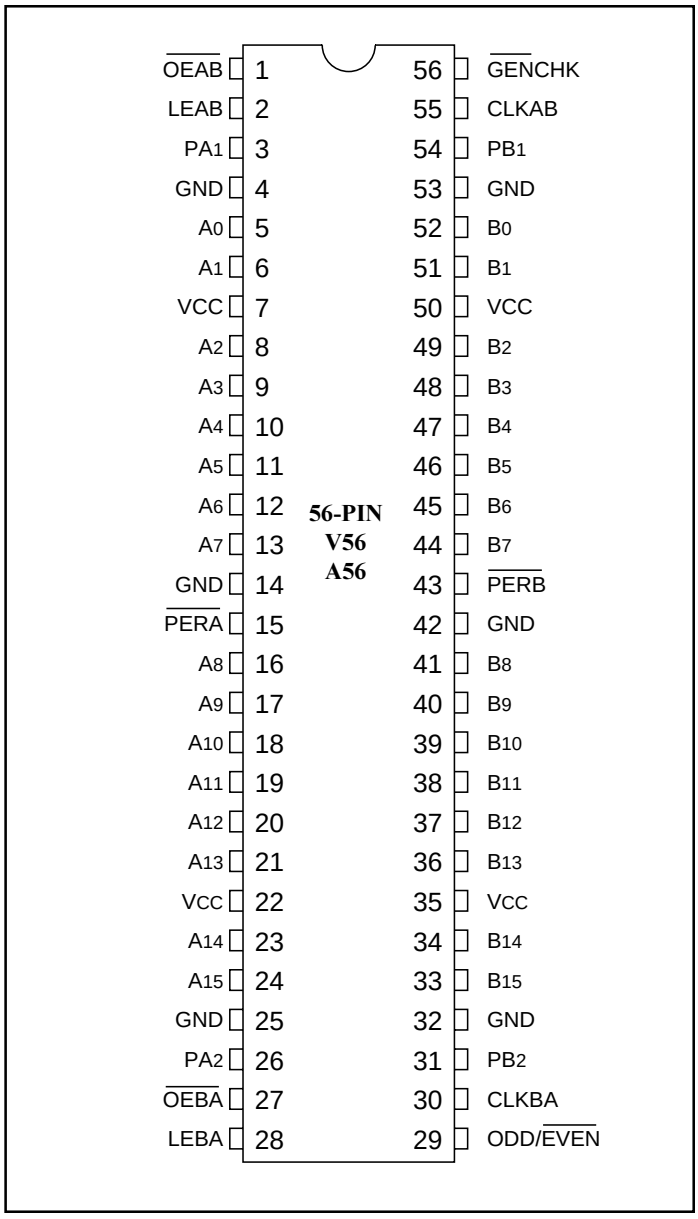


Product Pin Description

Pin Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{PERA}$	Parity Error (Open Drain) on A Outputs
$\overline{PERB}$	Parity Error (Open Drain) on B Outputs
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or B-to-A 3-State Outputs
ODD/$\overline{EVEN}$(1)	Parity Mode Selection Input
$\overline{GEN}$/CHK(1)	A-to-B Port Generate or Check Mode Input
PAx(2)	A-to-B Parity Input, B-to-A Parity Output
PBx	B-to-A Parity Input, A-to-B Parity Output
GND	Ground
VCC	Power

NOTES:
1. ODD/$\overline{EVEN}$ and $\overline{GEN}$/CHK should be tied to VCC or GND with no resistor for optimum results.
2. The PAx pin input is internally disabled during parity generation. This means that when generating parity in the A-to-B direction, there is no need to add a pull-up resistor to guarantee state. The pin will still function properly as the parity output for the B-to-A direction.

Product Pin Configuration



Capacitance (T_A = 25°C, f = 1 MHz)

Parameters(1)	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF
C_O	Open Drain Capacitance	V_{OUT} = 0V	4.5	6.0	pF

Note:
1. This parameter is determined by device characterization but is not production tested.

Truth Table[1,2]

Inputs				Output Buffers
$\overline{OEAB}$	LEAB	CLKAB	Ax	Bx
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L	X	B[3]
L	L	H	X	B[4]

NOTES:
1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care or Irrelevant
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition
2. A-to-B data flow is shown. B-to-A flow control is the same, except using $\overline{OEBA}$, LEBA, and CLKBA.
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, assuming CLKAB was HIGH before LEAB went LOW.

Truth Table (Parity Generation) [1, 2, 3, 4, 5]

A0 - A7, Total Number of Inputs that are high	ODD/$\overline{EVEN}$	PB1
1, 3, 5 or 7	L	H
1, 3, 5 or 7	H	L
0, 2, 4, 6 or 8	L	L
0, 2, 4, 6 or 8	H	H

NOTES:
1. Conditions shown are for $\overline{GEN}$/CHK = L, $\overline{OEAB}$ = L, $\overline{OEBA}$ = H.
2. A-to-B parity generation is shown. B-to-A can check parity while A-to-B is performing generation. B-to-A will not generate parity.
3. The response shown is for LEAB = H. If LEAB = L, then CLKAB will control as an edge triggered clock.
4. Conditions shown are for the byte A0-A7. The byte A8-A15 is similar but will output the parity on PB2.
5. The error flag $\overline{PERB}$ will remain in a high state during parity generation.

Truth Table (Parity Checking) [1, 2, 3, 4]

A0 - A7 and PA1[5], Total Number of Inputs that are high	ODD/$\overline{EVEN}$	$\overline{PERB}$
1, 3, 5, 7 or 9	L	L
1, 3, 5, 7 or 9	H	H[6]
0, 2, 4, 6 or 8	L	H[6]
0, 2, 4, 6 or 8	H	L

NOTES:
1. Conditions shown are for $\overline{GEN}$/CHK = H, $\overline{OEAB}$ = L, $\overline{OEBA}$ = H.
2. A-to-B parity checking is shown. B-to-A parity checking is same but uses $\overline{OEBA}$ = L, $\overline{OEAB}$ = H and errors will be indicated on $\overline{PERA}$.
3. In parity checking mode the parity bits will be transmitted unchanged along with the corresponding data regardless of parity errors. (PB1 = PA1)
4. The response shown is for LEAB = H. If LEAB = L, then CLKAB will control as an edge triggered clock.
5. Conditions shown are for the byte A0-A7 and PA1. The byte A8-A15 and PA2 is same.
6. The parity error flag $\overline{PERB}$ is a combined flag for both bytes A0-A7 and A8-A15. If a parity error occurs on either byte $\overline{PERB}$ will go low.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Ambient Temperature with Power Applied ..... –40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only) ..... –0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) .. –0.5V to +7.0V
DC Input Voltage ..... –0.5V to +7.0V
DC Output Current 120mA
Power Dissipation 1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description		Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{IH}	Input HIGH Voltage		Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage		Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	(Input pins)	V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
		(I/O pins)					–1	
I_{IL}	Input LOW Current	(Input pins)	V_{CC} = Max.	V_{IN} = GND			1	µA
		(I/O pins)					–1	
I_{OZH}	High Impedance		V_{CC} = Max.	V_{OUT} = 2.7V			1	µA
I_{OZL}	Output Current			V_{OUT} = 0.5V			–1	µA
V_{IK}	Clamp Diode Voltage		V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current (I/O pins)		V_{CC} = Max.[3], V_{OUT} = GND		–80	–140	–225	mA
I_O	Output Drive Current (I/O pins)		V_{CC} = Max.[3], V_{OUT} = 2.5V		–50		–180	mA
I_{OFF}	Output Leakage Current (Open Drain)		V_{CC} = Max., V_{OUT} = 4.5V				±100	µA
V_H	Input Hysteresis					100		mV

PI74FCT16511T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3.0 mA	2.5	3.5		V
			I_{OH} = –15.0 mA	2.4	3.5		
			I_{OH} = –32.0 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64 mA		0.2	0.55	V
I_{OFF}	Power Down Disable	V_{CC} = 0V, V_{IN} or V_{OUT} ≤4.5V		—	—	±100	µA

PI74FCT162511T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –24.0 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA		0.3	0.55	V
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CCL}, I_{CCH}, I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]		0.5	1.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $\overline{OEAB}$ = GND $\overline{OEBA}$ = V_{CC} One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10 MHz (CLKAB) 50% Duty Cycle $\overline{LEAB}$ = $\overline{OEAB}$ = GND $\overline{OEBA}$ = V_{CC} f_i = 5 MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND		0.8	1.7[5]	mA
			V_{IN} = 3.4V V_{IN} = GND		1.3	3.2[5]	
		V_{CC} = Max., Outputs Open f_{CP} = 10 MHz (CLKAB) 50% Duty Cycle $\overline{LEAB}$ = $\overline{OEAB}$ = GND $\overline{OEBA}$ = V_{CC} f_i = 2.5 MHz 18 Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND		3.8	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND		9.0	21.8[5]	

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_I = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

16511T/162511T Switching Characteristics over Operating Range (Propagation Delays)

Parameters	Description	Conditions[1]	16511/162511T Com. Min	16511/162511T Com. Max	162511AT Com. Min	162511AT Com. Max	Unit
t_{PLH}	Propagation Delay	C_L = 50 pF	1.5	6.5	1.5	5.7	ns
t_{PHL}	PAx to PBx	R_L = 500Ω					
t_{PLH}	Propagation Delay		1.5	6.5	1.5	5.0	ns
t_{PHL}	Ax to Bx or Bx to Ax, PBx to PAx						
t_{PLH}	Propagation Delay		1.5	9.0	1.5	7.5	ns
t_{PHL}	Ax to PBx						
t_{PLH}[3]	Propagation Delay		1.5	10.5	1.5	9.0	ns
t_{PHL}	Ax to $\overline{PERB}$, PAx to $\overline{PERB}$		1.5	9.5	1.5	8.0	
t_{PLH}[3]	Propagation Delay		1.5	10.5	1.5	9.0	ns
t_{PHL}	Bx to $\overline{PERA}$, PBx to $\overline{PERA}$		1.5	9.5	1.5	8.0	
t_{PLH}	Propagation Delay		1.5	6.0	1.5	5.6	ns
t_{PHL}	LEBA to Ax and PAx						
	LEAB to Bx and PBx						
t_{PLH}[3]	Propagation Delay		1.5	7.5	1.5	7.0	ns
t_{PHL}	LEBA to $\overline{PERA}$, LEAB to $\overline{PERB}$		1.5	6.5	1.5	6.0	
t_{PLH}	Propagation Delay		1.5	6.0	1.5	5.6	ns
t_{PHL}	CLKBA to Ax and PAx						
	CLKAB to Bx and PBx						
t_{PLH}[3]	Propagation Delay		1.5	7.5	1.5	7.0	ns
t_{PHL}	CLKBA to $\overline{PERA}$		1.5	6.5	1.5	6.0	
	CLKAB to $\overline{PERB}$						
t_{PZH}	Output Enable Time		1.5	7.0	1.5	6.0	ns
t_{PZL}	$\overline{OEBA}$ to Ax and PAx						
	$\overline{OEAB}$ to Bx and PBx						
t_{PHZ}	Output Disable Time[4]		1.5	7.0	1.5	5.6	ns
t_{PLZ}	$\overline{OEBA}$ to Ax and PAx						
	$\overline{OEAB}$ to Bx and PBx						
t_{PLZ}[3]	Parity ERROR Enable		1.5	6.0	1.5	6.0	ns
t_{PZL}	$\overline{OEBA}$ to $\overline{PERA}$, $\overline{OEAB}$ to $\overline{PERB}$		1.5	6.0	1.5	6.0	
t_{PLH}	ODD/$\overline{EVEN}$ to $\overline{PERB}$		1.5	10.0	1.5	10.0	ns
t_{PHL}			1.5	10.0	1.5	10.0	
t_{PLH}	ODD/$\overline{EVEN}$ to PBx		1.5	10.0	1.5	10.0	ns
t_{PHL}							

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. On Open Drain Outputs t_{PLH} is measured up to $V_{OUT} = V_{OL} + 0.3V$.
4. This parameter is guaranteed but not production tested.

PI74FCT16511T/162511T Switching Characteristics over Operating Range (Setup Times)

Parameters	Description	Conditions[1,3]			16511/162511T Com. Min.	16511/162511T Com. Max.	162511AT Com. Min.	162511AT Com. Max.	Unit
t_{SU}	Setup Time HIGH or LOW Ax to CLKAB	$\overline{GEN}$/CHK LOW	PBx valid	C_L = 50 pF R_L = 500Ω	6.5	—	4	—	ns
			PBx not valid		3	—	3	—	ns
		$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid		6.5	—	4	—	ns
			$\overline{PERB}$ not valid		3	—	3	—	ns
t_{SU}	Setup Time PAx to CLKAB	$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid		6.5	—	4	—	ns
			$\overline{PERB}$ not valid		3	—	3	—	ns
t_{SU}	Setup Time Bx to CLKBA PBx to CLKBA		$\overline{PERA}$ valid		6.5	—	4	—	ns
			$\overline{PERA}$ not valid		3	—	3	—	ns
t_{SU}	Setup Time Ax to LEAB	CLKAB LOW	PBx valid		6.5	—	3.5	—	ns
		$\overline{GEN}$/CHK LOW	PBx not valid		3	—	3	—	ns
		CLKAB LOW	$\overline{PERB}$ valid		6.5	—	3.5	—	ns
		$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ not valid		3	—	3	—	ns
		CLKAB HIGH	PBx valid		6.5	—	3.5	—	ns
		$\overline{GEN}$/CHK LOW	PBx not valid		3	—	3	—	ns
		CLKAB HIGH	$\overline{PERB}$ valid		6.5	—	3.5	—	ns
		$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ not valid		3	—	3	—	ns
t_{SU}	Setup Time PAx to LEAB	CLKAB LOW	$\overline{PERB}$ valid		6.5	—	3.5	—	ns
		$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ not valid		3	—	3	—	ns
		CLKAB HIGH	$\overline{PERB}$ valid		6.5	—	3.5	—	ns
		$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ not valid		3	—	3	—	ns
t_{SU}	Setup Time Bx to LEBA PBx to LEBA	CLKBA LOW	$\overline{PERA}$ valid		6.5	—	3.5	—	ns
			$\overline{PERA}$ not valid		3	—	3	—	ns
		CLKAB HIGH	$\overline{PERA}$ valid		6.5	—	3.5	—	ns
			$\overline{PERA}$ not valid		3	—	3	—	ns

PI74FCT16511T/162511T Switching Characteristics over Operating Range (Hold Times)

Parameters	Description	Conditions[1]	16511/162511T Com. Min.	16511/162511T Com. Max.	16511/162511AT Com. Min.	16511/162511AT Com. Max.	Unit
t_H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA	C_L = 50 pF R_L = 500Ω	1	—	1	—	ns
t_H	Hold Time HIGH or LOW PAx to LEAB		1	—	1	—	ns
t_H	Hold Time HIGH or LOW PBx to LEBA		1	—	1	—	ns
t_H	Hold Time Ax to CLKAB, PAx to CLKAB		1	—	1	—	ns
t_H	Hold Time Bx to CLKBA, PBx to CLKBA		1	—	1	—	ns
t_W	LEAB or LEBA Pulse Width HIGH[2]		3	—	3	—	ns
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW[2]		3	—	3	—	ns

Notes:
1. See test circuit and wave forms.
2. This parameter is guaranteed but not production tested.
3. "Not valid" means the setup time indicated is not sufficient to assure proper functioning of this output; however, the set-up time indicated will assure proper functioning of the A-to-B or B-to-A port respective to the indicated direction.