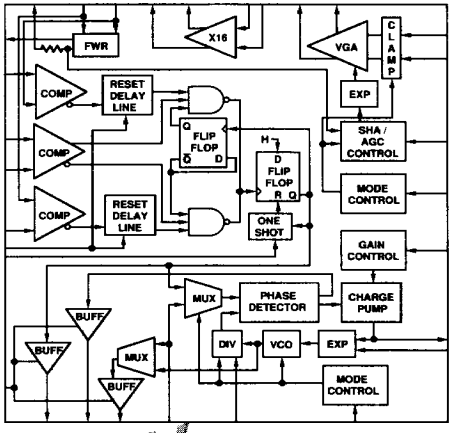
40 Mb/s Fully Integrated Disk Drive Read Channel

AD897

FEATURES

- **40 Mb/s Data Transfer Rate Capability**
- **500 ps (max) Additional Pulse Pairing**
- **30 dB Gain VGA with 40 dB Control Range**
- **24 dB Buffer with 200 Ω Differential Load Drive Capabilities**
- **0.1 dB/ms Typical Gain Drift in Hold Mode**
- **Symmetrical and User Programmable AGC Attack/Decay Times**
- **Three Levels of Data Qualification**
  - **Amplitude Threshold**
  - **Time Above Threshold**
  - **Data Polarity**
- **Offset Trimmed Zero Crossing Comparator**
- **±1 ns (max) PLL Window Uncertainty**
- **Zero Phase Error VCO Start-Up**
- **No Phase Detector Dead Band at Center of Decode Window**
- **Exponential VCO Control**
- **52-Pin PQFP Package, +5 V and +12 V Supplies**

AD897 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD897 is a complete solution for recovering binary information in a hard disk drive with data transfer rates up to 40 megabits per second. It is connected to the output of the head amplifier and performs the signal conditioning, data qualification and data synchronization tasks with a minimum of external components.

The AD897 has the flexibility to perform both continuous and sampled AGC functions; it is also ideal for embedded, dedicated, or mixed servo applications. Fast acquisition and low droop while in the hold mode allow for the AGC operation to be performed within the sector header without compromising channel behavior when reading data.

Three levels of data qualification are provided: amplitude threshold, time above amplitude threshold, and data polarity. Level qualification is performed on positive and negative cycles of the data waveform using a user-defined threshold level which is applied to the level qualification comparators. Each comparator then drives a resettable delay line, which implements the time above threshold qualification. Once the first two valid criteria have been satisfied, a third comparator is able to detect a zero crossings and clock a flip-flop if the data also exhibits the correct polarity. Each clocking of the flip-flop causes a second flip-flop to toggle and thereby implement the polarity check. The valid data event also triggers an output one-shot, with a user-defined pulse width.

The data synchronizer section provides four modes of operation: lock to external clock, lock to preamble, lock to data, and tristate. The phase detector/charge pump utilizes a tri-phase pump-up, pump-down, pump-up approach in the lock to data mode, thereby ensuring no dead band zone in the center of the window. In addition, when switching to the lock to data mode, zero-phase error start-up is initiated. In the lock to external clock mode, feedback dividers provide the capability to achieve VCO to external clock ratios of 1:2, 1:1, 3:2, 2:1. When switching PLL operating modes, the charge pump is temporarily tristated to prevent the VCO control voltage from being disturbed.

The AD897 is available in a 52-pin plastic flat pack package (PQFP) and is specified to operate over the commercial (0 to +70°C) temperature range.

SPECIFICATIONS

PEAK DETECTOR SECTION (@ +25°C, +5 V, +12 V dc, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
VARIABLE GAIN AMPLIFIER					
Maximum Gain[1]		**29**	30	**31**	dB
Gain Variation	T_{min} to T_{max}	−0.3		0.7	dB
±3 dB Bandwidth	Up to 40 dB Gain Reduction	40	60		MHz
Input Voltage Noise	0 dB Gain Reduction		6		nV/√Hz
Input Signal Range	p–p Differential	10		200	mV
Input Resistance	Differential	20	24		kΩ
Input Capacitance	Differential		1	5	pF
Output Impedance	Differential, f = 1 MHz		10	20	Ω
Harmonic Distortion	40 dB Gain, 10 mV p–p Differential Input			0.25	%
	14 dB Gain, 200 mV p–p Differential Input			2	%
Output DC Level			6.7		V
Control Range	Set Gain Mode	**36**	40		dB
Control Sensitivity	Set Gain Mode (Per 20 mV Input)		−1		dB
Control Linearity	Set Gain Mode (26 dB VGA Range)			**±0.5**	dB
VGA Level Set Input Range	Set Gain Mode (For Specified Accuracy)	**0**		**800**	mV
	Nondestructive Input Range	−0.3		V_{12}	V
VGA Level Set Input Current				−50	µA
INPUT CLAMP[2]					
Turn-On Time				100	ns
Turn-Off Time				100	ns
Input Signal Attenuation	200 Ω Source Resistance		34		dB
On-State Input Impedance	Differential		40		Ω
GAIN OF 16 BUFFER					
Gain	f = 1 MHz	**23.5**	24	**24.5**	dB
Gain Variation	T_{min} to T_{max}	−0.5		0.5	dB
±3 dB Bandwidth		60			MHz
Input Voltage Noise			8		nV/√Hz
Input Resistance	Differential	20	24		kΩ
Input Capacitance	Differential		1	5	pF
Input Common-Mode Range			TBD		V
Output Impedance	Differential, f = 1 MHz		10	20	Ω
Harmonic Distortion	1 V p–p Differential Output, 200 Ω Load			0.5	%
Output Signal Level	p–p Differential			4	V
Output DC Level			5.75		V
FULL WAVE RECTIFIER					
Input Signal Level	p–p Differential			4	V
−3 dB Bandwidth		70			MHz
Input Resistance	Differential	8	10		kΩ
Input Capacitance	Differential		1	5	pF
DC Offset[3]	Relative to the Reference Voltage			**±30**	mV
Output Impedance			10	20	Ω
Peak Detector V_{REF}		4.2		5.0	V
AGC CONTROL SECTION					
Attack Time (Slow)	AGC Acquire Gain = "0"				
	26 dB Gain Step – 1000 pF C_{SAMPLE}		10		µs
	26 dB Gain S – <50 pF C_{SAMPLE}		1.2		µs
Attack Time (Fast)	AGC Acquire Gain = "1"				
	26 dB Gain Step – 1000 pF C_{SAMPLE}		1.0		µs
	26 dB Gain Step – <50 pF C_{SAMPLE}		120		ns
Hold–Droop	1 dB Gain Change – 1000 pF C_{SAMPLE}		10		ms
Dynamic Range	AGC Acquire Mode		TBD		dB
AGC Level Range	AGC Acquire Mode (@ S/H Rectifier)	0.5		2.0	V
Control Sensitivity	AGC Acquire Mode (Per 10 mV Input)		5		mV
AGC Level Set Input Range	For Specified Accuracy	**200**		**600**	mV
	Nondestructive Input Range	−0.3		V_{CC}	V
AGC Level Set Input Current				−50	µA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	Conditions	Min	Typ	Max	Units
COMPARATORS					
Input Offset Voltage			1	2.0	mV
Input Offset Current			TBD		pA
Input Bias Current			200	1000	pA
Open-Loop Gain	f = 10 MHz		TBD		dB
Input Resistance	Differential		100		kΩ
Input Capacitance	Differential		1	5	pF
Input Common-Mode Range	Referred to Digital Ground		TBD		V
RESETTABLE DELAY LINE					
Resistor Scaling[4]			Delay ≈ 2+7.5 × R_{SET}		ns
Pulse Duration	R_{SET} = 1 kΩ		TBD		ns
	R_{SET} = 5 kΩ		TBD		ns
Resistor Range	R_{SET} = R_{min} to R_{max}		TBD		kΩ
OUTPUT ONE SHOT					
Resistor Scaling			One Shot Pulse ≈ 6+4.5 × R_{SET}		ns
Pulse Duration	R_{SET} = R_{min} to R_{max}		TBD		ns
	R_{SET} = 30 kΩ		TBD		ns
	R_{SET} = 10 kΩ		TBD		ns
Resistor Range	R_{SET} = R_{min} to R_{max}		TBD		kΩ
DATA THROUGHPUT					
Additional Pulse Pairing[5]			100	500	ps
Max Transfer Rate		40			Mb/s

NOTES

[1]Over the full 60 MHz bandwidth of the AD897, the worst case rms signal-to-noise ratio is 40 dB or better with a 40 dB AGC range.

[2]Clamp Operation is specified with a source impedance of 200 Ω in series with 0.1 μF.

[3]Measured using a 4 kΩ resistor connected between rectified signal to derive threshold pin (Pin 15) and Ground.

[4]R_{SET} specified in kΩ.

[5]Measurements were performed using a 100 mV sine wave applied to the input of the VGA. The resultant pulse pairing is the difference in delay times for two consecutive output pulses at the raw data output.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

AGC MODE CONTROL

Control Line	AGC Mode Control 0	AGC Mode Control 1	AGC Acquire Gain
AGC Acquire with Slow Attack	0	0	0
AGC Acquire with Fast Attack	0	0	1
AGC Hold	0	1	X
VGA Gain Set	1	0	X
Input Clamp	1	1	X

X = Do not care.

SPECIFICATIONS

PLL SECTION (@ + 25°C, +5 V, +12 V dc, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
PHASE DETECTOR					
Phase Detector Range			$\pm\pi$		Radians
Gain	Data Updates n Clock Cycles Apart		$1/n2\pi$		1/Radians
CHARGE PUMP					
Gain	Minimum Gain Mode	80	100	120	μA
	Nominal Gain Mode	160	200	240	μA
	Maximum Gain Mode	320	400	480	μA
VCO/EXPONENTIATOR					
Frequency		10		60	MHz
Range	Fixed Frequency		4:1		
Gain		1.10ω	1.40ω	1.65ω	(Rad/s)/V
WINDOW STROBE					
Range			$\pm T_W/2$		Seconds
Sensitivity	Per 10 mV Input on Window Strobe Control				
Control Line Input Range	Relative to Analog V_S	−1		1	V
Control Line Input Current				50	μA
WINDOW LOSS					
Jitter (6σ)	Lock to Data Mode with Minimum Gain		1	1.5	ns
Window Center Offset	Lock to Data with Nominal Gain			1% ±1 ns	% of T_W
Zero Phase Start-Up					
Accuracy	Lock to External CLK or Data Mode		1	1.5	ns
Static Window Loss	Lock to Data Mode with Minimum Gain				% of T_W
DATA THROUGHPUT					
Max Data Transfer Rate	RLL 1, 7 Encoding	40			Mb/s
Max External Clock Frequency		60			MHz
External Clock to Synchronized Clock Delay	Lock to External Clock		4	6	ns

Specifications subject to change without notice.

PLL LOCK MODE CONTROL

Control Line	PLL Lock Mode Control 0	PLL Lock Mode Control 1	PLL Acquire Gain
Lock to External Clock (Charge Pump – 1/2 Nominal)	0	0	0
Lock to External Clock (Charge Pump – Nominal)	0	0	1
Lock to Preamble (Charge Pump – Nominal)	0	1	0
Lock to Preamble (Charge Pump – 2× Nominal)	0	1	1
Tristate	1	0	X
Lock to Data (Charge Pump – 1/2 Nominal)	1	1	0
Lock to Data (Charge Pump – Nominal)	1	1	1

X = Do not care.

VCO DIVIDER CONTROL

Control Line	Division Factor Bit 0	Division Factor Bit 1
Division Factor = 1	0	0
Division Factor = 2	0	1
Division Factor = 3	1	0
Division Factor = 4	1	1

MODE CONTROL AND OUTPUT PINS

Parameter	Conditions	Min	Typ	Max	Units
MODE CONTROL PINS	TTL Compatible CMOS Inputs				
V_{IH}		2.0		V_5+0.5	V
V_{IL}		V_{GND} −0.5		0.8	V
I_{IH}				1	nA
I_{IL}				1	nA
Mode Switching Times				50	ns
OUTPUT PINS	CMOS Compatible				
V_{OH}		4.0		V_5+0.5	V
V_{OL}		V_{GND} −0.5		1.0	V
I_{OH}		4			mA
I_{OL}		4			mA

Specifications subject to change without notice.

POWER SUPPLIES (@ +25°C, +5 V, +12 V dc, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage V_{12}		10.8	12	13.2	V
Supply Voltage V_5		4.5	5	5.5	V
Quiescent Current I_{12}	T_{min} to T_{max}		40	50	mA
Quiescent Current I_5	T_{min} to T_{max}		60	72	mA

Specifications subject to change without notice.

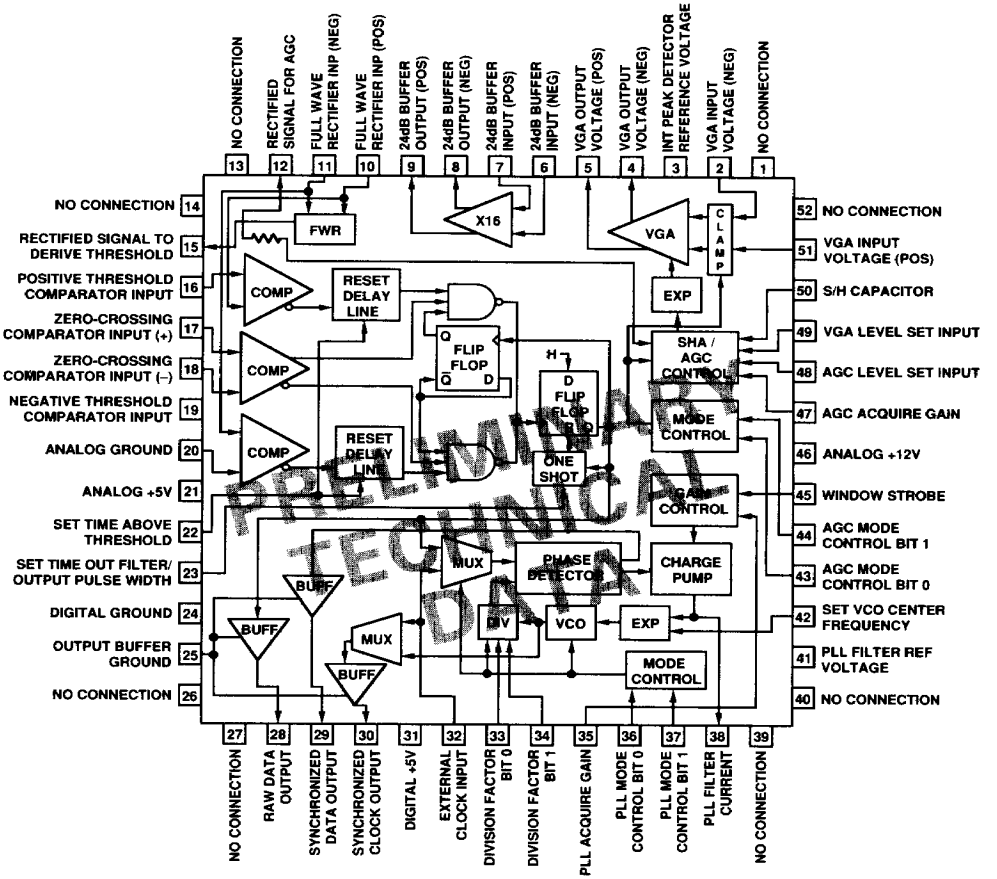
ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage V_{12}				14.5	V
Supply Voltage V_5				7.5	V
RF Input Stage Differential Input Voltage		−0.8		5.6	V
Comparator Differential Input Voltage		−0.8		5.6	V
Storage Temperature Range		−65		130	°C
Operating Temperature Range[2]		0		+70	°C
Lead Temperature Range	Soldering 60 sec			+300	°C

Notes
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute rating conditions for extended period may affect device reliability.
[2]52-pin PQFP package: θ_{JA} = 65°C/watt.

CONNECTION DIAGRAM

52-Pin PQFP



ORDERING GUIDE

Model	Description	Package Option*
AD897JS	52-Pin PQFP	S-52

*See Section 20 for package outline information.

Pin	Description	I/O Type	Application Notes
1	No Connection		May be left floating.
2	VGA Input Voltage (Neg)	Analog Voltage Input	
3	Internal Peak Detector Reference Voltage	Analog Voltage Output	+4.3 V reference is used to bias the full wave rectifier.
4	VGA Output Voltage (Neg)	Analog Voltage Output	Emitter follower output, biased at 6.5 V.
5	VGA Output Voltage (Pos)	Analog Voltage Output	Emitter follower output, biased at 6.5 V.
6	24 dB Buffer Output (Neg)	Analog Input Voltage	Internally based at 5 V.
7	24 dB Buffer Input (Pos)	Analog Voltage Input	Internally biased at 5 V.
8	24 dB Buffer Output (Neg)	Analog Voltage Output	Emitter follower output, biased at 6.5 V.
9	24 dB Buffer Output (Pos)	Analog Voltage Output	Emitter follower output, biased at 6.5 V.
10	Full Wave Rectifier Input (Pos)	Analog Voltage Input	Internally biased at 5 V.
11	Full Wave Rectifier Input (Neg)	Analog Voltage Input	Internally biased at 5 V.
12	Rectified Signal to AGC	Analog Voltage Output	Emitter follower output with 250 Ω in series. No internal pull-down is provided.
13	No Connection		May be left floating.
14	No Connection		May be left floating.
15	Rectified Signal to Derive Threshold	Analog Voltage Output	Emitter follower output. No internal pull-down is provided.
16	Positive Threshold Comparator Input	Analog Voltage Input	Threshold for positive amplitude comp.
17	Zero-Crossing Comparator Input (Pos)	Analog Voltage Input	DC biased through passive differentiator network.
18	Zero-Crossing Comparator Input (Neg)	Analog Voltage Input	DC biased through passive differentiator network.
19	Negative Threshold Comparator Input	Analog Voltage Input	Threshold for positive amplitude comp.
20	Analog Ground	Power Input	
21	Analog +5 V	Power Input	Decoupling with 0.1 μF‖0.01 μF required.
22	Set Time Above Threshold	Analog Current Input	Resistor/current programmable.
23	Set Time Out Filter/Output Pulse Width	Analog Current Input	Resistor/current programmable.
24	Digital Ground	Power Input	
25	Output Buffer Ground	Power Input	
26	No Connection		May be left floating.
27	No Connection		May be left floating.
28	Raw Data Output	Digital CMOS Output	Active high represents data pulse.
29	Synchronized Data Output	Digital CMOS Output	Active high data output pulse lasting one clock period. Synchronized to rising edge of synchronized clock.
30	Synchronized Clock Output	Digital CMOS Output	
31	Digital +5 V	Power Input	Decoupling with 0.1 μF‖0.01 μF required.
32	External Clock Input	TTL Input	Source clock divided by 2 internally.
33	Division Factor Bit 0	TTL Input	Sets division factor of VCO.
34	Division Factor Bit 1	TTL Input	Sets division factor of VCO.
35	PLL Acquire Gain	TTL Input	Active high doubles charge pump gain.
36	PLL Lock Mode Control Bit 0	TTL Input	
37	PLL Lock Mode Control Bit 1	TTL Input	
38	PLL Filter Current	Analog Current Output	Apply PLL filter referenced to Pin 41.
39	No Connection		May be left floating.
40	No Connection		May be left floating.
41	PLL Filter Reference Voltage	Analog Output Voltage	5 V reference voltage for the PLL filter, decoupling with 01 μF capacitor required.
42	Set VCO Center Frequency	Analog Current Input	Resistor/current programmable.
43	AGC Mode Control Bit 0	TTL Input	Defines read channel operating mode.
44	AGC Mode Control Bit 1	TTL Input	Defines read channel operating mode.
45	Window Strobe	Analog Input Voltage	±1 V range relative to analog +5 V.
46	Analog +12 V	Power Input	Decoupling with 0.1 μF‖0.01 μF required.
47	AGC Acquire Gain	Digital CMOS Input	Logic "1" = 800 μA, Logic "0" = 80 μA.
48	AGC Level Set Input	Analog Voltage Input	Sets the average signal to the S/H to the applied input voltage.
49	VGA Level Set Input	Analog Voltage Input	Sets the VGA gain (dB) =30 − (50 × V_{SET} level).
50	Sample-and-Hold Capacitor	Analog Current Output	
51	VGA Input Voltage (Pos)	Analog Voltage Input	
52	No Connections		May be left floating.

CHANNEL PROCESSING STAGES

The VGA Stage

The 30 dB variable gain stage input is biased at a potential of 5.0 V above analog ground. No additional dc bias is required, but ac coupling is necessary. The bias voltage is maintained during normal operation and during operation of the read after write recovery clamp.

The VGA differential output stage is an emitter follower with nominal dc biasing of 6.7 V. An internal 1.25 mA current source provides bias current to the output emitter followers. Output drive can be increased by an additional 1.25 mA by paralleling external resistors to the analog ground. However, caution should be exercised in order to avoid causing excess power dissipation for the package. The recommended output level for the VGA is 300 mV p–p differential into a 200 Ω differential load.

When the AD897 is used in the "VGA Set Gain" mode, AGC Mode Control Bit 0 = 1 (Pin 43) and Bit 1 = 0 (Pin 44), the VGA gain is programmable through the "VGA Level Set" pin (Pin 49). A 0 V potential applied to the "VGA Level Set" pin will produce a nominal VGA gain of 30 dB. Each 20 mV increment of voltage applied will produce a 1 dB reduction in VGA gain. Therefore, a simple equation can be used to calculate the nominal gain of the VGA in this mode:

$$VGA\ Gain\ (dB) = 30 - (50 \times V_{SET\ LEVEL})$$

If the "VGA Level Set" pin is not used, as may be the case when the AD897 is used in the AGC acquire and AGC hold modes only, it should be tied to analog ground.

The AD897 offers a read-after-write overdrive protection clamp. The "Input Clamp" mode, AGC Mode Control Bit 0 = 1 (Pin 43), Bit 1 = 1 (Pin 44), lowers the differential input impedance of the VGA from nominally 24 kΩ to 40 Ω. While the input clamp is active, the AGC loop is placed in the hold mode. In order for the clamp to operate correctly with an emitter driven input, a 50 Ω minimum resistor should be placed in series with the input coupling capacitors. The input resistors can be used in conjunction with a shunt capacitor to limit the input bandwidth. For example, a 100 Ω series resistor with a 10 pF shunt capacitor will limit the input bandwidth to 75 MHz. When the VGA input is being driven by an open collector driver with resistive termination, no additional series resistors are required.

The X16 Buffer

The inputs of this stage has on-chip dc biasing of 4.3 V (Internal Peak Detector Reference Voltage, Pin 3), therefore, no input bias current path needs to be provided. The inputs to the buffer should then be ac coupled. When not used, the inputs should be shorted together in order to avoid noise pickup and instability.

The nominal dc output level is 5.75 V with an internal 3.0 mA pull down current source. Output drive can be increased in a similar manner to that described for the VGA stage, by paralleling external resistors to analog ground. As before, precautions to limit excessive overall power dissipation apply when steps are taken to increase the output drive capability.

The Full Wave Rectifiers

The inputs to the full wave rectifiers are biased at an internal voltage of 5.75 V; therefore, only ac coupling is recommended. The full wave rectifier outputs consist of two nearly identical stages. Both employ emitter follower outputs. The nominal output voltage with zero input voltage is close to the peak detector's internal reference voltage of 4.3 V (Pin 3).

The rectified output voltage for the AGC loop is available through a 250 Ω resistor (Pin 12). The emitter follower output stage does not have a committed pull-down resistor. This enables the user to implement "peak-hold" AGC operation by applying the appropriate parallel RC combination between the "Rectified Signal for the AGC" (Pin 12) and ground.

The other full wave rectifier output – a rectified signal to derive the threshold for the data qualifier – is connected directly to its respective emitter follower output stage (Pin 15). This output also does not have a committed pull-down resistor, allowing for increased design flexibility.

When choosing the respective pull-down resistor values, caution should be exercised in order to avoid causing excess power dissipation for the package. In addition, to maintain well controlled rectifier offset voltages their quiescent currents must be matched.

The AGC Sample and Hold

When the AD897 is used in the "AGC Acquire" mode, AGC Mode Control Bit 0 = 0 (Pin 43) and Bit 1 = 0 (Pin 44), the AGC level is programmable through the AGC Level Set pin (Pin 48). A third control line, AGC Acquire Gain (Pin 47), sets the AGC charge current.

The AGC Level is defined as the AVERAGE of the full wave rectified output voltage to the sample-and-hold amplifier. A 200 mV dc potential applied to the AGC Level Set pin will produce a nominal AGC level of 100 mV. Each 10 mV increment/decrement of the applied "AGC Level Set" voltage will produce a 5 mV increase/decrease in the AGC level. Therefore, a simple equation can be used to calculate the nominal AGC level in this mode:

$$AGC\ Level = 0.5 \times V_{AGC\ LEVEL\ SET}$$

Without a peak hold capacitor at the full wave rectifier output for the AGC (Pin 12), accurate AGC operation only occurs with sinusoidal input signals. If your application requires the AGC operation to use a peak hold scheme, a "Peak-Hold" capacitor in series with a resistor maybe applied to the full wave rectifier output pin for the AGC (Pin 12). The addition of the RC alters the symmetry of the attack and decay rates of the rectifier, which is otherwise symmetric in operation. In order to ensure that the overall AGC response is the same for both high to low and low to high input level steps, it is necessary to make the rectifier attack and decay times at least a factor of two less than the AGC response time.

The AD897 offers two user programmable attack/decay times for the AGC loop. The AGC "slow" attack/decay times are achieved by setting the AGC Acquire Gain = "0" (Pin 47) and results in an 80 μA charge/discharge current on the Sample/Hold capacitor. Conversely, "fast" attack/decay times are achieved by setting the AGC acquire gain = "1" (Pin 47) and results in an 800 μA charge/discharge current. With the AD897 in the "fast" attack/decay mode and a 1000 pF sample-and-hold capacitor applied to Pin 50, a symmetrical 1 μs attack/decay time is achieved. A low leakage variety of hold capacitor, such as a silver mica, is necessary to ensure a low droop rate.

The AGC control potential is present at the "Sample-and-Hold Capacitor" pin (Pin 50). If control over open loop gain is desired, based on AGC control potentials measured during trial AGC operations, a FET input op amp should be used to buffer this node in order to avoid disturbing the hold operation.

DATA QUALIFIER STAGE

The AD897 data qualifier stage consists of three comparators, a pair of externally adjustable "resettable" delay lines, two Nand gates, two D-type flip-flops, and an externally adjustable one-shot (refer to the AD897 block diagram).

Figure 1 illustrates the operation of the AD897 data qualifier, using the recommended passive delay-line/differentiator described in the application section. Sequence "A" represents the pattern written on the disk, where a logic "1" is a change in magnetic state. Each change in magnetic state results in an output pulse. The analog input to the AD897 consists of a sequence of alternating pulses "B." The data pattern shown is for worst case RLL 1, 7 code input. The AD897 requires that the analog data input pass three criteria in order to qualify a signal and produce an output bit. The triple data qualification requirement significantly reduces errors by ensuring that noise will not be misinterpreted.

The first data qualification criteria is signal amplitude and is accomplished through the use of two amplitude threshold comparators. The outputs of each comparator drives a "resettable" delay line. The "resettable" delay line implements the second valid-data criteria, minimum time above valid-signal threshold before a zero-crossing can be detected. The minimum time above valid-signal threshold is set through an external resistor. The output of the "resettable" delay line is then used to determine if the data exhibits the correct polarity, the third data qualification criteria. To determine if the data exhibits the correct polarity a D-type flip-flop is used. The flip-flop is toggled with each valid data pulse, thereby, ensuring an alternate polarity qualification for each valid incoming data bit.

"C" represents the output waveform from the external differentiator, such that the points at which zero-crossings occur correspond to the peaks of the analog input "B." Sequence "D" shows the output from the zero-crossing comparator. Changes in the state of this output are used to clock an internal D-type flip-flop. The flip-flop is enabled using the output from the data polarity check, such that the flip-flop output changes state only when ALL three of the data qualification criteria, described earlier, have been satisfied. If ALL three data qualification criteria were met, and a zero-crossing event occurs, the flip-flop changes state, producing an output pulse "E." The duration of this pulse, seen at the Raw Data Output pin (Pin 28), is set using an external resistor. The one-shot also triggers the second D-type flip-flop, toggling the required valid-data polarity. The final output data sequence is shown in "F." As can be seen, despite inflections in the analog input, the data is correctly detected and the output is a reconstructed version of the write data.

Since the 1–7 code input is the most demanding of the popular encoding schemes to qualify, the AD897 easily handles such other codes as MFM and RLL 2, 7.

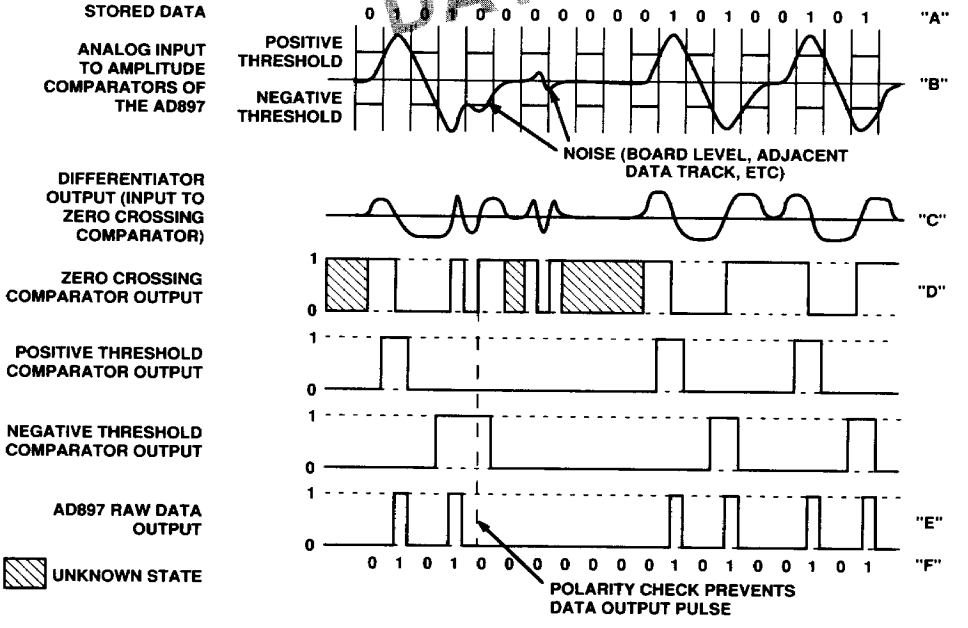


Figure 1. AD897 Operation for Worst Case 1–7 RLL Code

DATA SYNCHRONIZER STAGES

Phase Detector/Charge Pump

Figure 2 illustrates the operation of the phase/frequency detector and the charge pump in the lock to data mode. The data signal initiates a pump up – pump down – pump up cycle. The window center is marked by the falling edge of the clock present at the phase detector as shown. If the rising edge of the data pulse arrives at the window center then each charge pump cycle is exactly one half of the clock period long. Since the charge down current equals twice the charge up current charge balance is achieved at the end of the sequence. When the data pulse is early the first charge up cycle is stretched and the voltage on the filter increases. Conversely, if the data pulse is late the first pump-up cycle is shortened, thereby decreasing the voltage on the filter.

The above "Tri-Phase" phase detector avoids the shortcomings of the traditional "sliver" approach phase detector, by eliminating the dead band (zero phase detector gain) in the middle of the window. In addition, the "Tri-Phase" implementation does not require a half clock period long delay line, therefore window centering is improved and independent of the VCO frequency. To further improve window centering, the pump-up and pump-down currents are laser trimmed to ensure charge balancing.

The "Tri-Phase" phase detector was designed to allow the detection of data pulses arriving in adjacent windows, although that would be considered illegal with most encoding schemes. If such an event does occur, the synchronized data output would remain high for two consecutive clock periods.

In the frequency lock mode, the charge pump currents are equal in both directions. In this mode, the earlier of the data or clock pulse generates a charge-up or charge-down cycle. The charge cycle is terminated upon arrival of the later pulse, data or clock. Therefore, the lock to frequency mode does utilize the "sliver" approach and has the aforementioned drawbacks. However, in the frequency lock (lock to external clock or lock to preamble) mode the emphasis is on acquiring frequency matching between the reference source and the VCO.

In the tristate mode both the charge up and charge down current sources are disabled. This results in a frequency hold mode with respect to the VCO (coast).

The charge pump gain depends on the state of the PLL mode control lines (PLL Lock Mode Control Bit 0, PLL Lock Mode Control Bit 1) and the PLL Acquire Gain line (Pin 35). The following table gives a summary of the possible gain settings:

PLL Acquire Gain	Lock to Preamble	Charge Pump Gain
0	No	1/2 Nominal
0	Yes	Nominal
1	No	Nominal
1	Yes	2× Nominal

When considering the overall gain of the phase detector/charge pump block, it is important to remember that the gain is a function of the update rate of the detector:

$$Nominal\ Overall\ Gain = 200\ \mu A/(n2\pi)$$

where "n" = number of clock cycles per update

In lock to external clock and lock to preamble modes n is equal to 1.

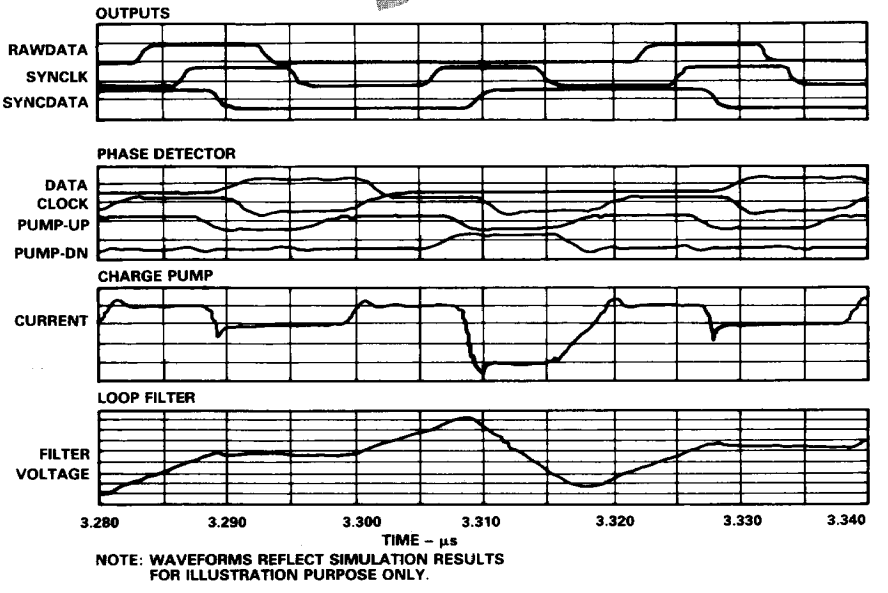


Figure 2. PLL Operation in Lock to Data Mode

Exponentiator/VCO

The exponentiator provides an exponential relationship between the control voltage appearing on the loop filter and the VCO frequency. Figure 3 graphically illustrates this exponential relation, with the control voltage on the X axis and the VCO frequency (normalized to ω_O) on the Y axis.

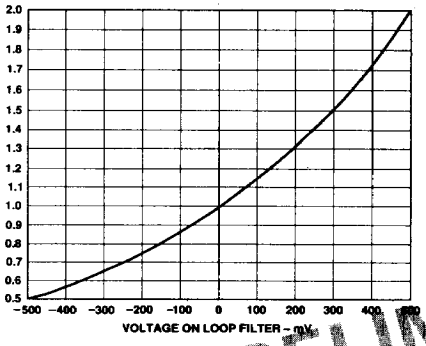


Figure 3. Exponentiator/VCO Transfer Curve Normalized to Center Frequency

The input stage of the exponentiator block uses PMOS transistors resulting in negligible charge leakage on the loop filter when the PLL is in tristate mode. This in turn enables the AD897 to achieve excellent frequency hold characteristics when the VCO is coasting.

The VCO center frequency is resistor or current programmable through the Set VCO Center Frequency pin (Pin 42). To help determine the appropriate resistor value, Figure 4 is provided.

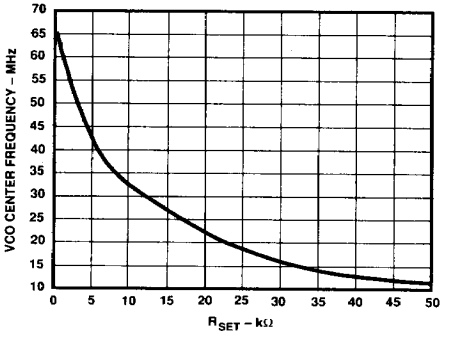


Figure 4. VCO Center Frequency vs. Resistor Value

The achievable VCO frequency range relative to center frequency is limited to 4:1. For example, if the user sets the center frequency to 30 MHz, the PLL will be abie to lock to a reference frequency anywhere from 15 MHz to 60 MHz, more than adequate for zone bit recording applications with their 2:1 range.

Dividers

The VCO clock is passed through a divider/multiplexer block prior to being applied to the phase/frequency detector. The division factor is programmed through the Division Factor Bit 0 (Pin 33) and the Division Factor Bit 1 (Pin 34) control pins.

Division Factor Bit 0	Division Factor Bit 1	Division Factor
0	0	1
0	1	2
1	0	3
1	1	4

Under normal conditions these control lines are expected to change together with PLL mode control lines and the PLL acquire line.

In the lock to external clock and lock to preamble modes the user has the option to determine the VCO/external clock or VCO/preamble frequency ratio. In both cases the VCO frequency is divided down by the programmed division factor. Also, in the lock to external clock, the reference frequency is divided by a factor of two. In the lock to data and tristate modes, the VCO clock is passed directly to the phase detector input.

Having a programmable divider in the feedback path and a fixed division of the reference clock path coupled with the 4:1 VCO frequency range provides considerable flexibility in choosing the reference crystal or preamble frequency for any encoding schemes.

9

GENERAL LAYOUT REQUIREMENTS

The AGC section of the AD897 has almost 60 dB of total gain available at 60 MHz. Good RF layout must be used in the circuit board to avoid oscillations in the 150 MHz to 350 MHz region. A single pole RC filter applied at the input of each stage, with a cutoff in the region of 75 MHz to 125 MHz, will help avoid oscillation problems. As a general rule, keep the connections to interstage components as short as possible; it is also recommended that any low-pass filtering that may be required by the system be performed between the VGA stage and the X16 buffer amplifier. A ground plane should be used to surround any interstage components wherever possible. If these simple rules are followed, stable operation should be assured.

A parallel combination of 0.1 μF and 0.01 μF ceramic capacitors should be used as close to the supply pins as possible; this includes the Analog +12 V (Pin 46), Analog +5 V (Pin 21) and Digital +5 V (Pin 31) supplies. It is also recommended that the PLL Filter Reference Voltage (Pin 41) is decoupled with a 0.1μF ceramic capacitor.

Extensive use of a ground plane is recommended. An analog ground (Pin 20) is supplied for the AGC section, while two digital grounds are supplied: one for the Data Qualifier/PLL section (Pin 24), and one for the output buffers (Pin 25). The digital ground should be connected to the analog ground as near to the power supply common as possible to minimize noise injection to the analog ground.

The filter and output pulse setting resistors should be tied, as directly possible, to the +5 V analog supply.

PPL OPERATING MODES

Lock to External Clock – PLL Lock Mode Control Bit 0 = 0, Bit 1 = 0. Lock to both frequency and phase of the reference clock is divided down internally by 2. In the feedback path the VCO output is divided down by the programmed division factor: 1, 2, 3, or 4. This enables the user to achieve a range of VCO vs. external clock frequency ratios namely 1:2, 1:1, 3:2, 2:1. The clock signal on the External Clock Input (Pin 32) is multiplexed to the Synchronized Clock Output (Pin 30). Upon entering or exiting this mode a glitch-free transition between the VCO and the external clock is provided.

Lock to Preamble – PLL Mode Control Bit 0 = 0, Bit 1 = 1. In this mode, the raw input data stream provides the phase information. A constant frequency input which equals the VCO frequency divided by the programmed division factor is required. The loop is operated in the frequency lock mode. The charge pump gain is doubled or quadrupled if the PLL Acquire Gain pin (Pin 35) is high at the same time.

Lock to Data – PLL Mode Control Bit 0 = 1, Bit 1 = 1. Phase lock only to the Raw Data Output (Pin 28) of the read channel. When entering this mode zero phase start-up is automatically initiated after four data pulse updates have been received following the command. The charge pump is tristated during the delay period, ensuring a minimal glitch during synchronization. The loop time constant is defined by an external RC filter network. This is the only mode when the Synchronized Data Output (Pin 29) is enabled.

Tristate – PLL Mode Control 0 = 1, Bit 1 = 0. This mode allows the user to hold the loop filter voltage so that the VCO frequency remains constant without having to switch to lock to external clock.

Switching Between PPL Operating Modes

Figure 5 illustrates a typical sequence of PLL operating modes. The control signals should be derived from an external register. When changing between operating modes care should be taken to avoid shorter pulses than required to complete the transition from one operating mode to another. In most cases the charge pump is tristated and the VCO is disabled for a period of four data pulses applied to the phase detector (see Figure 6); this translates into a delay of 4 data or 8 external clock pulses. This features prevents the charge pump from generating any glitches thus preserving the integrity of the loop voltage.

Upon the appropriate delay, the subsequent pulse restarts the VCO. When switching to lock to data mode the VCO is synchronized with the 5th data pulse, resulting in a zero phase start-up error. The combination of the above described frequency hold and zero phase start-up error eliminates any disturbance of the loop during the transition from one operating mode to another. To further minimize the lock in time, the user has the option of momentarily doubling the charge pump gain through the "PLL Acquire Gain" control line.

When switching from/to lock to external clock, the transition involves changing the clock source present on the Synchronized Clock Output pin (Pin 30). The signal present at this pin changes from the external clock (Pin 32) to the VCO, or vice versa. Extra care has been taken to provide glitch-free multiplexing of these clock sources and to minimize the time while the clock is inactive.

The following table summarizes the possible operating mode transitions and their effects on the different circuit blocks.

Previous Mode	Present Mode	Charge Pump	VCO	Synchronized Clock
Lock to Ext. Clock	Lock to Preamble	Gain = 2×	No Effect	Switch to VCO Clock
	Lock to Data	Tristate for 4 Updates	Zero Phase Start-Up	Switch to VCO Clock
	Tristate	High Impedance	Coast	Switch to VCO Clock
Lock to Preamble	Lock to Data	Tristate for 4 Updates	Zero Phase Start-Up	Inactive for 4 Updates
	Tristate	High Impedance	Coast	Inactive for 4 Updates
	Lock to Ext. Clock	Tristate for 8T Ext. Clock	Disabled for 8T Ext. Clock	Switch to Ext. Clock
Lock to Data	Tristate	High Impedance	Coast	VCO Clock
	Lock to Ext. Clock	Tristate for 8T Ext. Clock	Disabled for 8T Ext. Clock	Switch to Ext. Clock
	Lock to Preamble	Gain = 2×	No Effect	VCO Clock
Tristate	Lock to Ext. Clock	Tristate for 8T Ext. Clock	Disabled for 8T Ext. Clock	Switch to Ext. Clock
	Lock to Preamble	Tristate for 4 Updates	Disabled for 4 Updates	Inactive for 4 Updates
	Lock to Data	Tristate for 4 Updates	Zero-Phase Start-Up	Inactive for 4 Updates

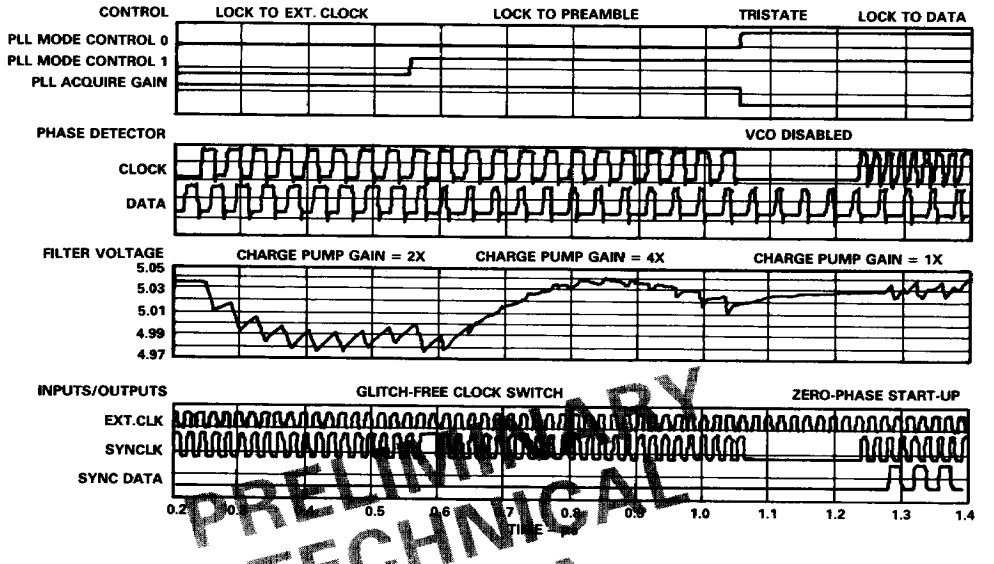


Figure 5. PLL Operating Mode Sequencing

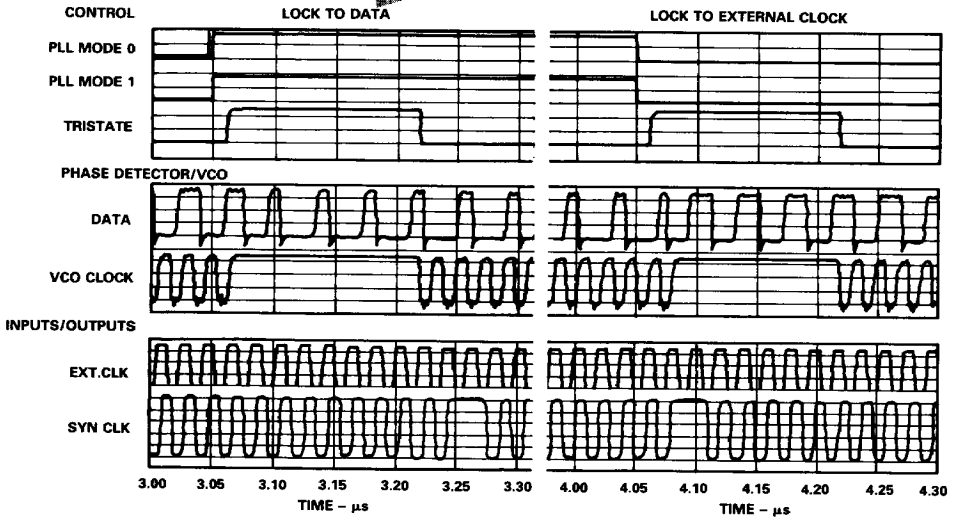
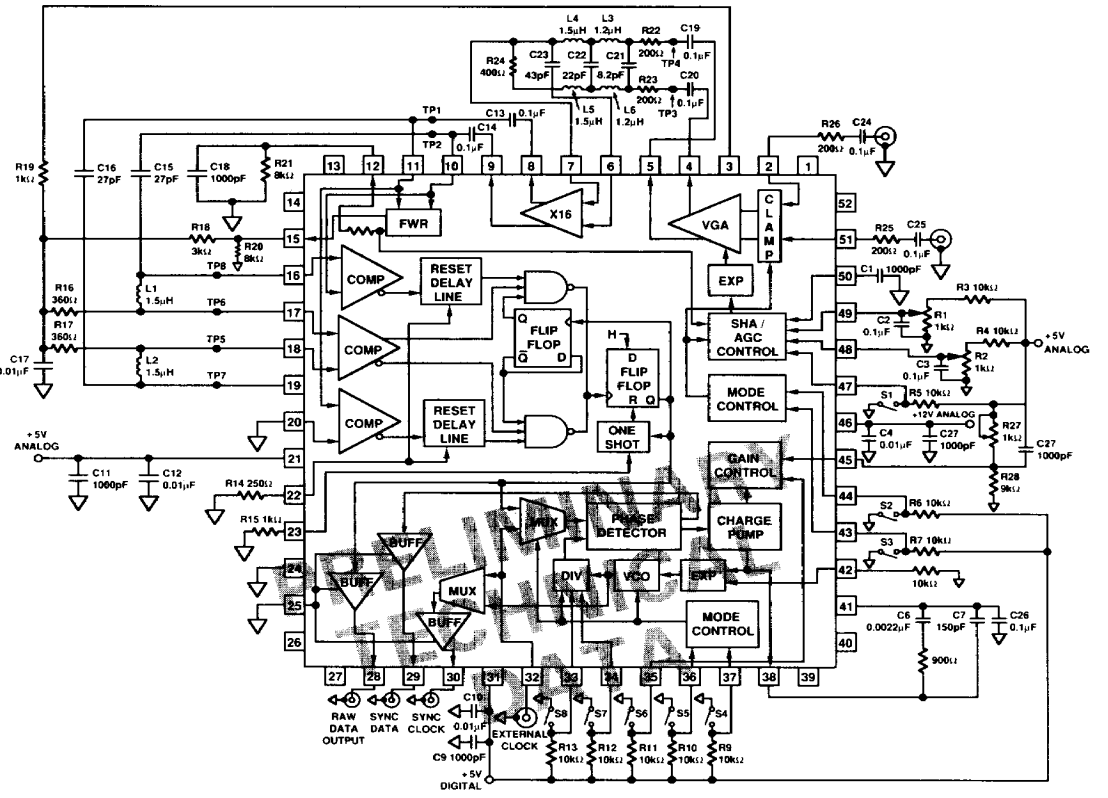


Figure 6. Transition Between Operation Modes. Lock to External Clock—Lock to Data—Lock to External Clock



FUNCTIONALITY OF SWITCHES

Switch	Description
1	AGC Acquire Gain
2	AGC Mode Control Bit 1
3	AGC Mode Control Bit 0
4	PLL Lock Mode Control Bit 1
5	PLL Lock Mode Control Bit 0
6	PLL Acquire Gain
7	Division Factor Control Bit 1
8	Division Factor Control Bit 0

DEFINITION OF TEST POINTS

Test Point	Definition
1	Negative input to the full wave rectifier, also serves as input to the passive differentiator and the negative comparator input.
2	Positive input to the full wave rectifier, also serves as input to the passive differentiator and the positive comparator input.
3	Negative AC coupled output of the VGA.
4	Positive AC coupled output of the VGA.
5	Negative input to the zero-crossing comparator.
6	Positive input to the zero-crossing comparator.
7	Negative threshold comparator input.
8	Positive threshold comparator input.