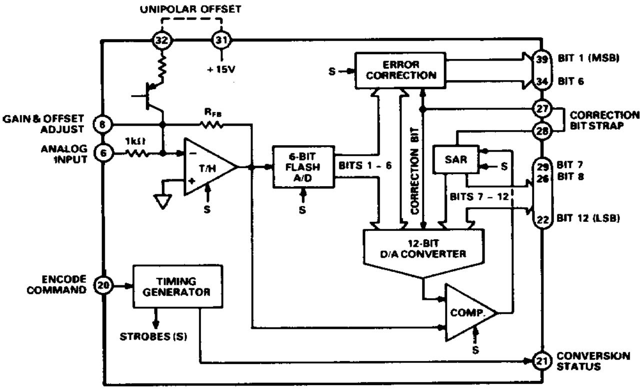
12-Bit, 1 MSPS A/D Converter

AD9003

FEATURES
12-Bit Resolution
1 MSPS Word Rates
T/H and Timing Included
Single 40-Pin DIP

APPLICATIONS
Radar Systems
Digital Oscilloscopes
Test Systems
Analytical Instrumentation
Waveform Analyzers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9003 is a complete 12-bit, 1 MSPS analog-to-digital converter (ADC) which combines low cost and high performance in a single 40-pin DIP. This unique converter includes track-and-hold (T/H), timing, and encoding functions with a power dissipation of only 2.2 watts.

This remarkable unit is capable of converting analog signals to the Nyquist limit at word rates through 1 MSPS. Its 1µs conversion interval includes acquisition time for the internal T/H, making it a true 1 MSPS converter.

Proprietary conversion techniques achieve linearity equivalent to the best successive approximation ADC along with subranging conversion speeds. A conversion status signal simplifies transferring output data into system logic. Innovative thick- and thin-film technologies assure excellent performance over temperature without compromising ac characteristics.

The AD9003KM operates at case temperatures from 0 to +70°C; the SM and TM units operate from −25°C to +100°C.

 (typical with nominal supplies, unless otherwise noted.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- $\pm V_S$ . . . . ±18V
- V_{CC} . . . . −0.5V to +7V

Analog Input . . . . ±15V
Digital Inputs . . . . −0.5 to V_{CC}
Maximum Junction Temperature
- Models AD9003SM/TM . . . . 165°C
- Model AD9003KM . . . . 150°C

Operating Temperature Range (Case)
- AD9003KM . . . . 0 to +70°C
- AD9003SM/TM . . . . −25°C to +100°C

Storage Temperature . . . . −65°C to +150°C
Lead Soldering Temperature (10 sec) . . . . +300°C

Parameter[1, 2] (Conditions)	Temp	AD9003KM[1] Min	AD9003KM[1] Typ	AD9003KM[1] Max	AD9003SM[2] Min	AD9003SM[2] Typ	AD9003SM[2] Max	AD9003TM[2] Min	AD9003TM[2] Typ	AD9003TM[2] Max	Units
RESOLUTION			12			12			12		Bits
			0.024			0.024			0.024		%FS
LSB Weight			1.22			1.22			1.22		mV
STATIC ACCURACY											
√ Gain Error	+25°C		±0.1	±0.2		±0.1	±0.2		±0.1	±0.2	%FS
# Gain Error	Full			±0.46			±0.6			±0.6	%FS
√ Bipolar Offset	+25°C		±5	±10		±5	±10		±5	±10	mV
# Bipolar Offset	Full			±23			±32			±32	mV
√ Unipolar Offset	+25°C		±5	±10		±5	±10		±5	±10	mV
# Unipolar Offset	Full			±23			±32			±32	mV
√ Differential Linearity	+25°C		±0.5	±1.0		±0.5	±1.0		±0.5	±1.0	LSB
√ Differential Linearity	Full			−1.0/+2.0			−1.0/+2.0			±1.0	LSB
√ Integral Linearity (Best Fit)	+25°C		±0.8	±1.5		±0.8	±1.5		±0.8	±1.5	LSB
√ Integral Linearity (Best Fit)	Full			±1.5			±2.0			±2.0	LSB
√ Resolution for Which There are No Missing Codes	Full		12			12			12		Bits
DYNAMIC CHARACTERISTICS (Conversion Rate = 1MHz)[3]											
In-Band Harmonics[4]											
√ dc to 100kHz	+25°C	74	80		74	80		74	80		dB
√ dc to 100kHz	Full	72			72			72			dB
# 100kHz to 500kHz	+25°C		75			75			75		dB
√ Conversion Time[5]	+25°C		820	850		820	850		820	850	ns
# Effective Aperture Delay Time	+25°C	6	16	27	6	16	27	6	16	27	ns
# Aperture Uncertainty (Jitter)	+25°C		26			26			26		ps, rms
√ Signal-to-Noise Ratio[6]	+25°C	65	69		65	69		65	69		dB
√ Signal-to-Noise Ratio[6]	Full	65			65			65			dB
# Transient Response[7]	+25°C		200			200			200		ns
# Overvoltage Recovery Time[8]	+25°C			1500			1500			1500	ns
# Two-Tone Intermodulation[9]	+25°C		87			87			87		dB
ANALOG INPUT											
# Voltage Range (Full Scale)[10]	Full		5			5			5		V, p-p
# Input Impedance	+25°C	950	1000	1050	950	1000	1050	950	1000	1050	Ω
# Input Impedance	Full	950	1000	1050	950	1000	1050	950	1000	1050	Ω
Input Bandwidth											
# Small Signal, −3dB[11]	+25°C		10			10			10		MHz
# Large Signal, −3dB[12]	+25°C		8			8			8		MHz
TEMPERATURE DRIFT											
Offset Temperature Coefficient											
√ Bipolar	Full		±10	±35		±10	±40		±10	±40	ppm/°C
√ Unipolar	Full		±10	±35		±10	±40		±10	±40	ppm/°C
√ Gain Temperature Coefficient	Full		±15	±40		±15	±40		±15	±40	ppm/°C
# Differential Linearity Tempco	Full		±1.5	±3.5		±1.5	±3.5		±1.5	±3.5	ppm/°C
DIGITAL INPUTS											
# Logic Compatibility	Full		TTL			TTL			TTL		
# Logic "1" Voltage	Full	+2.0		V_{CC}	+2.0		V_{CC}	+2.0		V_{CC}	V
# Logic "0" Voltage	Full	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	V
Encode Command[13]											
Input Current											
# Logic "1"	Full			60			60			60	μA
# Logic "0"	Full			−1.2			−1.2			−1.2	mA
# Width[14]	Full	200		750	200		750	200		750	ns
# Rate	Full	dc		1.0	dc		1.0	dc		1.0	MSPS
# Rise/Fall Times	Full			10			10			10	ns

Parameter[1, 2] (Conditions)	Temp	AD9003KM[1] Min	AD9003KM[1] Typ	AD9003KM[1] Max	AD9003SM[2] Min	AD9003SM[2] Typ	AD9003SM[2] Max	AD9003TM[2] Min	AD9003TM[2] Typ	AD9003TM[2] Max	Units
DIGITAL OUTPUTS											
# Logic Compatibility	Full		TTL			TTL			TTL		
# Logic "1" Voltage	Full	+2.4			+2.4			+2.4			V
# Logic "0" Voltage	Full			+0.4			+0.4			+0.4	V
# Output Drive	Full		1 Standard			1 Standard			1 Standard		TTL Load
Format			Parallel			Parallel			Parallel		
Coding											
Unipolar Mode			Complementary Binary			Complementary Binary			Complementary Binary		
Bipolar Mode			Complementary Offset Binary			Complementary Offset Binary			Complementary Offset Binary		
POWER REQUIREMENTS											
$+V_S$ Voltage	Full	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	V
√ $+V_S$ Current	Full		78	90		78	90		78	90	mA
$-V_S$ Voltage	Full	−14.5	−15.0	−15.5	−14.5	−15.0	−15.5	−14.5	−15.0	−15.5	V
√ $-V_S$ Current	Full		44	49		44	49		44	49	mA
V_{CC} Voltage	Full	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	V
√ V_{CC} Current	Full		75	200		75	200		75	200	mA
√ Power Dissipation	Full		2.2	3.2		2.2	3.2		2.2	3.2	W
# PSRR[15]	+25°C		45			45			45		dB
THERMAL RESISTANCE											
Junction to Air, θ_{CA}[16]			19			19			19		°C/W
Junction to Case, θ_{JC}			3			3			3		°C/W
MTBF[17]											
Mean Time Between Failures					7.84×10^4			7.84×10^4			Hours
PACKAGE OPTION[18]											
M-40			AD9003KM			AD9003SM			AD9003TM		

NOTES

√ 100% tested (See Notes 1 and 2). #Specification guaranteed by design; not tested.

[1]AD9003KM parameters preceded by a check (√) are tested at +25°C ambient temperature; performance is guaranteed over the commercial temperature range (0 to +70°C case temperature).

[2]AD9003SM and TM parameters preceded by a check (√) are tested at −25°C case, +25°C ambient, and +100°C case temperatures.

[3]Converting in excess of 1.0MHz is possible; however, acquisition time is reduced, which may increase distortion of high-frequency analog signals.

[4]In-band harmonics are expressed in dB below FS in terms of spurious in-band signals generated at 1MHz encode rate and single tone analog input in range shown.

[5]Measured from leading edge of encode command to trailing (rising) edge of conversion status signal (see Timing Diagram).

[6]RMS signal to rms noise ratio; analog input 1dB below FS @ 100kHz; 1MHz encode rate.

[7]For full-scale step input, 12-bit accuracy attained in specified time.

[8]Recovers to 12-bit accuracy in specified time after 2×FS input overvoltage. (See text and Figure 5 for information on overloads.)

[9]Intermodulation measured in dB below FS at 1MHz encode rate with input frequencies of 75kHz and 105kHz; each 7dB below FS.

[10]Voltage Range = ±2.5V or 0V to −5.0V.

[11]With analog input 40dB below FS.

[12]With FS analog input. (Large-signal BW flat within 0.5dB, dc to 500kHz.)

[13]Transition from "0" to "1" initiates conversion.

[14]For 1MHz encode rate. At conversions below 1MHz, max width is conversion period minus 250ns. Optimum linearity at 200 to 250ns widths.

[15]Power Supply Rejection Ratio (PSRR) is sensitivity of offset to V_{CC}. This is parameter which is most sensitive to variations in supply voltage.

[16]The relationship between the device package and outside environment (θ_{ca}) varies with the application. Value shown is based on measuring case temperature with supply voltages applied to a device installed in a ZIF socket mounted on a standard "EJ" burn-in board.

[17]Calculated for SM/TM versions using MIL-HNBK-217; Ground Fixed; +80°C case temperature.

[18]M = Metal Can DIP. For outline information see Package Information section.

ORDERING INFORMATION

For operating case temperatures from 0 to +70°C, order part number AD9003KM. Two models are available for operation at case temperatures betweeen −25°C and +100°C. With the exception of differential linearity, the electrical specifications on these devices are the same. The AD9003SM guarantees no missing codes over temperature; the AD9003TM is screened for differential nonlinearity of ±1LSB maximum.

Both the commercial temperature and extended temperature versions are packaged in 40-pin metal can DIPs.

PIN DESIGNATIONS
(As viewed from bottom)

PIN	FUNCTION	PIN	FUNCTION
40	DIGITAL GROUND	1	+5V
39	BIT 1	2	REFERENCE BYPASS[1]
38	BIT 2	3	DIGITAL GROUND
37	BIT 3	4	DIGITAL GROUND
36	BIT 4	5	−15V
35	BIT 5	6	ANALOG INPUT
34	BIT 6	7	DO NOT CONNECT
33	+5V	8	GAIN & OFFSET ADJUST
32	UNIPOLAR OFFSET[2]	9	ANALOG GROUND
31	UNIPOLAR OFFSET[1,2]	10	ANALOG GROUND
30	+15V	11	ANALOG GROUND
29	BIT 7	12	ANALOG GROUND
28	CORRECTION BIT[3]	13	ANALOG GROUND
27	CORRECTION BIT[3]	14	ANALOG GROUND
26	BIT 8	15	ANALOG GROUND
25	BIT 9	16	ANALOG GROUND
24	BIT 10	17	+5V
23	BIT 11	18	DIGITAL GROUND
22	BIT 12	19	−15V
21	CONVERSION STATUS	20	ENCODE COMMAND

NOTES
Although Grounds are Designated as Analog or Digital, All Grounds Should Be Connected to a Single Common Low-Impedance Ground Plane for Best Results.
[1]**Pins 2 and 31 Must Be Bypassed to Ground with 0.1µF for Optimum Performance.**
[2]**For Unipolar Operation, Connect Pins 31 and 32; for Bipolar Operation, Ground Pin 32 and Connect Pin 31 Only to 0.1µF.**
[3]**Pins 27 and 28 Must Always Be Strapped Together with No Other Connections.**

THEORY OF OPERATION

Refer to the block diagram of the AD9003.

Basically, the design of the unit is based on successive approximation techniques. However, the AD9003 also uses parallel encoding for the most significant bits (MSBs).

When a TTL-compatible Encode Command signal is applied to Pin 20, it causes the internal Timing Generator to generate strobe pulses used for controlling the timing of the various actions within the device.

The encode command causes the track-and-hold (T/H) to switch from a "track" mode to a "hold" mode; switches the 6-bit flash converter to a tracking mode of operation to allow it to reach the held value from the T/H; and resets the SAR. When the flash converter output has been determined, Bits 1 – 6 become inputs to the 12-bit D/A converter.

If the D/A voltage applied to the comparator is greater than the "held" value being applied to the comparator, a correction bit is turned on. If the D/A voltage is less, there is no correction bit and no change in the signal.

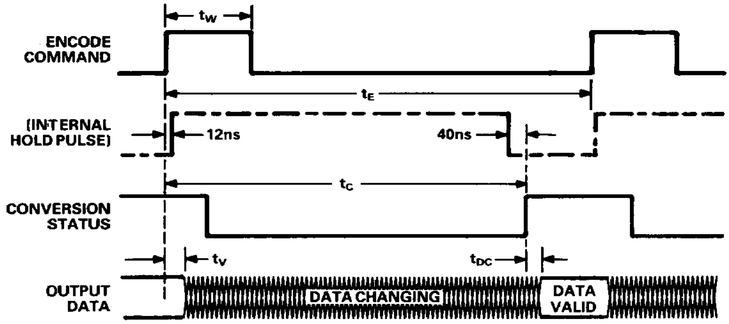
At this point, the D/A output voltage and the correction circuit outputs are 12-bit accurate. Standard successive approximation techniques are used to determine Bits 7 – 12; the end result is a 12-bit parallel output from the AD9003 A/D Converter.

The overall linearity of the AD9003 is independent of the flash converter, which materially enhances the performance of the unit. In addition, the architecture used in the converter makes it less sensitive to nonlinearities caused by D/A and/or comparator settling.

Performance of the AD9003 is equivalent to that of an ultrahigh-speed SAR type of design. But the design techniques which are used relieve the stringent comparator/DAC settling requirements usually associated with SAR designs. Instead, the AD9003 reaps the benefits of combining the best characteristics of flash converters and SARs while avoiding the penalties which are inherent in each individually.

Refer to Figure 1, the timing diagram for the AD9003. In this illustration, spacing between encode commands is shown as it would be for a 1MHz word rate, i.e., 1000ns. The width of the encode pulse is at its minimum value of 200ns.

The period of data validity associated with each encode command appears, in the figure, to be relatively short. Remember, however, each encode command generates the necessary switching to perform the digitizing function, and causes the output data to begin changing.



		MIN	MAX
t_W	ENCODE COMMAND PULSE WIDTH	200ns	750ns
t_E	SPACING BETWEEN ENCODE COMMANDS	1000ns	
t_C	CONVERSION TIME		850ns
t_V	DATA VALID		50ns
t_{DC}	DATA CHANGING		35ns

Figure 1. AD9003 Timing Diagram

In Figure 1, the timing is based on a maximum encode rate, with minimum spacing between encode commands. At lower conversion rates, this spacing would be lengthened correspondingly and the interval when data are valid would become longer.

Internal timing within the AD9003 typically requires 770ns to accomplish the necessary switching and processing of the analog input "frozen" by the encode command. Since the AD9003 is a true 1MHz converter, this leaves 230ns for the T/H to re-establish full accuracy when it returns to the "track" mode at the completion of the digitizing period.

This addition of the required 770ns and the 230ns accuracy increment shows up as a total of 1,000ns minimum between encode commands in Figure 1; any shorter interval will detract from the overall performance of the unit. Higher encode rates, i.e., shorter intervals between encode commands, are possible; but they may cause distortion on high-frequency analog signals because the T/H will not be fully settled when it is switched to the "hold" mode.

SETTING GAIN AND OFFSET

Varying gain and offset for the AD9003 enhances performance of the unit and increases its flexibility in applications. One suggested method of obtaining approximately 5% variation in each is shown in Figure 2.

The AD9003 can be operated in a unipolar mode or a bipolar mode; strap options and adjustments of the external controls shown in Figure 2 determine which is used. When calibrating for either mode, apply an encode command at the word rate frequency of the system to Pin 20.

Connect a precision voltage source between the ANALOG INPUT connection shown in Figure 2 and ground. Set its output for the voltage shown in Table I as being equal to $-FS + 1/2LSB$ for the input range to be used ($-0.6mV$ for unipolar operation and $+2.4994V$ for bipolar operation if using the full-scale 5V input range of the AD9003).

Adjust the OFFSET control for a digital output which "dithers" between 0000 0000 0000 and 0000 0000 0001.

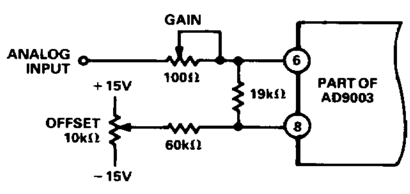


Figure 2. AD9003 Gain and Offset

To set gain, readjust the output of the voltage reference source to the value shown in Table I as being equal to +FS −1-1/2LSB for the input range to be used (−4.9982V for unipolar operation; −2.4982V for bipolar operation with the full-scale 5V range).

Adjust the GAIN control for a digital output which "dithers" between 1111 1111 1110 and 1111 1111 1111.

Figures 3 and 4 provide additional information about the switching points of the LSB when adjusting for either unipolar or bipolar operation using the full-scale 5V input.

AD9003 DRIVER CIRCUIT WITH CLAMP

The choice of the driver amplifier for an A/D can have significant effect on the performance of the converter. The ADI AD9610 Op Amp is the recommended choice for operation with the AD9003. This amplifier has extremely fast settling time and low distortion; these are especially important as the selected word rate frequency approaches the Nyquist limit.

In some applications, the analog input signals to be digitized may be outside the 5V range of the AD9003 converter, which can detract from the performance of the device by driving it into saturation.

At input frequencies greater than 50kHz, overloads larger than approximately 25% will saturate the front-end circuits of the internal track-and-hold. When the overload is removed, the T/H may cause erroneous codes to be generated at the output. Figure 5 shows a suggested circuit to avoid this.

Table I.

For UNIPOLAR Input	Apply Reference	And Adjust	For "Dither" Between	For BIPOLAR Input	Apply Reference	And Adjust	For "Dither" Between
0 to −5V	−0.6mV	OFFSET	0000 0000 0000 and 0000 0000 0001	0.00	0.00	OFFSET	0111 1111 1111 and 1000 0000 0000
0 to −5V	−4.9982V	GAIN	1111 1111 1110 and 1111 1111 1111	±2.5V	−2.4982V	GAIN	1111 1111 1110 and 1111 1111 1111

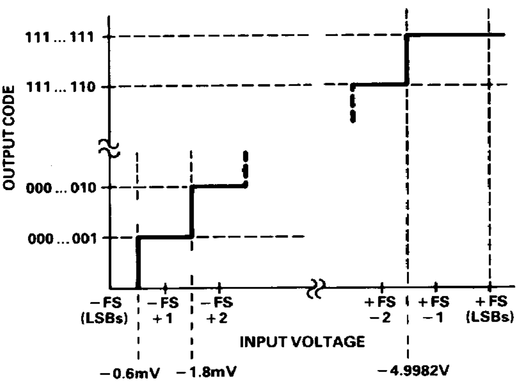


Figure 3. AD9003 Unipolar Adjustment

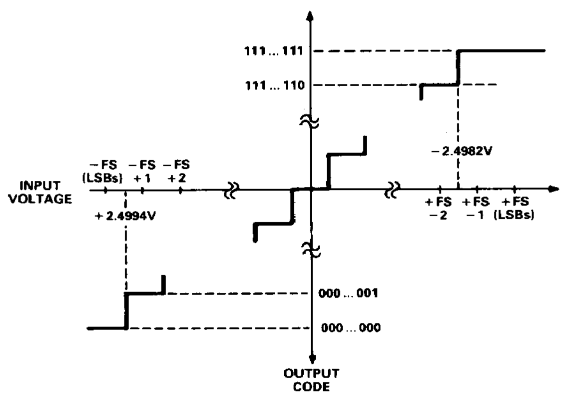


Figure 4. AD9003 Bipolar Adjustment

In this diagram, the value of the feed forward resistor R_{FF} is calculated on the basis of the equation:

$$R_{FF} = |\text{Desired Full-Scale Bipolar Voltage}| \times 500$$

The circuit eliminates saturating the internal T/H of the AD9003. Using an Analog Devices AD9610 ahead of the converter allows ±3x overdrives before the amplifier goes into saturation. Even in those instances in which the input signal exceeds the ±3x limit, the AD9610 comes out of saturation much more quickly than the input circuits of the converter would under the same circumstances.

Bipolar inputs to the AD9003 are held to a maximum of ±2.5V by the clamp circuits made up of 1N2810 Schottky diodes. The Analog Devices AD744 amplifiers and their associated circuits are for the purpose of clamping the Schottky diodes at the desired maximum input levels. As shown, +CLAMP ADJUST and −CLAMP ADJUST are set for +2.530V and −2.530V respectively.

These adjustment values take into account the gain and offset tolerances of the AD9003. If resistors with low temperature coefficients are selected, the clamp circuit will operate over the entire temperature range of the converter.

The bipolar circuit in Figure 5 can also be used for unipolar operation of the A/D with only minor changes. For this mode, the upper op amp (AD744 #1) and its associated reference circuits are removed; the upper 1N2810 clamp is connected, instead, to ground.

With these changes, the unipolar full-scale overdrive limit is 1.5x rather than the 3x of the bipolar connections; but this will prevent saturating the front end circuits of the AD9003. The value of R_{FF} in the unipolar circuit is based on:

$$R_{FF} = |\text{Desired Full-Scale Unipolar Voltage}| \times 250$$

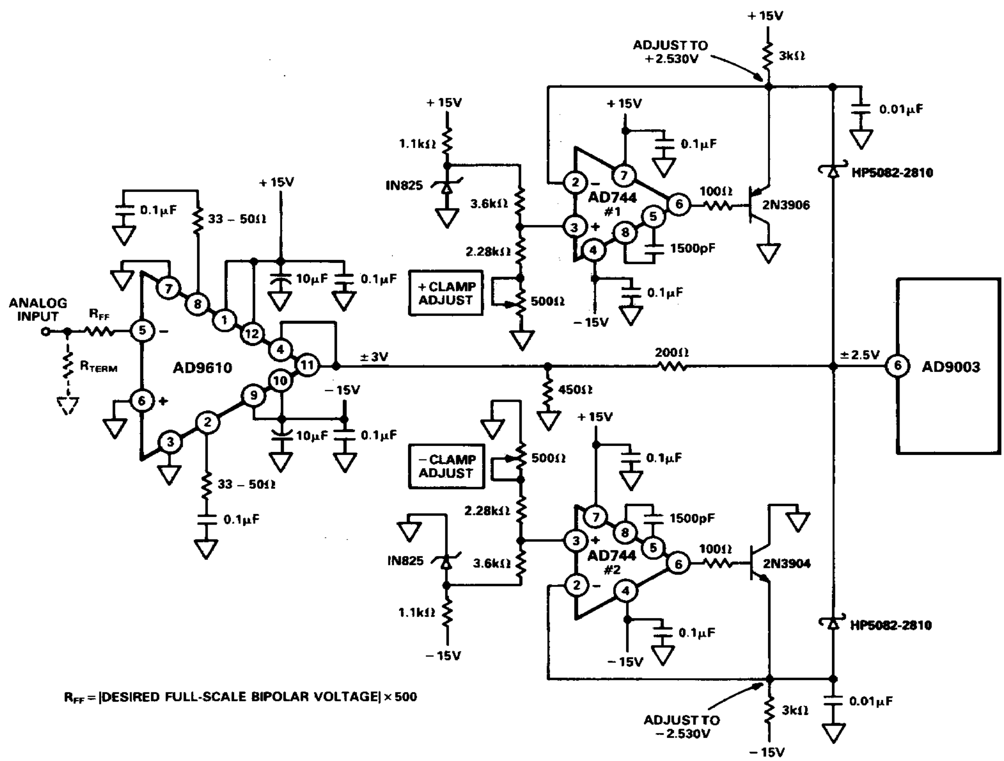


Figure 5. AD9003 Driver Circuit with Clamp

SUGGESTED LAYOUT

To obtain optimum performance from systems using the AD9003 or any other high-speed component, the user must exercise care in laying out the circuit. It is critical to use the shortest possible lead lengths and circuit runs. Construct the circuit on a large, low-impedance ground plane containing the maximum possible amount of copper dedicated as ground surface.

The AD9003 also requires the use of bypass capacitors on the power supplies; these should be connected as closely as possible to the supply pins. A suggested layout for the AD9003 when it is mounted on a printed circuit board is shown in Figure 6.

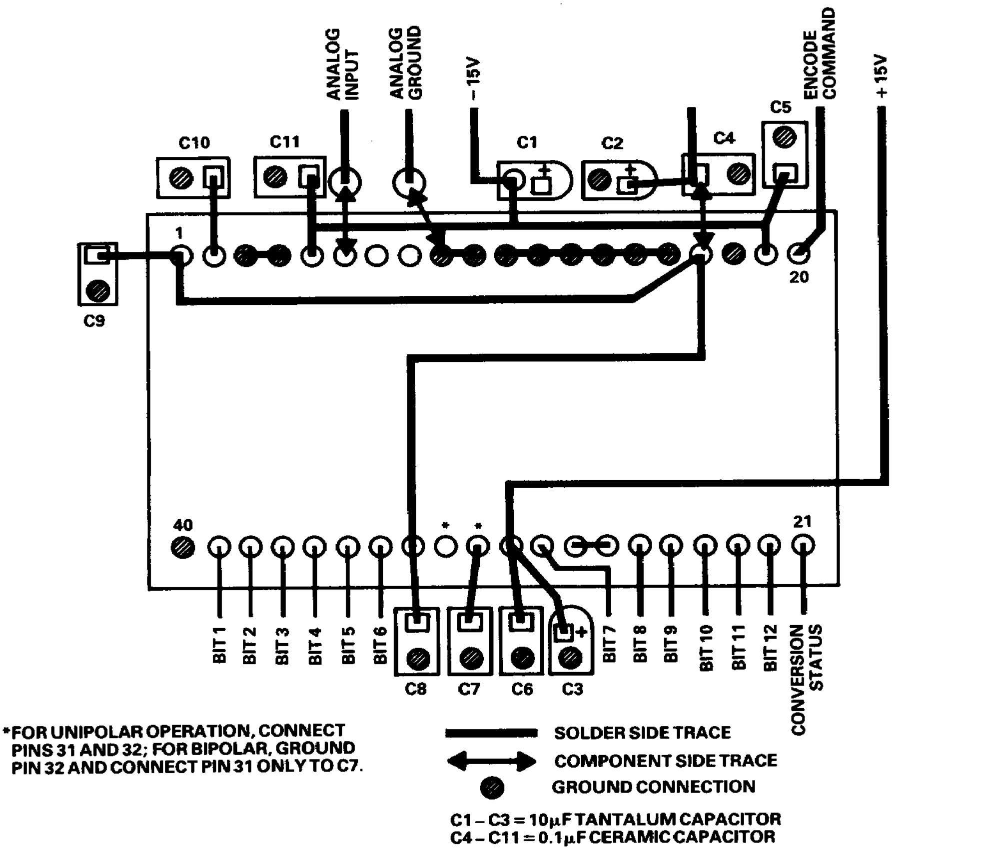


Figure 6. AD9003 Suggested Layout (As Viewed from Bottom – Not to Scale)