



ANALOG DEVICES INC

8-Bit, 35 MSPS Video A/D Converter

AD9048**1.1 Scope.**

This specification covers the requirements for an 8-bit, 35 Msp/s analog-to-digital converter (ADC). Refer to the commercial data sheet for applications information.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD9048S(X)/883B
-2	AD9048T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
E	E-28A	28-Contact LCC
Q	Q-28	28-Pin Ceramic DIP

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to DGND	-0.5 V to +7.0 V
AGND to DGND	-0.5 V to +7.0 V
V_{EE} to AGND	+0.5 V to -7.0 V
V_{IN} , V_{RT} or V_{RB} to AGND	+0.5 V to V_{EE}
V_{RT} to V_{RB}	-2.2 V to +2.2 V
CONV, NMINV or NLINV to DGND	-0.5 V to +5.5 V
Applied Output Voltage to DGND ¹	-0.5 V to +5.5 V
Applied Output Current, Externally Forced ^{2, 3}	-1.0 mA to +6.0 mA
Output Short Circuit Duration ⁴	1.0 sec
Operating Temperature Range (Case)	-55°C to +125°C
Junction Temperature	+175°C
Storage Temperature Range (Case)	-65°C to +150°C
Lead Soldering Temperature (10 sec)	+300°C

NOTES

¹Applied voltage must be current limited to specific range.

²Forcing voltage must be limited to specified range.

³Current is specified as negative when flowing into the device.

⁴Output HIGH; one pin to ground; one second duration.

1.5 Thermal Characteristics.

Maximum junction temperature should not be allowed to exceed +175°C. Typical thermal impedances:

28-Contact LCC: $\theta_{JA} = 69^\circ\text{C/W}$; $\theta_{JC} = 21^\circ\text{C/W}$;

28-pin Ceramic DIP: $\theta_{JA} = 49^\circ\text{C/W}$; $\theta_{JC} = 15^\circ\text{C/W}$.

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Table 1.

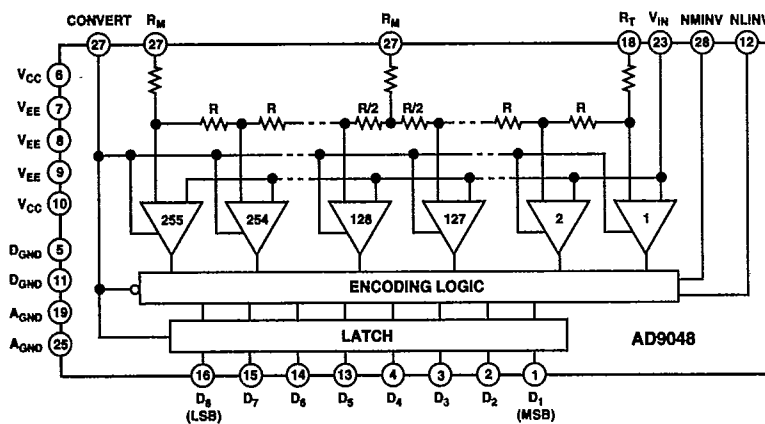
Test	Symbol	Device	Design Limits ¹	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 5, 6	Sub Group 7, 8	Sub Group 9	Test Conditions ²	Units
Input Bias Current	I_B	All		60	100					Measured with $V_{IN} = 0$ V; CONVERT low; $V_{CC} = +5.5$ V; $V_{EE} = -5.5$ V	μ A max
Input Resistance	R_I	All		200							k Ω min
Differential Nonlinearity	DNL	-1				0.75	1.0				LSB
		-2				0.5	0.75				
Integral Nonlinearity	INL	-1				0.75	1.0				LSB
		-2				0.5	0.75				
No Missing Codes		All				Guaranteed					
Reference Ladder Resistance	R_{RL}	All		50							Ω min
				125							Ω max
Reference Ladder Current	I_{RL}	All		40						$V_{EE} = -4.9$ V	mA max
Reference Ladder Offset (Top)	O_{RLT}	All		12	12					$+V_{REF} \geq -V_{REF}$ All Circumstances.	mV max
Reference Ladder Offset (Bottom)	O_{RLB}	All		8	8					$+V_{REF} \geq -V_{REF}$ All Circumstances	mV max
+0.4 V Input Current (NMINV; NLINV)		All		200	200					$V_{CC} = +5.5$ V; $V_{EE} = -4.9$ V	μ A max
+2.4 V Input Current (NMINV; NLINV)		All		10	10					$V_{CC} = +5.5$ V; $V_{EE} = -4.9$ V	μ A max
+5.5 V Input Current (NMINV; NLINV)		All		10	10					$V_{CC} = +5.5$ V; $V_{EE} = -4.9$ V	μ A max
Convert Pulse Voltage (HIGH)	$V_{C(H)}$	All						2.0			V min
Convert Pulse Voltage (LOW)	$V_{C(L)}$	All						0.8			V max
Convert Pulse Current (HIGH)	$I_{C(H)}$	All		15	15					$V_{CC} = +5.5$ V; $V_{EE} = -4.9$ V; $V_I = +2.4$ V	μ A max
Convert Pulse Current (HIGH)	$I_{C(H)}$	All		15	15					$V_{CC} = +5.5$ V; $V_{EE} = -4.9$ V; $V_I = +5.5$ V	μ A max
Convert Pulse Current (LOW)	$I_{C(L)}$	All		500	500					$V_{CC} = +5.5$ V; $V_{EE} = -4.9$ V	μ A max
High Level Output Voltage	V_{OH}	All		2.4	2.4					$V_{CC} = +4.5$ V	V min
Low Level Output Voltage	V_{OL}	All		0.5	0.5					$V_{CC} = +4.5$ V $V_{EE} = -5.5$ V	V max
Output Delay	t_{OD}	All							15		ns max
Output Hold Time	t_{OH}	All							5		ns min
Rise Time	t_R	All							9		ns max
Fall Time	t_F	All							14		ns max
Output Time Skew	t_{OS}	All							7		ns max

Test	Symbol	Device	Design Limits ¹	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 5, 6	Sub Group 7, 8	Sub Group 9	Test Conditions ²	Units
Signal-to-Noise Ratio @ 1.248 MHz A_{IN}	SNR	-1				43.5				RMS to RMS	dB min
		-2				45				Encode = 20 Msps	
Signal-to-Noise Ratio @ 1.248 MHz A_{IN}	SNR	-1				52.5				Peak to RMS	dB min
		-2				54				Encode = 20 Msps	
Harmonics @ 1.248 MHz A_{IN}	HD	-1				48				Encode = 20 Msps	dBc min
		-2				50					
Signal-to-Noise Ratio @ 2.438 MHz A_{IN}	SNR	-1				43				RMS to RMS	dB min
		-2				44				Encode = 20 Msps	
Signal-to-Noise Ratio @ 2.438 MHz A_{IN}	SNR	-1				52				Peak to RMS	dB min
		-2				53				Encode = 20 Msps	
Harmonics @ 2.438 MHz A_{IN}	HD	-1				47				Encode = 20 Msps	dBc min
		-2				49					
Signal-to-Noise Ratio @ 1.238 MHz A_{IN}	SNR	-1				43.5				RMS to RMS	dB min
		-2				45				Encode = 35 Msps	
Positive Supply Current	$+I_S$	All		46	46					$V_{CC} = +5.5 \text{ V};$ $V_{EE} = -5.5 \text{ V}$	mA max
Negative Supply Current	$-I_S$	All		110	110					$V_{CC} = +5.5 \text{ V};$ $V_{EE} = -5.5 \text{ V}$	mA max

NOTES

¹ Value shown is over full temperature range. Number in this column indicates specification is guaranteed but not tested.² $+V_{CC} = +5 \text{ V}; V_{EE} = -5.2 \text{ V};$ Differential Reference Voltage = 2.0 V, unless otherwise noted.

3.2.1 Functional Block Diagram and Terminal Assignments.



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3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (D-57).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

