

Product Features

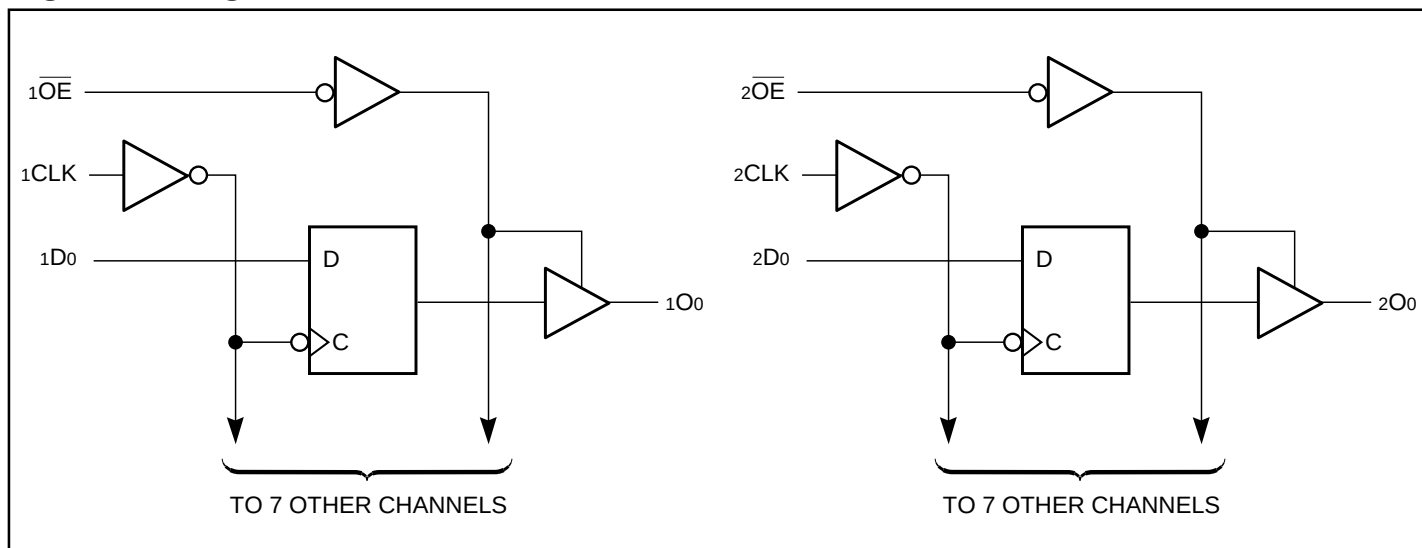
- Advanced Low Power CMOS Operation
- Can serve as a 5V to 3V translator
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
Compatible with LVC™ class of products.
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- Industrial operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Inputs can be driven by 3.3V or 5V devices
- Multiple center pin and distributed Vcc/GND pins minimizing switching noise
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A)
 - 48-pin 300 mil wide plastic SSOP (V)
 - 48-pin 173 mil wide plastic TVSOP (K)

Product Description

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT163374 is a 16-bit octal register designed with 16 D-type flip-flops with a buffered common clock and 3-state outputs. The Output Enable ($\overline{\text{xOE}}$) and clock (xCLK) controls are organized to operate as two 8-bit registers or one 16-bit register. When $\overline{\text{OE}}$ is HIGH, the outputs are in the high-impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

Logic Block Diagram



Product Pin Description

Pin Name	Description
$\overline{xOE}$	3-State Output Enable Inputs (Active LOW)
$xCLK$	Clock Inputs
xDx	Data Inputs
xOx	3-State Outputs
GND	Ground
V _{CC}	Power

Truth Table

Function	Inputs ⁽¹⁾			Outputs ⁽¹⁾
	xDx	$xCLK$	$\overline{xOE}$	xOx
High-Z	X	L	H	Z
	X	H	H	Z
Load Register	L		L	L
	H		L	H
	L		H	Z
	H		H	Z

Product Pin Configuration

$\overline{1OE}$	1	48	$1CLK$
$1O0$	2	47	$1D0$
$1O1$	3	46	$1D1$
GND	4	45	GND
$1O2$	5	44	$1D2$
$1O3$	6	43	$1D3$
V _{CC}	7	42	V _{CC}
$1O4$	8	41	$1D4$
$1O5$	9	40	$1D5$
GND	10	39	GND
$1O6$	11	38	$1D6$
$1O7$	12	37	$1D7$
$2O0$	13	36	$2D0$
$2O1$	14	35	$2D1$
GND	15	34	GND
$2O2$	16	33	$2D2$
$2O3$	17	32	$2D3$
V _{CC}	18	31	V _{CC}
$2O4$	19	30	$2D4$
$2O5$	20	29	$2D5$
GND	21	28	GND
$2O6$	22	27	$2D6$
$2O7$	23	26	$2D7$
$\overline{2OE}$	24	25	$2CLK$

Note:

- H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Z = High Impedance

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0 V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0 V	5.5	8	pF

Note:

- This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–55°C to +125°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only) ...	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = –40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level		2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)			2.0	—	Vcc+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max.	VIN = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)	VCC = Max.	VIN = VCC	—	—	±1	µA
IIL	Input LOW Current (Input pins)	VCC = Max.	VIN = GND	—	—	±1	µA
	Input LOW Current (I/O pins)	VCC = Max.	VIN = GND	—	—	±1	µA
IOZH	High Impedance Output Current (3-State Output pins)	VCC = Max.	VOU = VCC	—	—	±1	µA
IOZL		VCC = Max.	VOU = GND	—	—	±1	µA
VIK	Clamp Diode Voltage	VCC = Min., IIN = –18mA		—	–0.7	–1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾		–36	–60	–110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾		50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min. VIN = VIH or VIL	IOH = –0.1mA	Vcc-0.2	—	—	V
			IOH = –3mA	2.4	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL	IOH = –8mA	2.4 ⁽⁵⁾	3.0	—	V
			IOH = –24mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min. VIN = VIH or VIL	IOL = 0.1mA	—	—	0.2	V
			IOL = 16mA	—	0.2	0.4	V
			IOL = 24mA	—	0.3	0.5	V
Ios mA	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND			–60	–85	–240
VH	Input Hysteresis			—	150	—	mV

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. VOH = VCC – 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
ICC	Quiescent Power Supply Current	VCC = Max.	VIN = GND or VCC		0.1	10	μA
ΔICC	Quiescent Power Supply Current TTL Inputs HIGH	VCC = Max.	VIN = VCC – 0.6V ⁽³⁾		2.0	30	μA
ICCD	Dynamic Power Supply ⁽⁴⁾	VCC = Max., Outputs Open XOE = GND One Bit Toggling 50% Duty Cycle	VIN = VCC VIN = GND		50	75	μA/ MHz
IC	Total Power Supply Current ⁽⁶⁾	VCC = Max., Outputs Open fI = 10 MHz 50% Duty Cycle XOE = GND One Bit Toggling	VIN = VCC – 0.6V VIN = GND		0.5	0.8	mA
		VCC = Max., Outputs Open fI = 2.5 MHz 50% Duty Cycle XOE = GND 16 Bits Toggling	VIN = VCC – 0.6V VIN = GND		2.5	4.0 ⁽⁵⁾	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at Vcc = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at Vcc or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
- IC = IQUIESCENT + IINPUTS + IDYNAMIC
 IC = ICC + ΔICC DHNT + ICCD (fCP/2 + fINI)
 ICC = Quiescent Current (ICCL, ICCH and ICCZ)
 ΔICC = Power Supply Current for a TTL High Input
 DH = Duty Cycle for TTL Inputs High
 NT = Number of TTL Inputs at DH
 ICCD = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 fCP = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 NCP = Number of Clock Inputs at fCP
 fI = Input Frequency
 NI = Number of Inputs at fI
 All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	FCT163374		FCT163374A		FCT163374C		Units
			Com.		Com.		Com.		
			Min. ⁽³⁾	Max.	Min. ⁽³⁾	Max.	Min. ⁽³⁾	Max.	
tPLH tPHL	Propagation Delay xCLK to xOx	CL = 50pF RL = 500Ω	2.0	10.0	2.0	6.5	2.0	5.2	ns
tPZH tPZL	Output Enable Time xOE to xOx		1.5	12.5	1.5	6.5	1.5	5.5	ns
tPHZ tPLZ	Output Disable Time ⁽⁴⁾ xOE to xOx		1.5	8.0	1.5	5.5	1.5	5.0	ns
tSU	Setup Time HIGH or LOW, xDx to xCLK		2.0		2.0		2.0		ns
tH	Hold Time HIGH or LOW, xDx to xCLK		1.5		1.5		1.5		ns
tW	xCLK Pulse Width HIGH ⁽⁴⁾		7.0		5.0		5.0		ns
tSK(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with $V_{cc} = 3.3V \pm 0.3V$, normal range. For $V_{cc} = 2.7V$, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.