Fast CMOS 16-Bit Latched Transceivers

Product Features:

Common Features:

- PI74FCT16543T and PI74FCT162543T have have high current drive and four speed grades.
  - Standard speeds at 8.5 ns max.
  - "A" speeds at 6.5 ns max.
  - "C" speeds at 5.3 ns max.
  - "D" speeds at 4.4 ns max.
  - "E" speeds at 3.4 ns max.
- V_{CC} = 5 V ±10%
- Hysteresis on all inputs
- Packaged in 56-pin plastic TSSOP and SSOP

PI74FCT16543T Features:

- High output drive: I_{OH} = –32 mA; I_{OL} = 64 mA
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) < 1.0 V at V_{CC} = 5 V, T_A = 25°C

PI74FCT162543T Features:

- Balanced output drivers: ±24 mA
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.6 V at V_{CC} = 5 V, T_A = 25°C

Product Description:

Pioneer Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

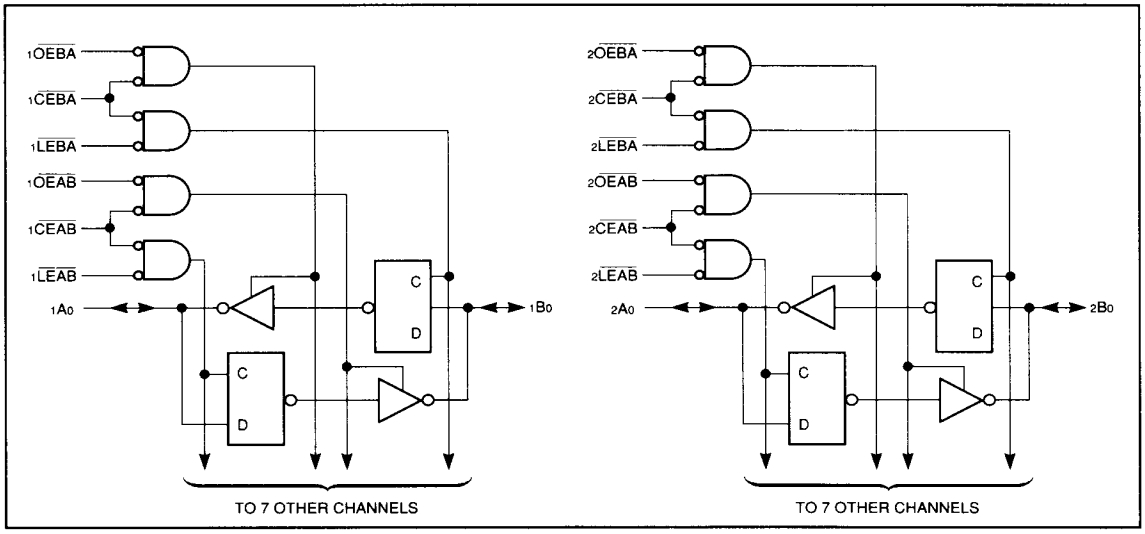
The PI74FCT16543T and PI74FCT162543T are 16-bit latched transceivers organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable (x$\overline{CEAB}$) input must be LOW in order to enter data from xAx or to take data from xBx, as indicated in the Truth Table. With x$\overline{CEAB}$ LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the x$\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With x$\overline{CEAB}$ and x$\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the x$\overline{CEBA}$, x$\overline{LEBA}$, and x$\overline{OEBA}$ inputs.

The PI74FCT16543T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74FCT162543T has ±24 mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Both products are available in 56-pin 240 mil wide plastic TSSOP and 300 mil wide plastic SSOP packages.

Logic Block Diagram



Product Pin Description

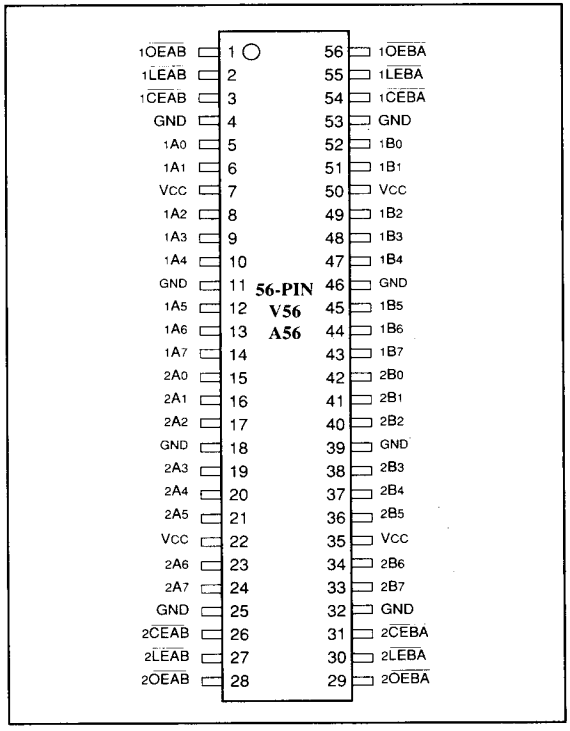
Pin Name	Description
xOEAB	A-to-B Output Enable Input (Active LOW)
xOEBA	B-to-A Output Enable Input (Active LOW)
xCEAB	A-to-B Enable Input (Active LOW)
xCEBA	B-to-A Enable Input (Active LOW)
xLEAB	A-to-B Latch Enable Input (Active LOW)
xLEBA	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or B-to-A 3-State Outputs
GND	Ground
Vcc	Power

Truth Table[1]

Inputs			Latch Status	Output Buffers
xCEAB	xLEAB	xOEAB	xAx to xBx	xBx
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

NOTES:
1. *Before xLEAB LOW-to-HIGH Transistion
   H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care or Irrelevant
   Z = High Impedance
2. A-to-B data flow shown. B-to-A flow control is the same, except using xCEBA, xLEBA, and xOEBA.

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–55°C to +125°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to Vcc
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = V_{CC}			±5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = GND			±5	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_{OUT} = 2.7 V			±10	µA
I_{OZL}	Output Current	V_{CC} = Max.	V_{OUT} = 0.5 V			±10	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max.[3], V_{OUT} = 2.5 V		–50		–180	mA
V_H	Input Hysteresis				100		mV

PI74FCT16543T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3.0 mA	2.5	3.5		V
			I_{OH} = –15.0 mA	2.4	3.5		
			I_{OH} = –32.0 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64 mA		0.2	0.55	V
I_{OFF}	Power Down Disable	V_{CC} = 0 V, V_{IN} or V_{OUT} ≤ 4.5 V		--	—	±100	µA

PI74FCT162543T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –24.0 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA		0.3	0.55	V
I_{ODL}	Output LOW Current	V_{CC} = 5 V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5 V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5 V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5 V[3]		–60	–115	–150	mA

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	5.5	8	pF

Notes:
1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		2	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4 V[3]		0.5	1.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $x\overline{CEAB}$ & $x\overline{OEAB}$ = GND $x\overline{CEBA}$ = V_{CC} One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10 MHz 50% Duty Cycle $x\overline{LEAB}$, $x\overline{CEAB}$, and $x\overline{OEAB}$ = GND $x\overline{CEBA}$ = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND		0.7	2.5[5]	mA
			V_{IN} = 3.4 V V_{IN} = GND		0.9	3.3[5]	
		V_{CC} = Max., Outputs Open f_i = 2.5 MHz 50% Duty Cycle $x\overline{LEAB}$, $x\overline{CEAB}$, and $x\overline{OEAB}$ = GND $x\overline{CEBA}$ = V_{CC} 16 Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND		2.5	5.5[5]	
			V_{IN} = 3.4 V V_{IN} = GND		6.5	17.5[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 5.0 V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4 V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4 V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16543T Switching Characteristics over Operating Range

Preliminary

Parameters	Description	Conditions[1]	'16543T Com. Min	'16543T Com. Max	'16543AT Com. Min	'16543AT Com. Max	'16543CT Com. Min	'16543CT Com. Max	'16543DT Com. Min	'16543DT Com. Max	'16543ET Com. Min	'16543ET Com. Max	Unit
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50 pF RL = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	1.5	3.4	ns
tPLH tPHL	Propagation Delay $\overline{xLEBA}$ to xAx, $\overline{xLEAB}$ to xBx		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	1.5	3.7	ns
tPZH tPZL	Output Enable Time $\overline{xOEBA}$ or $\overline{xOEAB}$ to xAx or xBx		2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	1.5	4.8	ns
tPHZ tPLZ	Output Disable Time $\overline{xOEBA}$ or $\overline{xOEAB}$ to xAx or xBx		2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	1.5	4.0	ns
tSU	Set-up Time HIGH or LOW xAx or xBx to $\overline{xLEAB}$ or $\overline{xLEBA}$		3.0	—	2.0	—	2.0	—	1.5	—	1.0	—	ns
tH	Hold Time HIGH or LOW xAx or xBx to $\overline{xLEAB}$ or $\overline{xLEBA}$		2.0	—	2.0	—	2.0	—	1.5	—	1.0	—	ns
tW	$\overline{xLEAB}$ or $\overline{xLEBA}$ Pulse Width LOW		5.0	—	5.0	—	5.0	—	3.0	—	3.0[4]	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

PI74FCT162543T Switching Characteristics over Operating Range

Preliminary

Parameters	Description	Conditions[1]	'162543T Com. Min	'162543T Com. Max	'162543AT Com. Min	'162543AT Com. Max	'162543CT Com. Min	'162543CT Com. Max	'162543DT Com. Min	'162543DT Com. Max	'162543ET Com. Min	'162543ET Com. Max	Unit
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50 pF RL = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	1.5	3.4	ns
tPLH tPHL	Propagation Delay $\overline{xLEBA}$ to xAx, $\overline{xLEAB}$ to xBx		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	1.5	3.7	ns
tPZH tPZL	Output Enable Time $\overline{xOEBA}$ or $\overline{xOEAB}$ to xAx or xBx		2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	1.5	4.8	ns
tPHZ tPLZ	Output Disable Time $\overline{xOEBA}$ or $\overline{xOEAB}$ to xAx or xBx		2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	1.5	4.0	ns
tSU	Set-up Time HIGH or LOW xAx or xBx to $\overline{xLEAB}$ or $\overline{xLEBA}$		3.0	—	2.0	—	2.0	—	1.5	—	1.0	—	ns
tH	Hold Time HIGH or LOW xAx or xBx to $\overline{xLEAB}$ or $\overline{xLEBA}$		2.0	—	2.0	—	2.0	—	1.5	—	1.0	—	ns
tW	$\overline{xLEAB}$ or $\overline{xLEBA}$ Pulse Width LOW		5.0	—	5.0	—	5.0	—	3.0	—	3.0[4]	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. This limit is gauranteed but not tested.