ANALOG DEVICES

Fast, Complete 12-Bit A/D Converter

1.1 Scope.

This specification covers the detail requirements of a hybrid, high speed, 12-bit successive approximation analog-to-digital converter including internal clock, reference and comparator.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD ADC85S-12/883B
–2	AD ADC85SZ-12/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-32F.

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage	±18V
Logic Supply Voltage	+7V
Analog Inputs (Pins 24, 25)	±25V
Digital Inputs	+5.5V
Junction Temperature	+175°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 8°C/W
θ_{JA} = 38°C/W

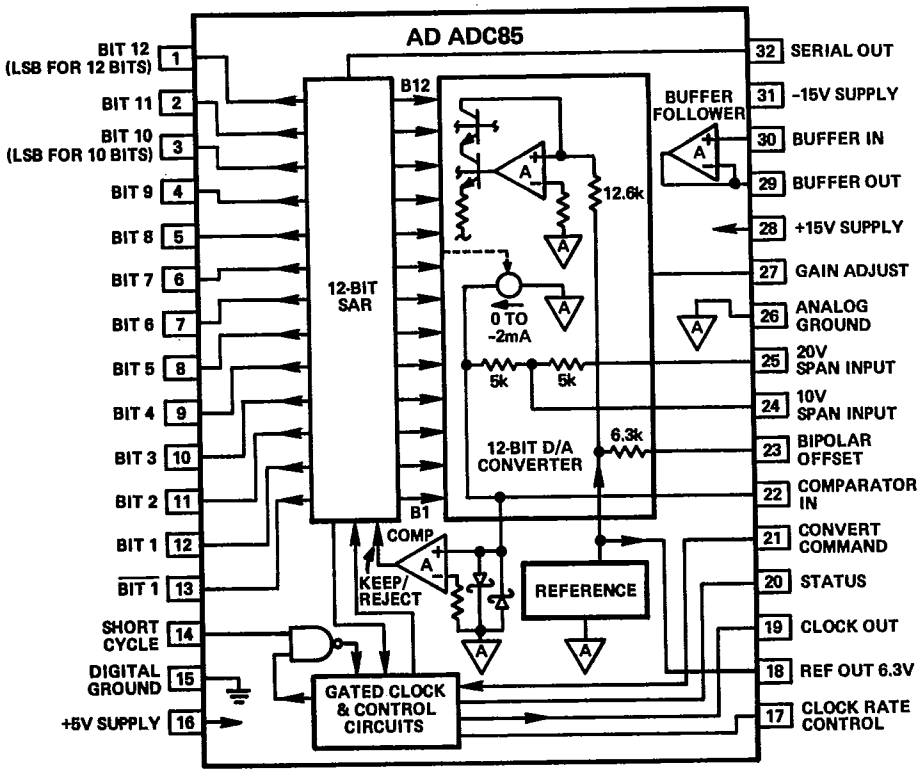
Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2,3	Sub Group 4	Sub Group 7	Test Condition[1]	Units
Analog Input Voltage Ranges	V_{IN}	−1	±2.5, ±5, ±10 0 to 5 0 to 10						V
	V_{IN}	−2	±2.5, ±5 0 to 5					$\pm V_{CC} = \pm 12V$ $+V_{DD} = +5V$	V
Input Impedance			3					10V Range	kΩ min
Buffer Amp Bias Current	I_B	−1,2	100				100		±nA max
Buffer Amp Offset Error		−1,2	10				10		±mV max
Buffer Amp Common-Mode Rejection		−1,2	70				70		dB min
Buffer Amp Settling Time		−1,2	2					T_A = 25°C To 0.01% for 10V Step	µs max
Reference Output Error	V_{REF}	−1,2	15	15				6.3V Nominal	±mV max
Reference Voltage Drift	V_{REFD}	−1,2	20		20			+5V Input Range	±ppm/°C max
Unipolar Gain Error[2]	V_{GE}	−1,2	0.25	0.25				0 to 10V Input Range	±% FSR max
Unipolar Offset Error[2]	V_{OSE}	−1,2	0.2	0.2				0 to 10V Input Range	±% FSR max
Unipolar Offset Drift	V_{OSD}	−1,2	5		5			0 to 10V Input Range	±ppm/°C max
Bipolar Gain Error[2]	V_{GE}	−1,2	0.25	0.25				±10V Input Range	±% FSR max
Bipolar Gain Drift	V_{FSE}	−1,2	25		25			±10V Input Range	±ppm/°C max
Bipolar Offset Error[2]	V_{OSE}	−1,2	0.25	0.25				±10V Input Range	±% FSR max
Bipolar Offset Drift	V_{OSD}	−1,2	10		10			±5V Input Range	±ppm/°C max
Linearity Error	RA	−1,2	1/2				1/2	Major Carries & Summations	±LSB max
Differential Linearity Error[3]	DNL	−1,2	1		1		1	Major Carries & Summations	±LSB max
+5V Power Supply Sensitivity	$PSRR_1$	−1,2	0.01				0.01	$+V_{DD}$ = 4.75V to 5.25V	±% FSR/% max
±15V Power Supply Sensitivity	$PSRR_2$	−1	0.04				0.04	$\pm V_{CC}$ = ±14.55V to 15.45V	±% FSR/% max
±12V Power Supply Sensitivity	PSRR	−2	0.04				0.04	$\pm V_{CC}$ = ±11.4V to ±12.6V	±% FSR/% max
Clock Adjust		−1,2	0.1	1.0				To 10V	µs/V min
Conversion Speed[4]	t_C	−1,2	10 8.4			10 8.4		To 12 Bits To 10 Bits	µs max
Serial/Parallel Code Match Error	SP_{CM}	−1,2	0				0		±Bits
Output High Drive	V_{OH}	−1,2	2.4				2.4	@ −80µA	V min
Output Low Drive	V_{OL}	−1,2	0.4				0.4	@ 3.2mA	V max
+5V (+V_{DD}) Supply Drain	$+I_{DD}$	−1,2	140				140	All Bits On	+mA max
+15V (+V_{CC}) Supply Drain	$+I_{CC}$	−1,2	25				25	All Bits On	+mA max
−15V (−V_{CC}) Supply Drain	$-I_{CC}$	−1,2	35				35	All Bits On	−mA max
Total Power Dissipation	P_D	−1,2	1.5				1.5	All Bits On	W max

Test	Symbol	Device	Design Limit @+25°C	Sub Group 1	Sub Group 2,3	Sub Group 4	Sub Group 7	Test Condition[1]	Units
Power Supply Range	$+V_{DD}$ $\pm V_{CC}$	−1	±5 ±10					For Rated Accuracy	%
	$+V_{DD}$ $\pm V_{CC}$	−2	±5 ±11.4 to ±16.5					For Rated Accuracy	V

NOTES
[1]V_{CC} = ±15V, V_{DD} = +5V unless otherwise noted.
[2]Adjustable to zero.
[3]V_{CC} = ±12 for the −2 version. No missing codes guaranteed with internal clock.
[4]With internal clock, Pin 17 tied to +5V.

3.2.1 Functional Block Diagram and Terminal Assignments.

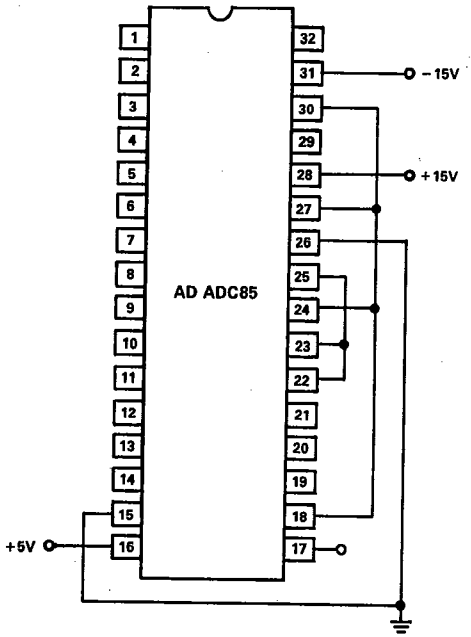


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



6.1 Clock Rate Control, Offset Adjust and Gain Adjust Connections.

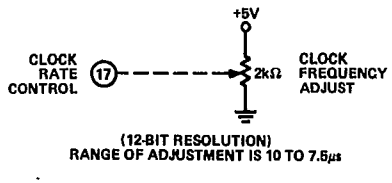


Figure 1. 12-Bit Clock Rate Control Optional Fine Adjust

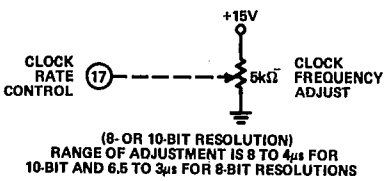


Figure 2. 8-Bit Clock Rate Control Optional Fine Adjust

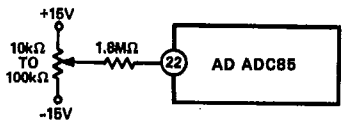


Figure 3. Offset Adjust Circuit

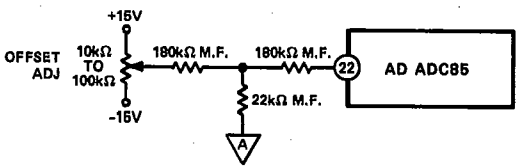


Figure 4. Low Tempco Zero Adjustment Circuit

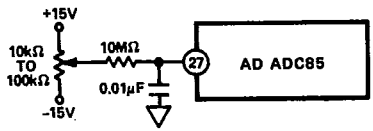


Figure 5. Gain Adjustment Circuit

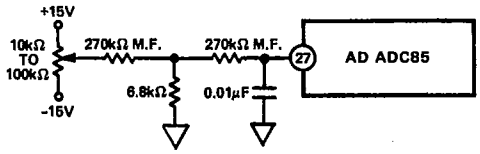


Figure 6. Low Tempco Gain Adjustment Circuit

Table 2. Short Cycle Connections

Connect Short Cycle Pin 14 To Pin:	Connect Clock Rate Control Pin 17 To	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
16	15	12	0.024	10	t_{12} +40ns
2	16	10	0.100	6	t_{10} +40ns
4	28	8	0.390	3.2	t_8 +40ns

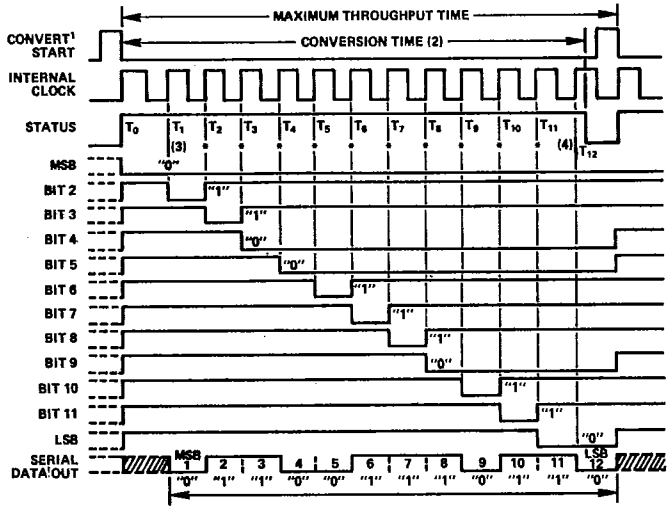


Figure 7. Timing Diagram (Binary Code 0 1 1 0 0 1 1 1 0 1 1 0)

Table 3. Input Voltages and Code Definition

INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 . . . 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES:
*COB = Complementary Offset Binary
**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available to pin 13.
***CSB = Complementary Straight Binary.
****Voltages given are the nominal value for transition to the code specified.

Table 4. AD ADC85 Input Scaling Connections

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Direct Input Connect Input Signal To	For Buffered Input Pin 30 Connect Pin 29 To Pin
±10V	COB or CTC	22	Input Signal	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0V to +5V	CSB	26	Pin 22	24	24
0V to +10V	CSB	26	Open	24	24