Fast CMOS Registered Transceivers

Product Features:

- PI74FCT2952/2953AT have the same speed and drive of Bipolar FAST™ "F" series, at CMOS power levels.
  - "B" speeds at 7.5 ns max.
  - "C" speeds at 6.3 ns max.
  - "D" speeds are an industry first, at 4.5 ns max.
- TTL input and output levels, reducing problematic "ground bounce"
- High output drive, I_{OL} = 64 mA
- Extremely low static power (1 mW, typ.)
- Industry standard pinout, plug into existing "74F" sockets for speed enhancement at reduced power levels
- Hysteresis on all inputs
- Packaged in 24-pin plastic DIP, surface mount SOIC, or the industry's new "1/4 size" surface mount QSOP

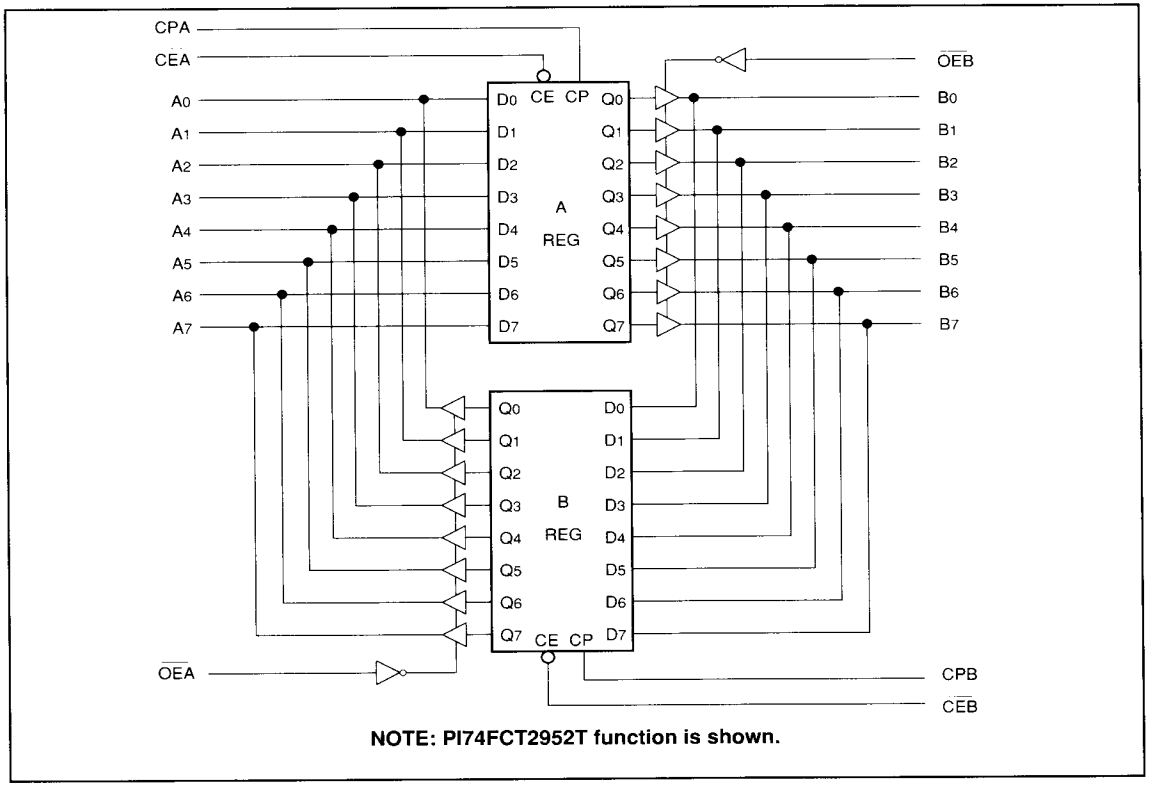
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT2952T and the PI74FCT2953T are 8-bit registered transceivers designed with two 8-bit back-to-back registers to store data flowing in both directions between two bidirectional buses. Separate clock enable and 3-state output enable signals are provided for each register. The PI74FCT2952T is a non-inverting option of the PI74FCT2953T.

All products are available in three package types: 24-pin, 300 mil wide plastic DIP, 300 mil wide plastic SOIC, and the industry's new 150 mil wide QSOP (one quarter the size of an SOIC).

PI74FCT2952T and PI74FCT2953T Logic Block Diagram



NOTE: PI74FCT2952T function is shown.

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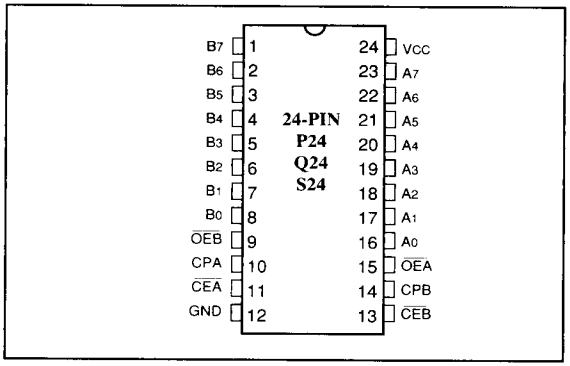
PI74FCT2952/2953T Product Pin Configuration



Product Pin Description

Pin Name	Description
A0-A7	A Register Inputs or B Register Outputs
B0-B7	B Register Inputs or A Register Outputs
CPA	Clock for A Register
CPB	Clock for B Register
$\overline{OEA}$	Output Enable for B Register
OEB	Output Enable for A Register
$\overline{CEA}$	Clock Enable for A Register
$\overline{CEB}$	Clock Enable for B Register
GND	Ground
VCC	Power

PI74FCT2952/2953T Register Truth Table[1]
(Applies to A or B Register)

	Inputs			Internal
Function	D_N	CP	$\overline{CE}$	Q_N
Hold Data	X	X	H	NC
Load Data	L	↑	L	L
	H	↑	L	H

PI74FCT2952/2953T Output Control Table[1]

		Internal	Y-Outputs	
Function	$\overline{OE}$	Q_N	2952	2953
Disable Outputs	H	X	Z	Z
Enable Outputs	L	L	L	H
	L	H	H	L

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
   NC = No Change
   ↑ = LOW-to-HIGH transition

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to Vcc
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8.0 mA	2.4	3.3		V
			I_{OH} = –15.0 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64 mA		0.3	0.55	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V	Except I/O Pins			5	µA
			I/O Pins			15	
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5 V	Except I/O Pins			–5	µA
			I/O Pins			–15	
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC} (Max.)				20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–60	–120		mA
I_{OFF}	Power Down Disable	V_{CC} = GND, V_{OUT} = 4.5 V		—	—	100	µA
V_H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF

Notes:
1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.5	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4 V[3]		0.5	2.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $\overline{OEA}$ or $\overline{OEB}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10 MHz 50% Duty Cycle $\overline{OEA}$ or $\overline{OEB}$ = GND f_i = 5 MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND		2.0	4.0[5]	mA
			V_{IN} = 3.4 V V_{IN} = GND		2.5	6.0[5]	
		V_{CC} = Max., Outputs Open f_{CP} = 10 MHz 50% Duty Cycle $\overline{OEA}$ or $\overline{OEB}$ = GND Eight Bits Toggling f_i = 2.5 MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		4.3	7.8[5]	
			V_{IN} = 3.4 V V_{IN} = GND		6.5	16.8[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0 V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4 V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4 V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

PI74FCT2952T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	FCT2952AT Com. Min	FCT2952AT Com. Max	FCT2952BT Com. Min	FCT2952BT Com. Max	FCT2952CT Com. Min	FCT2952CT Com. Max	FCT2952DT Com. Min	FCT2952DT Com. Max	Unit
t_{PLH}	Propagation Delay	C_L = 50 pF	2.0	10.0	2.0	7.5	2.0	6.3	2.0	4.5	ns
t_{PHL}	CPA, CPB, to A_N, B_N	R_L = 500Ω									
t_{PZH}	Output Enable Time		1.5	10.5	1.5	8.0	1.5	7.0	1.5	5.6	ns
t_{PZL}	$\overline{OEA}$, $\overline{OEB}$, to A_N, B_N										
t_{PHZ}	Output Disable Time		1.5	10.0	1.5	7.5	1.5	6.5	1.5	4.3	ns
t_{PLZ}	$\overline{OEA}$, $\overline{OEB}$, to A_N, B_N										
t_{SU}	Set-up Time HIGH or LOW, A_N, B_N to CPA, CPB		2.5	—	2.5	—	2.5	—	1.5	—	ns
t_H	Hold Time HIGH or LOW, A_N, B_N to CPA, CPB		2.0	—	1.5	—	1.5	—	1.0	—	ns
t_{SU}	Set-up Time HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		3.0	—	3.0	—	3.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		2.0	—	2.0	—	2.0	—	1.0	—	ns
t_W	Pulse Width HIGH[3] or LOW, CPA or CPB		3.0	—	3.0	—	3.0	—	3.0	—	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

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PI74FCT2953T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	FCT2953AT Com.		FCT2953BT Com.		FCT2953CT Com.		FCT2953DT Com.		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB, to A_N, B_N	C_L = 50 pF R_L = 500Ω	2.0	10.0	2.0	7.5	2.0	6.3	2.0	4.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$, $\overline{OEB}$, to A_N, B_N		1.5	10.5	1.5	8.0	1.5	7.0	1.5	5.6	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$, $\overline{OEB}$, to A_N, B_N		1.5	10.0	1.5	7.5	1.5	6.5	1.5	4.3	ns
t_{SU}	Set-up Time HIGH or LOW, A_N, B_N to CPA, CPB		2.5	—	2.5	—	2.5	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, A_N, B_N to CPA, CPB		2.0	—	1.5	—	1.5	—	1.0	—	ns
t_{SU}	Set-up Time HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		3.0	—	3.0	—	3.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		2.0	—	2.0	—	2.0	—	1.0	—	ns
t_W	Pulse Width HIGH[3] or LOW, CPA or CPB		3.0	—	3.0	—	3.0	—	3.0	—	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.