8-Bit, high-speed, μP-compatible A/D converter with track/hold function

ADC0820

DESCRIPTION

By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5μs conversion time while dissipating a maximum 75mW of power. The half-flash technique consists of 31 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820 is tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold for signals slewing at less than 100mV/μs.

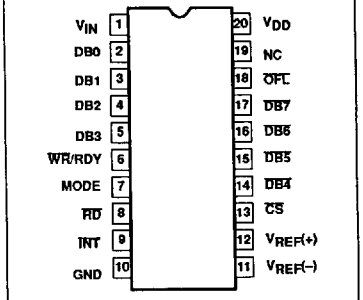
For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

FEATURES

- Built-in track-and-hold function
- No missing codes
- No external clocking
- Single supply—$5V_{DC}$
- Easy interface to all microprocessors, or operates stand-alone
- Latched 3-State outputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than VDD
- 0V to 5V analog input voltage range with single 5V supply
- No zero- or full-scale adjust required
- Overflow output available for cascading
- 0.3″ standard width 20-pin DIP

PIN CONFIGURATION

D, F, N Packages

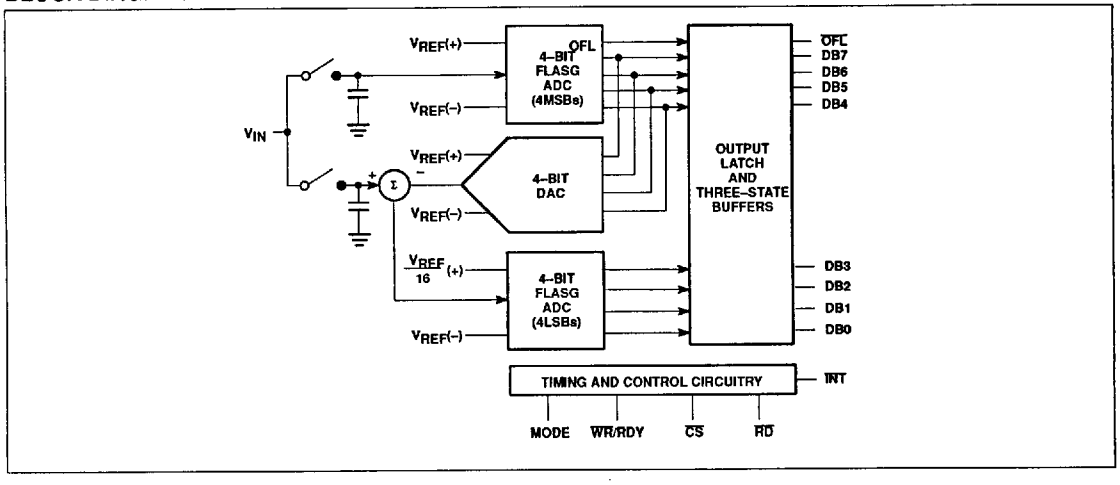


TOP VIEW

APPLICATIONS

- Microprocessor-based monitoring and control systems
- Transducer/μP interface
- Process control
- Logic analyzers
- Test and measurement

BLOCK DIAGRAM



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ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	ADC0820BNEN
20-Pin Plastic SO package	0 to +70°C	ADC0820BNED
20-Pin Plastic DIP	0 to +70°C	ADC0820CNEN
20-Pin Plastic SO package	0 to +70°C	ADC0820CNED
20-Pin Plastic DIP	-40 to +85°C	ADC0820BSAN
20-Pin Plastic SO package	-40 to +85°C	ADC0820BSAD
20-Pin Plastic DIP	-40 to +85°C	ADC0820CSAN
20-Pin Plastic SO package	-40 to +85°C	ADC0820CSAD
20-Pin Ceramic DIP	-55 to +125°C	ADC0820BSEF
20-Pin Ceramic DIP	-55 to +125°C	ADC0820CSEF

PIN DESCRIPTION

PIN NO	SYMBOL	DESCRIPTION
1	V_{IN}	Analog input; range=GND≤V_{IN}≤V_{DD}
2	DB0	3-state data output—Bit 0 (LSB)
3	DB1	3-state data output—Bit 1
4	DB2	3-state data output—Bit 2
5	DB3	3-state data output—Bit 3
6	$\overline{WR}$/RDY	**WR-RD Mode** $\overline{WR}$: With $\overline{CS}$ Low, the conversion is started on the falling edge of $\overline{WR}$. Approximately 800ns (the preset internal time out, t_I) after the $\overline{WR}$ rising edge, the result of the conversion will be strobed into the output latch, provided that $\overline{RD}$ does not occur prior to this time out (see Figures 3a and 3b). **RD Mode** RDY: This is an open-drain output (no internal pull-up device). RDY will go Low after the falling edge of $\overline{CS}$; RDY will go 3-State when the result of the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system (see Figure 1).
7	Mode	Mode: Mode selection input—it is internally tied to GND through a 30µA current source. RD Mode: When mode is Low. WR-RD Mode: When mode is High.
8	$\overline{RD}$	**WR-RD Mode** With $\overline{CS}$ Low, the 3-State data outputs (DB0-DB7) will be activated when $\overline{RD}$ goes Low. $\overline{RD}$ can also be used to increase the speed of the converter by reading data prior to the preset internal time out (T_I ~ 800ns). If this is done, the data result transferred to output latch is latched after the falling edge of the $\overline{RD}$ (see Figures 3a and 3b). **RD Mode** With $\overline{CS}$ Low, the conversion will start with $\overline{RD}$ going Low; also, $\overline{RD}$ will enable the 3-State data outputs at the completion of the conversion. RDY going 3-State and $\overline{INT}$ going Low indicate the completion of the conversion (see Figure 1).
9	$\overline{INT}$	**WR-RD Mode** $\overline{INT}$ going Low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ will go Low ~ 800ns (the preset internal time out, t_I) after the rising edge of $\overline{WR}$ (see Figure 3a); or $\overline{INT}$ will go Low after the falling edge of $\overline{RD}$, if $\overline{RD}$ goes Low prior to the 800ns time out (see Figure 3b). $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see Figures 3a and 3b). **RD Mode** $\overline{INT}$ going Low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see Figure 1).
10	GND	Ground

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PIN DESCRIPTION (Continued)

11	$V_{REF}(-)$	The bottom of resistor ladder, voltage range: $GND \leq V_{REF}(-) \leq V_{REF}(+)$
12	$V_{REF}(+)$	The top of resistor ladder, voltage range: $V_{REF}(-) \leq V_{REF}(+) \leq V_{DD}$.
13	$\overline{CS}$	$\overline{CS}$ must be Low in order for the $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.
14	DB4	3-State data output—Bit 4
15	DB5	3-State data output—Bit 5
16	DB6	3-State data output—Bit 6
17	DB7	3-State data output—Bit 7 (MSB)
18	$\overline{OFL}$	Overflow output—if the analog input is higher than the $V_{REF}(+)$- LSB, $\overline{OFL}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to have more resolution (9, 10-bit).
19	NC	No connection
20	V_{DD}	Power supply voltage

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage	7	V
	Logic control inputs	-0.2 to V_{DD}+0.2	V
	Voltage at other inputs and output	-0.2 to V_{DD}+0.2	V
T_{STG}	Storage temperature range	-65 to +150	°C
P_D	Maximum power dissipation[3] T_A=25°C(still-air)		
	F package	1560	mW
	N package	1690	mW
	D package	1390	mW
T_{SOLD}	Lead temperature (soldering, 10sec)	300	°C
T_A	Operating ambient temperature range	$T_{MIN} \leq T_A \leq T_{MAX}$	
	ADC0820BSEF/CSEF	–55 to +125	°C
	ADC0820BSAN/CSAN/BSAD/CSAD	–40 to +85	°C
	ADC0820BNEN/CNEN/BNED/CNED	0 to +70	°C

NOTES:
1. Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.
2. All voltages are measured with respect to GND, unless otherwise specified.
3. Derate above 25°C at the following rates:
   F package at 12.5mW/°C
   N package at 13.5mW/°C
   D package at 11.1mW/°C

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DC ELECTRICAL CHARACTERISTICS

RD mode (Pin 7=0), V_{DD}=5V, $V_{REF}(+)$=5V, and $V_{REF}(-)$=GND, unless otherwise specified. Limits apply from T_{MIN} to T_{MAX}.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ[3]	Max	
	Resolution			8	8	8	bits
	Unadjusted error[1]	ADC0820B				±1/2	LSB
		ADC0820C				±1	LSB
R_{REF}	Reference resistance			1	1.6	4	kΩ
$V_{REF}(+)$	Input voltage			$V_{REF}(-)$		V_{DD}	V
$V_{REF}(-)$	Input voltage			GND		$V_{REF}(+)$	V
V_{IN}	Input voltage			GND-0.1		V_{DD}+0.1	V
	Maximum analog input leakage current	$\overline{CS}$=V_{DD} V_{IN}=V_{DD} V_{IN}=GND		-3		3	µA
	Power supply sensitivity	V_{DD}=5V±5%			±1/16	±1/4	LSB
$V_{IN(1)}$	Logical "1" input voltage	V_{DD}=5.25V	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	2.0		V_{DD}	V
			Mode	3.5		V_{DD}	V
$V_{IN(0)}$	Logical "0" input voltage	V_{DD}=4.75V	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	GND		0.8	V
			Mode	GND		1.5	V
$I_{IN(1)}$	Logical "1" input current	$V_{IN(1)}$=5V; $\overline{CS}$, $\overline{RD}$				1	µA
		$V_{IN(1)}$=5V; $\overline{WR}$				3	µA
		$V_{IN(1)}$=5V; Mode			30	200	µA
$I_{IN(0)}$	Logical "0" input current	$V_{IN(0)}$=0V; $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, Mode		-1			µA
$V_{OUT(1)}$	Logical "1" output voltage	V_{DD}=4.75V, I_{OUT}=-360µA; DB0-DB7, $\overline{OFL}$, $\overline{INT}$		2.4	4.6		V
		V_{DD}=4.75V, I_{OUT}=-10µA DB0-DB7, $\overline{OFL}$, $\overline{INT}$		4.5	4.74		V
$V_{OUT(0)}$	Logical "0" output voltage	V_{DD}=4.75V, I_{OUT}=1.6mA; DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY			0.2	0.4	V
I_{OZ}	3-state output current	V_{OUT}=5V; DB0-DB7, RDY				3	µA
		V_{OUT}=0V; DB0-DB7, RDY		-3			µA
I_{SOURCE}	Output source current	V_{OUT}=0V, DB0-DB7, $\overline{OFL}$		6	12		mA
		$\overline{INT}$		4.5	8		mA
I_{SINK}	Output sink current	V_{OUT}=5V; DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY		7	20		mA
I_{DD}	Supply current	$\overline{CS}$=$\overline{WR}$=$\overline{RD}$=0			6	15	mA
V_{DD}	Range			4.5		5.5	V

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AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, $t_R = t_F$ = 20ns, $V_{REF(+)}$ = 5V, $V_{REF(-)}$ = 0V, and T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS[4]			UNIT
				Min	Typ[3]	Max	
t_{CRD}	Conversion time for RD mode		Mode=0, Figure 1		1.6	2.5	µs
t_{ACCO}	Access time (delay from falling edge of $\overline{RD}$ to output valid)		Mode=0, Figure 1		t_{CRD}+20	t_{CRD}+50	ns
t_{CWR-RD}	Conversion time for WR-RD mode		Mode=V_{DD}, t_{WR}=600ns, t_{RD}=600ns; Figures 3a and 3b			1.52	µs
t_{WR}	Write time	Min	Mode=V_{DD}, Figures 3a and 3b[2]	600			ns
		Max				50	µs
t_{RD}	Read time	Min	Mode=V_{DD}, Figures 3a and 3b[2]	600			ns
t_{ACC1}	Access time (delay from falling edge of $\overline{RD}$ t o output valid)		Mode=V_{DD}, t_{RD}<t_I; Figure 3b, C_L=15pF		190	280	ns
			C_L=100pF		210	320	ns
t_{ACC2}	Access time (delay from falling edge of $\overline{RD}$ t o output valid)		Mode=V_{DD}, t_{RD}>t_I; Figure 3a, C_L=15pF		70	120	ns
			C_L=100pF		90	150	ns
t_I	Internal comparison time		Mode=V_{DD}; Figures 2 and 3a, C_L=50pF		800	1300	ns
t_{1H}, t_{0H}	Three-state control (delay from rising edge of $\overline{RD}$ to Hi-Z state)		R_L=1kΩ, C_L=10pF		100	200	ns
$t_{\overline{INTL}}$	Delay from rising edge of $\overline{WR}$ to falling edge of $\overline{INT}$		Mode=V_{DD}, C_L=50pF t_{RD}>t_I; Figure 3a t_{RD}<t_I; Figure 3b		 t_{RD}+200	 t_I t_{RD}+290	 ns ns
$t_{\overline{INTH}}$	Delay from rising edge of $\overline{RD}$ to rising edge of $\overline{INT}$		Figures 1, 3a, and 3b, C_L=50pF		125	225	ns
$t_{\overline{INTHWR}}$	Delay from rising edge of $\overline{WR}$ to rising edge of $\overline{INT}$		Figure 2, C_L=50pF		175	270	ns
t_{RDY}	Delay from $\overline{CS}$ to RDY		Figure 1, C_L=50pF, Mode=0		50	100	ns
t_{ID}	Delay from $\overline{INT}$ to output valid		Figure 2		20	50	ns
t_{RI}	Delay from $\overline{RD}$ to $\overline{INT}$		Mode=V_{DD}, t_{RD}<t_I; Figure 3b		200	290	ns
t_P	Delay from end of conversion to next conversion		Figures 1, 2, 3a, and 3b[2]	500			ns
SR	Slew rate, tracking				0.1		V/µs
C_{VIN}	Analog input capacitance				45		pF
C_{OUT}	Logic output capacitance				5		pF
C_{IN}	Logic input capacitance				5		pF

NOTES:
1. Unadjusted error includes offset, full-scale, and linearity errors.
2. Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified.
3. Typicals are at 25°C and represent most likely parametric norm.
4. Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

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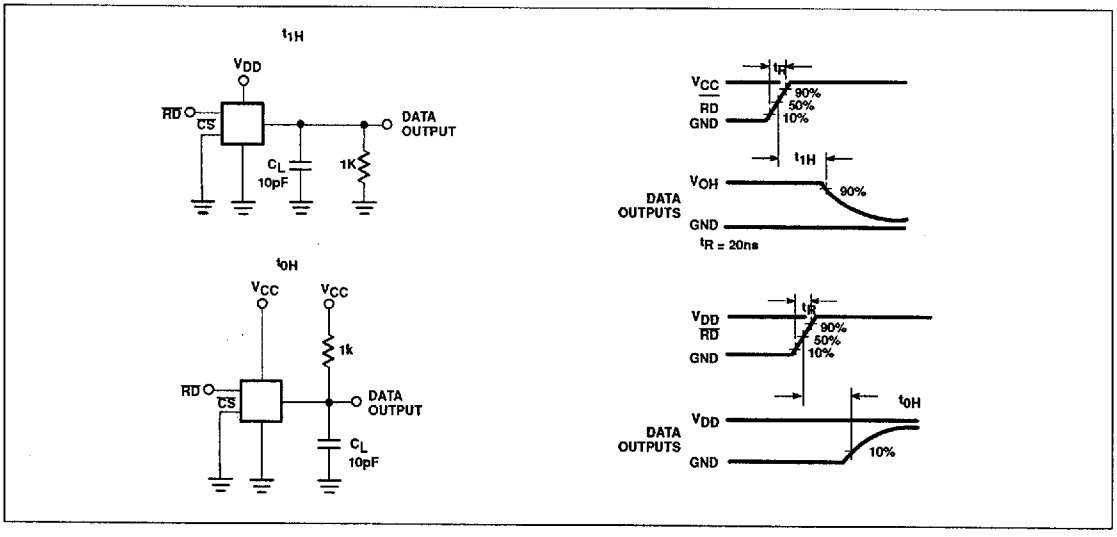
3-STATE TEST CIRCUITS AND WAVEFORMS



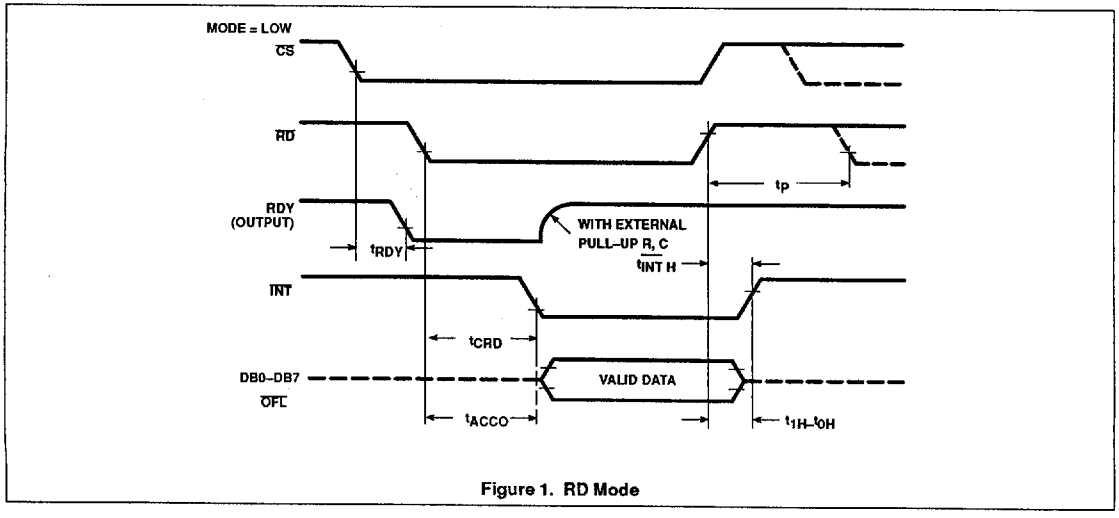


Figure 1. RD Mode

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ADC0820

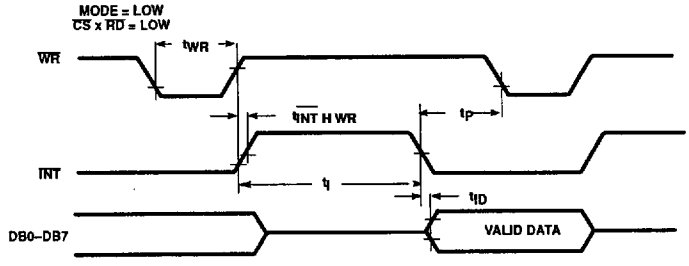
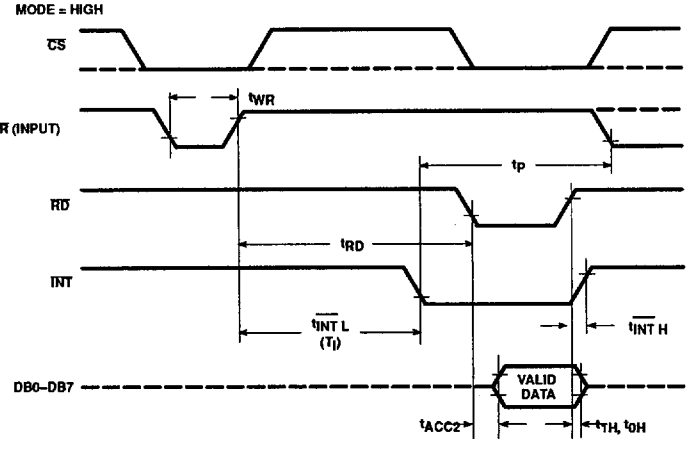
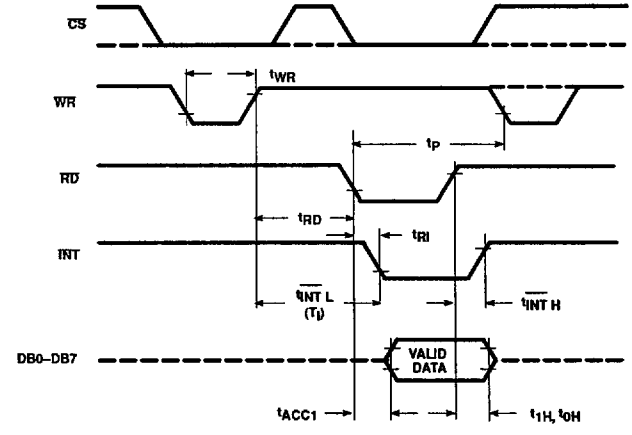


Figure 2. Stand-Alone Mode



a. WR-RD Mode ($t_{RD} > t_I$)



b. WR-RD Mode ($t_{RD} < t_I$)

Figure 3. WR–RD Mode

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ADC0820

FUNCTIONAL DESCRIPTION

General Operation

The ADC0820 uses two 4-bit flash A/D converters to make an 8-bit measurement (Block Diagram). Each flash ADC is made up of 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. To take a full 8-bit reading, one flash conversion is done to provide the 4 most significant data bits (via the MS flash ADC). Driven by the 4 MSBs, an internal DAC recreates an analog approximation of the input voltage. This analog signal is then subtracted from the input, and the difference voltage is converted by a second 4-bit flash ADC (the LS ADC), providing the 4 least significant bits of the output data word.

The internal DAC is actually a subsection of the MS flash converter. This is accomplished by using the same resistor ladder for the A/D as well as for generating the DAC signal. The DAC output is actually the tap on the resistor ladder which most closely approximates the analog input. In addition, the "sampled data" comparators used in the ADC0820 provide the ability to compare the magnitudes of several analog signals simultaneously, without using input summing amplifiers. This is especially useful in the LS flash ADC, where the signal to be converted is an analog difference.

The Sampled-Data Comparator

Each comparator in the ADC0820 consists of a CMOS inverter with a capacitively-coupled input (Figure 4). Analog switches connect the two comparator inputs to the input capacitor (C) and also connect the inverter's input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator, and another for making the comparison.

In the first cycle, one input switch and the inverter's feedback switch (Figure 4a) are closed. In this interval, C is charged to the connected input (V1) less the inverter's bias voltage (V_S, approximately 1.6V). In the second cycle (Figure 4b), these two switches are opened and the other (V2) input's switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter's open loop gain. The inverter's input (V_S') becomes

$$V_S' = V_S + (V2 - V1)\frac{C}{C + C_S}$$

and the output will go High or Low depending on the sign of $V_S'-V_S$.

The actual circuitry used in the ADC0820 is a simple but important expansion of the basic comparator described above. By adding a second capacitor and another set of switches to the input (Figure 5), the scheme can be expanded to make dual differential comparisons. In this circuit, the feedback switch and one input switch on each capacitor (Z switches) are closed in the zeroing cycle. A comparison is then made by connecting the second input on each capacitor (S switches) and opening all of the other switches. The change in voltage at the inverter's input, as a result of the change in charge on each input capacitor, will now depend on both input signal differences.

Architecture

In the ADC0820, 15 comparators are used in the MS and LS 4-bit flash A/D converters. The MS (most significant) flash ADC also has one additional comparator to detect input overrange. These two sets of comparators operate alternately, with one group in its zeroing cycle while the other is comparing.

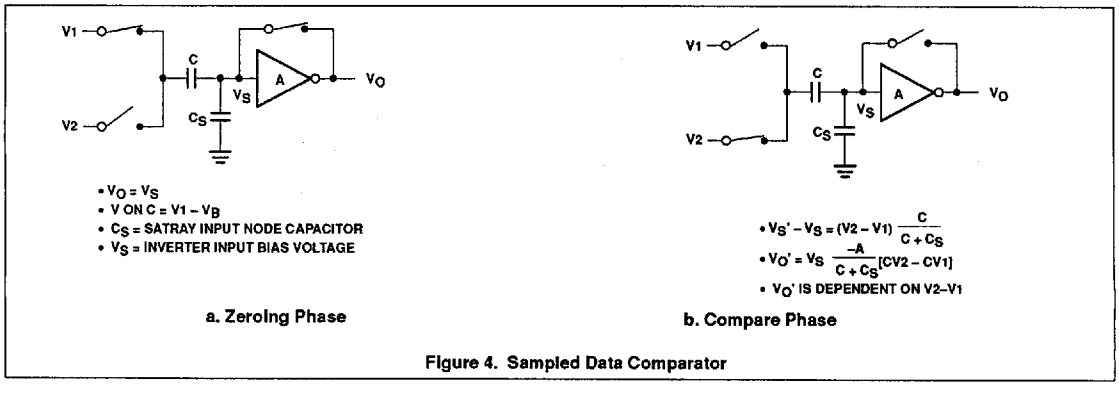

Figure 4. Sampled Data Comparator

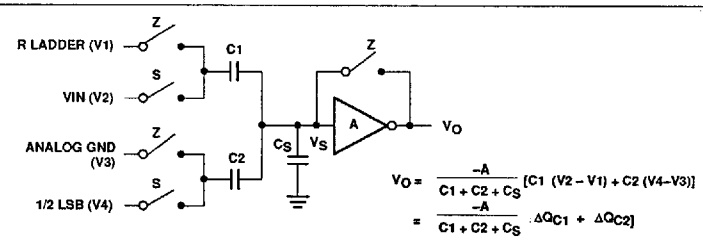

Figure 5. ADC0820 Comparator (From MS Flash ADC)

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To start a conversion in the WR-RD mode, the $\overline{WR}$ line is brought Low. At this instant the MS comparators go from zeroing to comparison mode (Figure 8). When $\overline{WR}$ is returned High after at least 600ns, the output from the first set of comparators (the first flash) is decoded and latched. At this point the two 4-bit converters change modes and the LS (least significant) flash ADC enters its compare cycle. No less than 600ns later, the $\overline{RD}$ line may be pulled Low to latch the lower four data bits and finish the 8-bit conversion. When $\overline{RD}$ goes Low, the flash A/Ds change state once again in preparation for the next conversion.

Figure 8 also outlines how the converter's interface timing relates to its analog input (V_{IN}). In WR-RD mode, V_{IN} is measured while $\overline{WR}$ is Low. In RD mode, sampling occurs during the first 800ns of $\overline{RD}$. Because of the input connections to the ADC0820's LS and MS comparators, the converter has the ability to sample V_{IN} at one instant, despite the fact that two separate 4-bit conversions are being done. More specifically, when $\overline{WR}$ is Low the MS flash is in compare mode (connected to V_{IN}, and the LS flash is in zero mode (also connected to V_{IN}). Therefore both flash ADCs sample V_{IN} at the same time.

Digital Interface

The ADC0820 has two basic interface modes which are selected by strapping the Mode pin High or Low.

RD Mode (Figure 6a)

With the Mode pin grounded, the converter is set to Read mode. In this configuration, a complete conversion is done by pulling $\overline{RD}$ Low until output data appears. An $\overline{INT}$ line is provided which goes Low at the end of the conversion as well as a RDY output which can be used to signal a processor that the converter is busy or can also serve as a system Transfer Acknowledge signal.

When in RD mode, the comparator phases are internally triggered. At the falling edge of $\overline{RD}$, the MS flash converter goes from zero to compare mode and the LS ADC's comparators enter their zero cycle. After 800ns, data from the MS flash is latched and the LS flash ADC enters compare mode. Following another 800ns, the lower four bits are recovered.

WR Then RD Mode (Figures 6b and c)

With the Mode pin tied High, the A/D will be set up for the WR-RD mode. Here, a conversion is started with the $\overline{WR}$ input; however, there are two options for reading the output data which relate to interface timing. If an interrupt-driven scheme is desired, the user can wait for $\overline{INT}$ to go Low

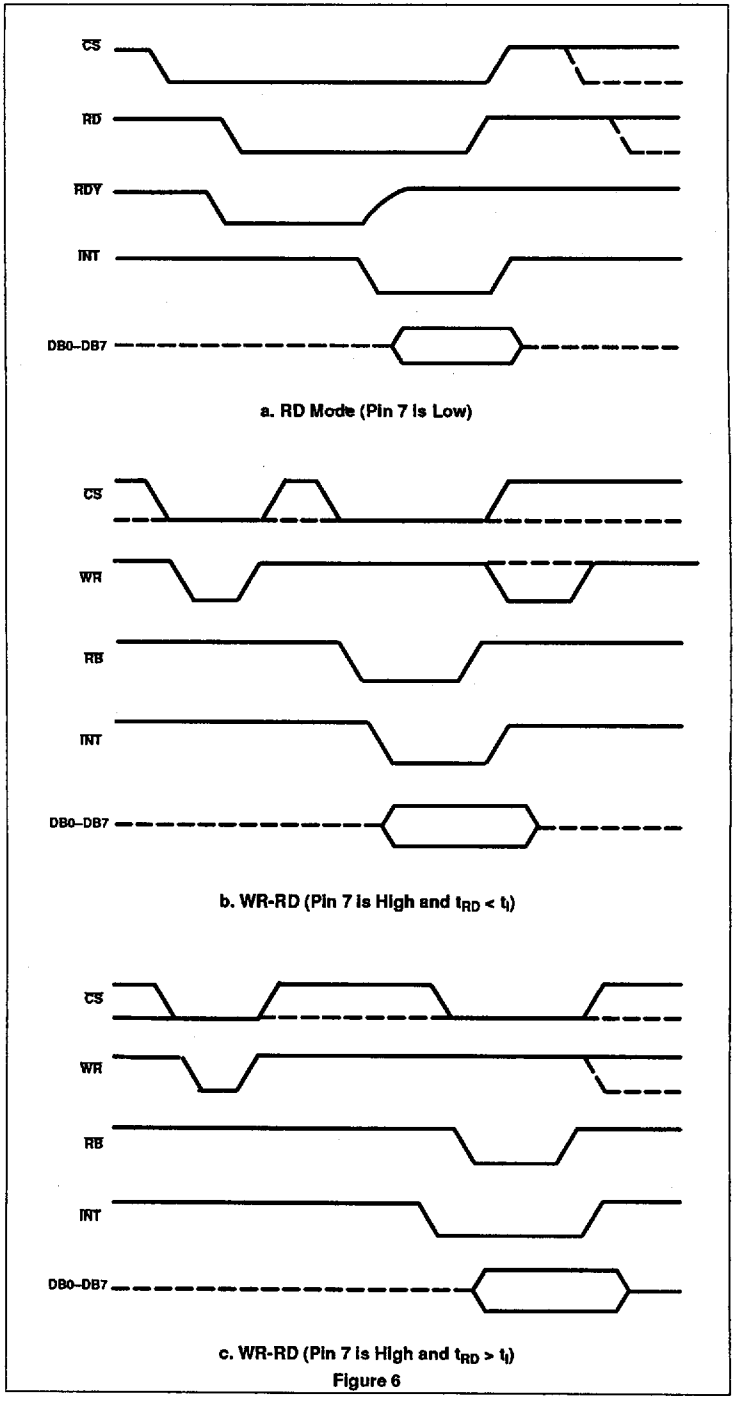


Figure 6

8-Bit, high-speed, μP-compatible A/D converter with track/hold function

before reading the conversion result. $\overline{INT}$ will typically go Low 800ns after $\overline{WR}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{INT}$ and can exercise a Read after only 600ns. If this is done, $\overline{INT}$ will immediately go Low and data will appear at the outputs.

Stand-Alone (Figure 7)
For stand-alone operation in WR-RD mode, $\overline{CS}$ and $\overline{RD}$ can be tied Low and a conversion can be started with $\overline{WR}$. Data will be valid approximately 800ns following $\overline{WR}$'s rising edge.

Other Interface Considerations

In order to maintain conversion accuracy, $\overline{WR}$ has a maximum width spec of 50μs. When the MS flash ADC's sampled data comparators are in comparison mode ($\overline{WR}$ is Low), the input capacitors (C, Figure 5) must hold their charge. Switch leakage can cause errors if the comparator is left in this phase for too long.

Since the MS flash ADC enters its zeroing phase at the end of a conversion, a new conversion cannot be started until this phase is complete. The minimum spec for this time is 500ns (t_P in Figure 1, 2, 3a, and 3b).

ANALOG CONSIDERATIONS

Reference and Input

The two V_{REF} inputs of the ADC0820 are fully differential and define the zero- to full-scale input range of the A/D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing $V_{REF}(V_{REF}=V_{REF}(+) - V_{REF}(-))$ to less than 5V, the sensitivity of the converter can be increased (i.e., if V_{REF}=2V, then 1 LSB=7.8mV). The input/reference arrangement also facilitates ratiometric operation and, in many cases, the chip power supply can be used for transducer power as well as the V_{REF} source.

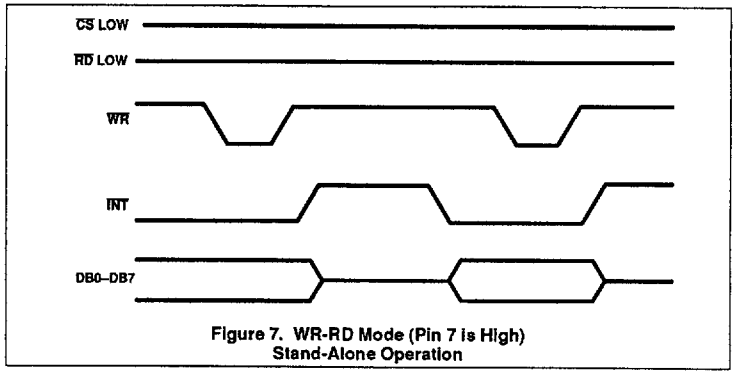


Figure 7. WR-RD Mode (Pin 7 is High) Stand-Alone Operation

This reference flexibility lets the input span not only be varied, but also offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes. Though V_{IN} is not itself differential, the reference design affords nearly differential-input capability for most measurement applications. Figure 9 shows some of the configurations that are possible.

Input Current

Due to the unique conversion techniques employed by the ADC0820, the analog input behaves somewhat differently than in conventional devices. The A/D's sampled data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the ADC0820 is shown in Figure 10a. When a conversion starts ($\overline{WR}$ Low, WR-RD mode), all input switches close, connecting V_{IN} to 31 1pF capacitors. Although the two 4-bit flash circuits are not both in their compare cycle at the same time, V_{IN} still sees all input capacitors at once. This is because the MS flash converter is connected to the input during its compare interval and the LS flash is connected to the input during its zeroing phase. In other words, the LS ADC uses V_{IN} as its zero-phase input.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 5kΩ to 10kΩ). In addition, about 12pF of input stray capacitance must also be charged. For large source resistances, the analog input can be modeled as an RC network as shown in Figure 10b. As R_S increases, it will take longer for the input capacitance to charge.

In RD mode, the input switches are closed for approximately 800ns at the start of the conversion. In WR-RD mode, the time that the switches are closed to allow this charging is the time that $\overline{WR}$ is Low. Since other factors force this time to be at least 600ns, input time constants of 100ns can be accommodated without special consideration. Typical total input capacitance values of 45pF allow R_S to be 1.5kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

Input Filtering

It should be made clear that transients in the analog input signal, caused by charging current flowing into V_{IN}, will not degrade the A/D's performance in most cases. In effect, the ADC0820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is Low, so at least 600ns will be provided to charge the ADC's input capacitance. It is

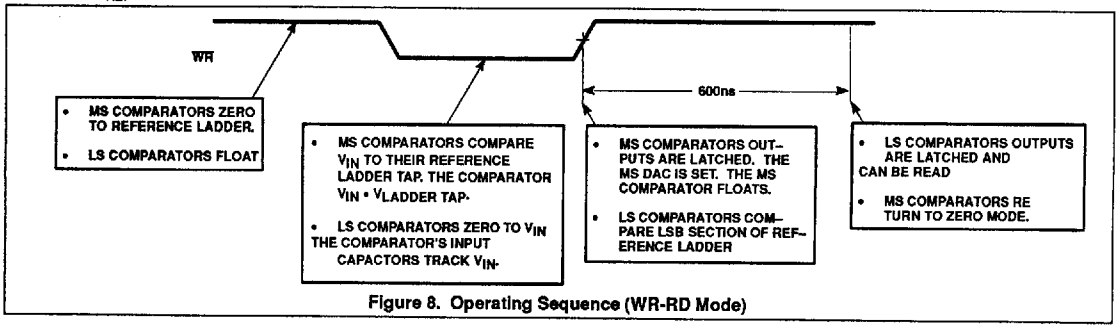
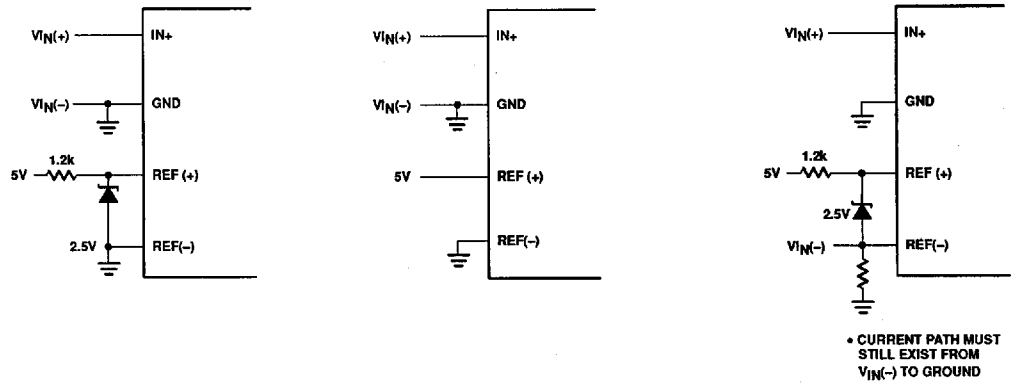


Figure 8. Operating Sequence (WR-RD Mode)

8-Bit, high-speed, μP-compatible A/D converter with track/hold function



a. External Reference 2.5V Full-Scale b. Power Supply as Reference c. Input not Referred to GND

Figure 9. Analog Input Options

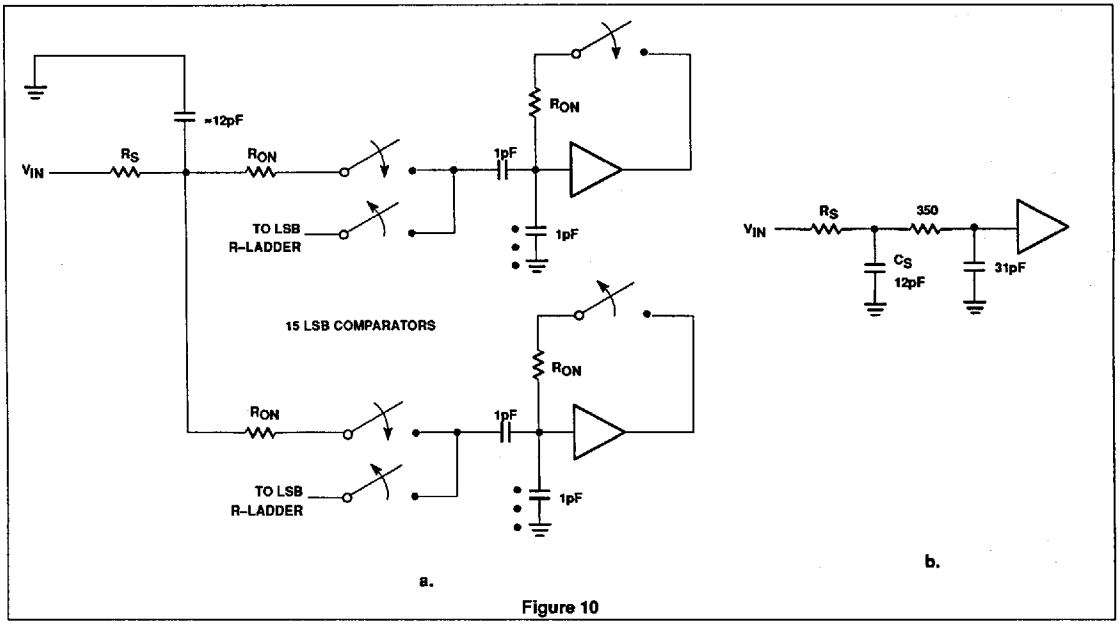


Figure 10

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therefore not necessary to filter out these transients by putting an external cap on the V_{IN} terminal, if an input amplifier that can settle within 600ns is used to drive the input. The NE530 is a suitable op amp for driving the input of the ADC0820.

Inherent Sample-Hold

Another benefit of the ADC0820's input mechanism is its ability to measure a variety of high-speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain at least LSB stable throughout the conversion process if full accuracy is to be maintained. Consequently, for many high-speed signals, this signal must be externally sampled, and held stationary during the conversion.

Sampled data comparators, by nature of their input switching, already accomplish this function to a large degree (Section 1.2). Although the conversion time for the ADC0820 is 1.5µs, the time through which V_{IN} must be 1/2LSB stable is much smaller. Since the MS flash ADC uses V_{IN} as its "compare" input and the LS ADC uses V_{IN} as its "zero" input, the ADC0820 only "samples" V_{IN} when $\overline{WR}$ is Low. Even though the two flashes are not done simultaneously, the analog signal is measured at one instant. The value of V_{IN} approximately 100ns after the rising edge of $\overline{WR}$ (100ns due to internal logic propagation delay) will be the measured value.

Input signals with slew rates typically below 100mV/µs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the ADC0820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. An SAR type converter with a conversion time as fast as 1µs would still not be able to measure a 5V, 1kHz sine wave without the aid of an external sample-and-hold. The ADC0820, with no such help, can typically measure 5V, 7kHz waveforms.

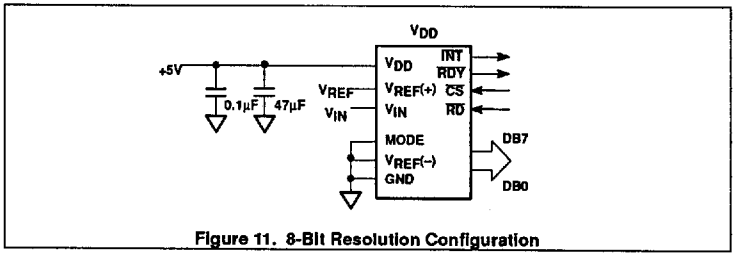

Figure 11. 8-Bit Resolution Configuration

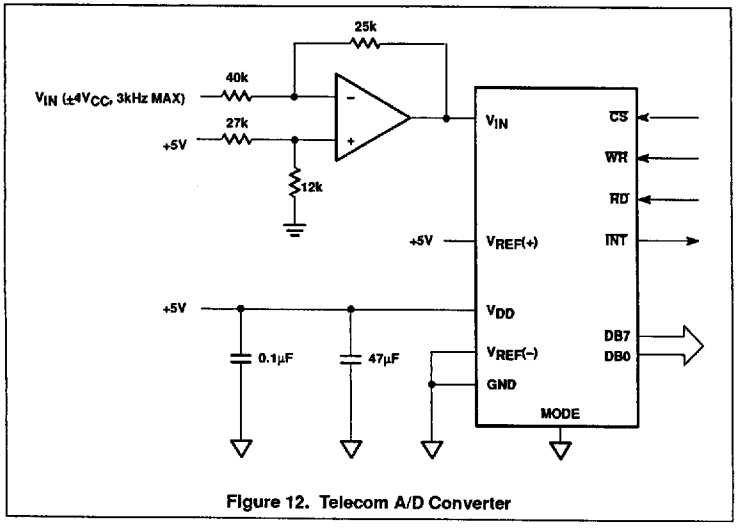

Figure 12. Telecom A/D Converter

8-Bit, high-speed, μP-compatible A/D converter with track/hold function

ADC0820

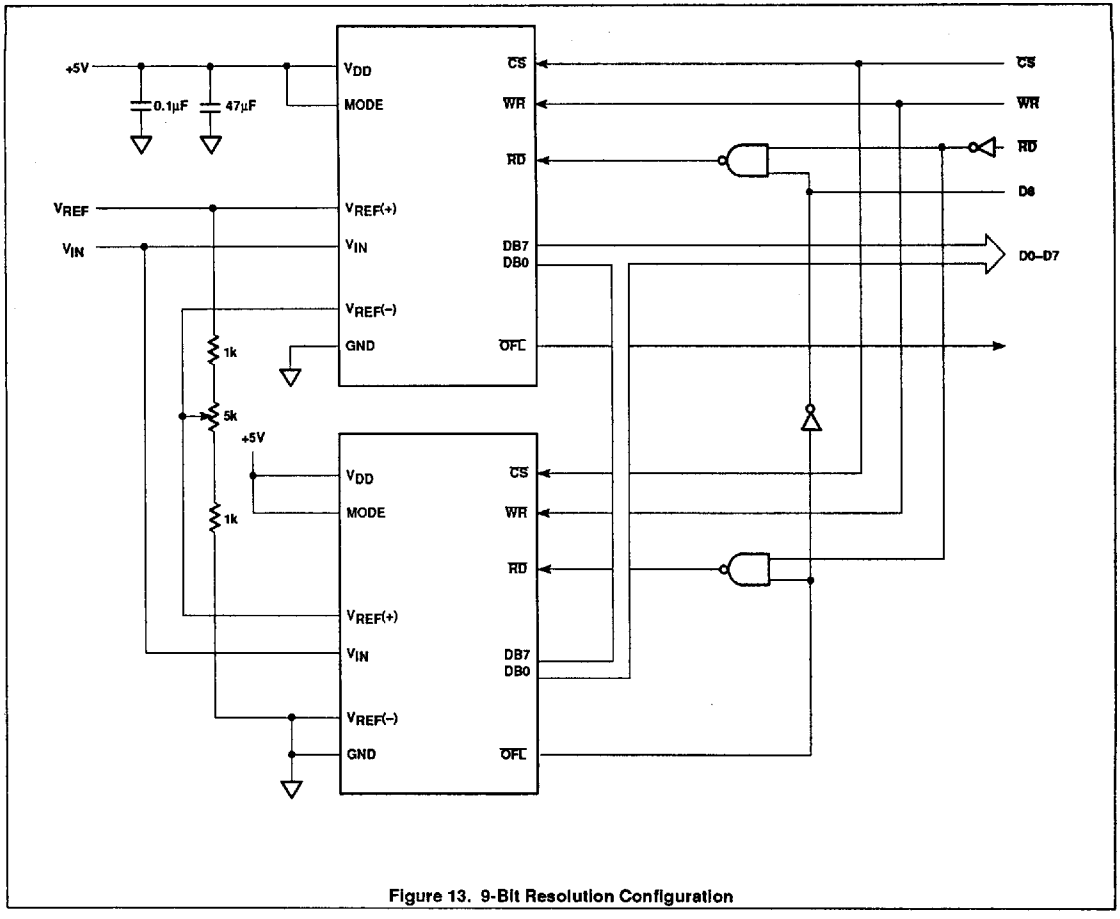

Figure 13. 9-Bit Resolution Configuration