National Semiconductor

November 1989

ADC0830
μP Compatible 8-Bit A/D with 21 Channel MUX/Digital Inputs

General Description

The ADC0830 data acquisition component is a monolithic, ion-implanted, low threshold metal gate CMOS device. It contains a *16 channel analog multiplexer; an 8-bit ratiometric analog to digital converter; a 9 channel digital input register; a 3 channel peripheral I/O port; an 8 channel bus I/O port;* and all logic for software configuration, channel selection, conversion control, bus interface and maskable interrupt compatibility.

The device contains *three 16-bit registers* which are accessed via double byte instructions. The *control register* is a write only register which controls the start of a new conversion, selects the channel to be converted, configures the 3-bit I/O port as input or output, provides information for the 3-bit output register, and controls the Interrupt Enable bit. (See Word Format Description.)

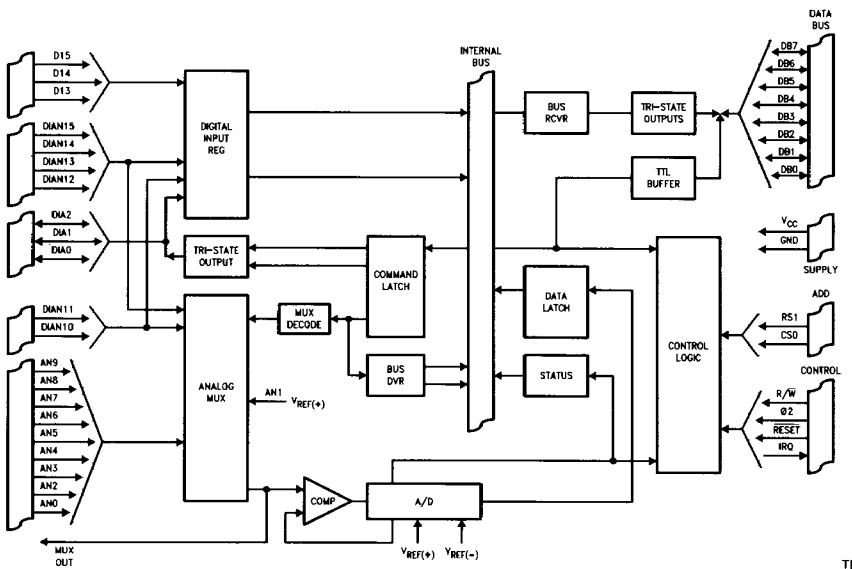
The *conversion results register* is a read only register which contains the current status and most recent conversion results. The *discrete input register* is also a read only register which contains the status of the 3-bit I/O port, 3 discrete inputs, the 4 address bits of the selected channel, and the 6 discrete inputs which are connected to the analog multiplexer.

The ADC0830 requires no external components, no calibration and features an absolute accuracy of 1 LSB, including quantizing error. The design has been optimized by offering high speed, high accuracy, minimal temperature dependence, excellent long term accuracy and repeatability, consumes minimal power and is completely compatible with the MC6800 microprocessor family.

Features

- No external components required
- No calibration or adjustments
- Total unadjusted error ≤ ±1/2 LSB
- Guaranteed monotonicity
- Conversion time 300 μs
- Complete MC6800 compatibility
- Single 5V supply
- Low power consumption
- TTL compatible

Block Diagram



TL/H/10600–1

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RRD-B20M119/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) $-0.3V$ to $+6.5V$

Voltage at Any Pin (V_{IN}) $-0.3V$ to $V_{CC}+0.3V$ or $6.5V$ Whichever is Less

Input Current at Any Input Pin (I_{IN}) $\leq \pm 5$ mA
Not to Exceed ± 20 mA Total for the Package.*

Operating Temperature (T_A) $-40°C$ to $+85°C$

*This current is conducted by the input protection circuit.

Storage Temperature (T_{STG}) $-55°C$ to $+150°C$

Lead Temperature (T_{LEAD}) (Soldering, 10 Seconds) 300°C

Package Dissipation (D_{PKG}) (at 85°C) 500 mW

Maximum Thermal Resistance (θ_{JA}) 90°C/W

Reference Isolation (R_{ISO})
between V_{CC} and V_{REF+} ≥ 100 kΩ
between GND and V_{REF-} ≥ 100 kΩ

Maximum Junction Temperature (T_J) 130°C

DC Electrical Characteristics $4.75V \leq V_{CC} \leq 5.5V$, $-40°C \leq T_A \leq 85°C$ (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage (D0–D7, DIA0–DIA2)	$I_{IN(1)} \leq +10\ \mu A$	2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage (D0–D7, DIA0–DIA2)	$I_{IN(0)} \leq -10\ \mu A$			0.8	V
$V_{IN(1)}$	Logical "1" Input Voltage (Ø2)	$I_{IN(1)} \leq +10\ \mu A$	$V_{CC}-0.6$			V
$V_{IN(0)}$	Logical "0" Input Voltage (Ø2)	$I_{IN(0)} \geq -10\ \mu A$			0.4	V
$V_{IN(1)}$	Logical "1" Input Voltage (D13–D15, DIAN10–DIAN15, R/$\overline{W}$, RS1, $\overline{RESET}$, CSO)	$I_{IN(1)} \leq +1\ \mu A$	2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage (D13–D15, DIAN10–DIAN15, R/$\overline{W}$, RS1, $\overline{RESET}$, CSO)	$I_{IN(0)} \geq -1\ \mu A$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage (D0–D7)	$I_{OUT} = -1.6$ mA	2.4	3.0		V
$V_{OUT(0)}$	Logical "0" Output Voltage (D0–D7)	$I_{OUT} = 1.6$ mA		0.2	0.4	V
$V_{OUT(1)}$	Logical "1" Output Voltage (DIA0–DIA2)	$I_{OUT} = -190\ \mu A$	$V_{CC}-0.4$	$V_{CC}-0.2$		V
$V_{OUT(0)}$	Logical "0" Output Voltage (DIA0–DIA2)	$I_{OUT} = 0.975$ mA		0.2	0.4	V
$V_{OUT(0)}$	Logical "0" Output Voltage (IRQ Output)	$I_{OUT} = -1.6$ mA		0.2	0.4	V
$I_{OUT(1)}$	Logical "1" Output Current (IRQ Output)	$V_{OUT} = V_{CC}$		1	10	μA
I_{CC}	Supply Current	$f_c = 1.048$ MHz		3	10	mA
I_{OUT}	TRI-STATE Output Current	$V_{OUT} = V_{CC}$ $V_{OUT} = 0V$		1 −1	10 −10	μA μA
V_{CLAMP+}	Voltage Clamp +	$I+ = 1$ mA $V_{CC} = 0V$			−2.0	V
V_{CLAMP-}	Voltage Clamp −	$I- = -1$ mA $V_{CC} = 5V$			−4.0	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperatures Range" they are not meant to imply that the devices should be operated at these limits. The Table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to GND unless otherwise specified.

Analog Multiplexer $4.75V \le V_{CC} \le 5.5V$, $-40°C \le T_A \le 85°C$

Symbol	Parameter	Conditions		Typ	Max	Units
R_{ON}	Analog Multiplexer ON Resistance			1.5	4	kΩ
I_{MUX}	Multiplexer Leakage Current for Any ON Channel	All Other Mux Channels at V_{CC}	Ø2 at GND	±50	±400	nA

Converter Section $4.75V \le V_{CC} \le 5.5V$, $-40°C \le T_A \le 85°C$, $4.6V \le V_{REF(+)} \le V_{CC}$

Parameter	Conditions	Min	Typ	Max	Units
Resolution		8			Bits
Non-Linearity*	(Note 3)		±¼	±½	LSB
Zero Error*	(Note 4)		±¼	±½	LSB
Full-Scale Error*	(Note 5)		±¼	±½	LSB
Total Unadjusted Error*	(Note 6)		±¼	±½	LSB
Quantization Error*	(Note 7)		±¼	±½	LSB
Absolute Accuracy	(Note 8)		±¾	±1	LSB
Converter Input Current	(Note 9)		±250	±500	nA
Converter Input Voltage Range		−0.3	V_{CC}	V_{CC} + 0.3	V

*Not directly tested but functionally guaranteed by absolute accuracy check.

Note 3: Non-linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic *(Figure 1)*.

Note 4: Zero error is the difference between the output of an ideal and the actual A/D for zero input voltage, *(Figure 1)*.

Note 5: Full-scale error is the difference between the output of an ideal and the actual A/D for full-scale input voltage *(Figure 1)*.

Note 6: Total unadjusted error is the maximum sum of non-linearity, zero and full-scale errors *(Figure 2)*.

Note 7: Quantization error is the ±½ LSB uncertainty caused by the converter's finite resolution *(Figure 2)*.

Note 8: Absolute accuracy describes the difference between the actual input voltage and the full scale weighted equivalent of the binary output code; included are quantizing and all other errors. Although rarely provided on data sheets, it is the best indication of a converter's true performance *(Figure 2)*.

Note 9: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directlly with clock frequency *(Figure 9)* and has little temperature dependence. Converter input current is the sum of comparator input current and multiplexer leakage current.

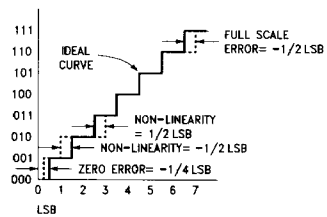

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FIGURE 1. 3-Bit A/D Transfer Curve

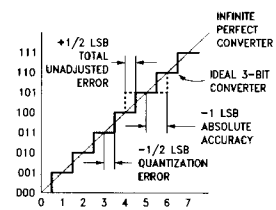

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FIGURE 2. 3-Bit A/D Absolute Accuracy Curve

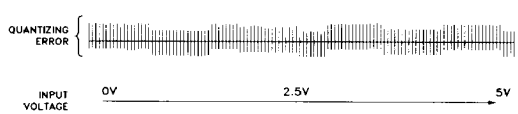

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FIGURE 3. Typical Error Curve
(See Application Note AN-179 for Details)

Ladder Section $4.75V \le V_{CC} \le 5.5V$, $-40°C \le T_A \le 85°C$

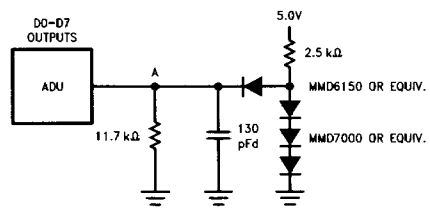
Symbol	Parameter	Min	Typ	Max	Units
R_{LAD}	Resistance Between $V_{REF(+)}$ and $V_{REF(-)}$	1.0	4.5		kΩ
$V_{REF(+)}$	Voltage, Top of Ladder	4.6	V_{CC}	V_{CC}	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	0	0	0.1	V

AC Electrical Characteristics $4.75V \le V_{CC} \le 5.5V$, $-40°C \le T_A \le +85°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_c	Clock Frequency		0.1	1.048	1.1	MHz
t_C	Conversion Time	f_c = 1.048 MHz		285	300	μs
t_{CA}	Channel Acquisition Time	f_c = 1.048 MHz		29	30	μs
t_{RB}	Data Bus Rise Time	*Figure 4a* *Figure 4c*		75 150	150 300	ns ns
t_{FB}	Data Bus Fall Time	*Figure 4b* *Figure 4d*		75 150	150 300	ns ns
t_{RD}	DIA Output Rise Time	*Figure 5a* *Figure 5c*		250 500	500 1000	ns ns
t_{FD}	DIA Output Fall Time	*Figure 5b* *Figure 5d*		250 500	500 1000	ns ns
t_{FI}	IRQ Output Fall Time	*Figure 6*		250	500	ns
C_{IN}	Input Capacitance D0–D7 Inputs All Other Inputs			 15 7	 30 15	 pF pF

CPU Timing Interface is covered by the Timing Diagram for CPU Bus Signal Interface Standards.

Rise and Fall Times are not directly tested. Functionality guaranteed by propagation delay test.



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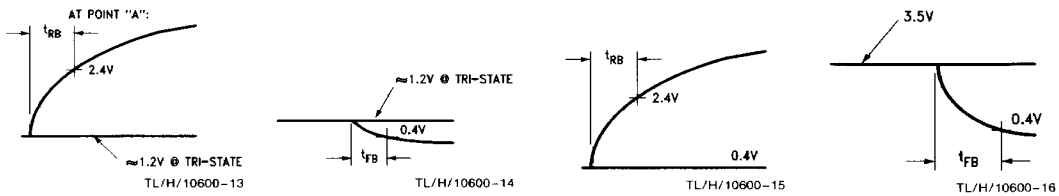
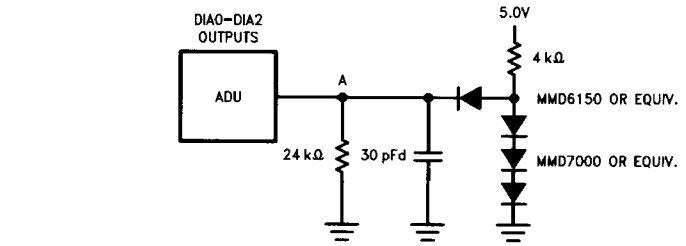


FIGURE 4. Data Bus Waveforms



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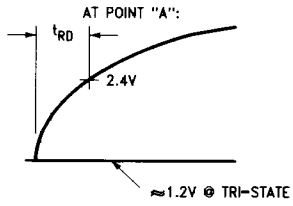

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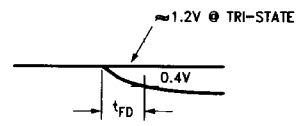
a



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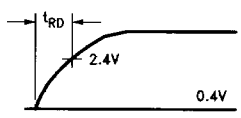
b



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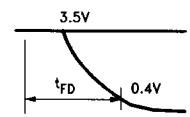
c



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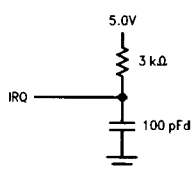
d

FIGURE 5. Discrete Outputs Waveforms



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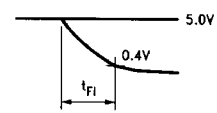

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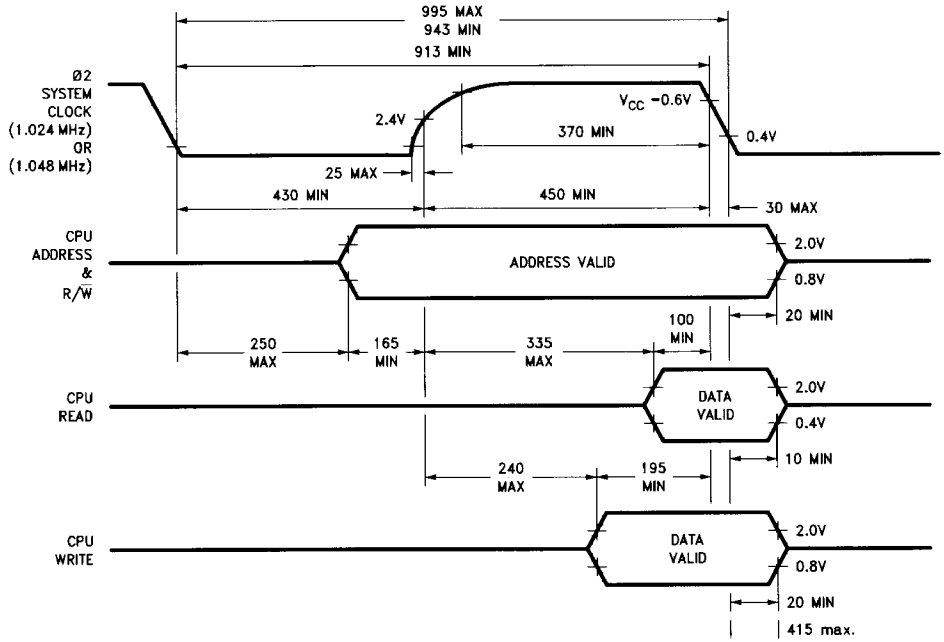
FIGURE 6. IRQ Waveform

Interface Timing Diagram



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Notes:

1) All times are in nanoseconds.

2) All timing transitions are measured from the levels specified in Notes 4 and 5 unless otherwise specified.

3) 02 CLK input levels are shown for the CPU.

4) All input levels are 0.8/2.0V (unless otherwise specified).

5) All output levels are 0.4/2.4V (unless otherwise specified).

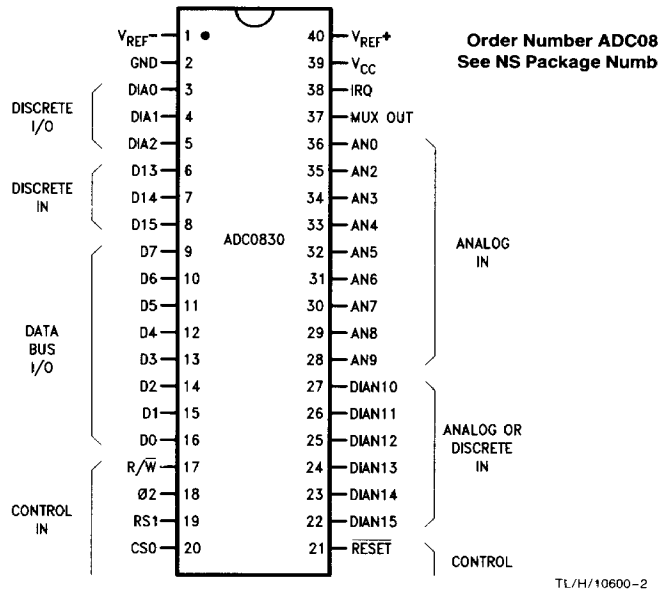
6) 02 CLK loading is 150 pF plus one TTL load.

7) Address bus loading is 90 pF plus one TTL load.

8) Data bus loading is 130 pF plus one TTL load.

Connection Diagram

Dual-In-Line Package



Order Number ADC0830CCN
See NS Package Number N40A

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Top View

Control Logic

The Control Logic interprets the microprocessor control signals and decodes these signals to perform the actual functions of selecting, reading, writing, enabling the outputs, etc.

State Descriptions

There are three internal states within the A/D converter) the NO OP state; the sample state; and the converting state.

The NO OP state is a stable state since the external stimulus (e.g., start conversion signal) is needed for a state transition.

The first transient state is sampling the input. The first 30 μs of the conversion are used for acquiring the channel; this settling time allows any transients to decay before conversion begins. The second transient state is the actual conversion. The conversion is completed by 256 μs and the conversion results register is updated. The converter then returns to the stable NO OP state awaiting further instructions.

The device has no comparator bias current and draws minimal power during the NO OP state.

Initialization

The device is initialized by an active low on $\overline{\text{RESET}}$. All outputs are initialized to the inactive state, the DIA0–DIA2 is initialized as inputs, the interrupt enable bit is reset, and the converter placed in its NO OP state. The data register is not affected by $\overline{\text{RESET}}$. System TRI-STATE® outputs are initialized to the high impedance state.

Conversion Control

The program normally initiates a conversion cycle with a double write command. (See control word format.) The control word selects a channel, configures the peripheral I/O, provides peripheral data information, and controls the interrupt enable bit. The conversion is initiated by setting the SC bit in the control word high.

The converter then resets the start conversion bit and begins the conversion cycle.

When the conversion is complete and the new conversion results transferred to the data register, the status bit is set and an interrupt requested if the interrupt enable bit is set.

The status bit is not reset when the conversion results are read. A full double byte write into the control word will reset the status bit, or a low level at master $\overline{\text{RESET}}$.

If a new conversion command occurs during a conversion, the conversion is aborted and a new channel acquisition phase will immediately begin.

The IRQ interrupt is composed of the status and Interrupt Enable bits. The master $\overline{\text{RESET}}$ signal forces both bits low, and end of conversion posts the status bit high. The interrupt enable bit is written by the control word.

Control Structure

The control logic continually monitors the control bus waiting for CSO to go low and Ø2 to go high. When this condition occurs, the internal decoder, which has already selected the proper function, activates.

The byte counter will always select the MSH of any word first, and the LSH second. Single byte instructions will always access the MSH portion of any word. After a single byte instruction the byte counter will return to the MSH portion of a word when CSO is high for a full clock cycle. A single byte instruction is especially useful for reading the status bit during a polled interrupt.

Control Word Format

← MSH Word →								← LSH Word →							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X	IE	X	X	X	X	X	SC	MA	DIA2	DIA1	DIA0	A3	A2	A1	A0

X: Don't Care

SC: Start Conversion
1 = Start new conversion
0 = Do not start new conversion

IE: Interrupt Enable
1 = IRQ is enabled
0 = IRQ is masked

A3–A0: Channel Address

Hex Value:	Definition:
0	Select AN0
1	Select $V_{REF\,(+)}$
2–F	Select Channels 2–15

DIA2–DIA0: Discrete Outputs

MA: Mode Select
1 = DIA2–DIA0 Discrete Outputs
0 = DIA2–DIA0 Discrete Inputs

Conversion Results Word Format

← MSH Word →								← LSH Word →							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
S	0	0	0	0	0	0	0	C7	C6	C5	C4	C3	C2	C1	C0

S: Status
1 = Data is Valid
0 = Data is Not Valid

C_7–C_0: 8-Bit Converted Result

Discrete Input Word Format

← MSH Word →								← LSH Word →							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
DIAN 15	DIAN 14	DIAN 13	DIAN 12	DIAN 11	DIAN 10	A3	A2	A1	A0	DI 5	DI 4	DI 3	DIA 2	DIA 1	DIA 0

DIA2–DIA0: Status of DIA2–DIA0

A3–A0: Status of channel address

DIAN15–DIAN10: Status of DIAN15–DIAN10
Interpreted as discrete inputs

DI3–DI5: Status of DI3–DI5

ADU Address Selection

CSO	R/$\overline{W}$	RS1	Description
1	X	X	Do Not Respond
0	0	0	Write NO OP
0	0	1	Write Control Word
0	1	0	Read Conversion Results
0	1	1	Read Discrete Inputs

Note: All words are transferred as two 8-bit bytes, MSH transferred first, LSH tranferred second.

Analog to Digital Converter

The heart of the ADC0830 is the A/D converter. The converter is composed of three major sections: the successive approximation register (SAR); the 256R ladder and analog decoder; and the chopper stabilized comparator.

Successive Approximation

The analog signal at the A/D input is compared 8 times to various ladder voltages to determine which of the 256 voltages in the ladder most closely approximates the input voltage. This stochastic technique is accomplished by converging on the proper tap in the ladder by simple iterative convergence. There are nine posting registers in the SAR which contain the position of the bit being tested and 8 latching registers which remember if the comparison was high or low. Starting with the MSB and continuing downward, each bit is set high by the posting register. The analog tree decoder selects the corresponding tap in the ladder and the A/D input is compared to that voltage. If the comparison is positive, the latch remains set, so higher voltages in the ladder are checked next. If the comparison is negative, the bit is reset so lower ladder voltages are sought.

After all 8 comparisons are made, the contents of the latching register are transferred to a data register, thus the A/D can perform a new conversion while the previous results remain available.

256R Ladder

The ladder is a very accurate voltage divider which divides the reference voltage into 256 equal steps. Special consideration was given to the ladder terminations at each end, and also the center, to ensure consistent and accurate voltage steps. The use of a 256R ladder guarantees monotonicity since only a single voltage gradient across the ladder exists. Shorted or unequal resistors in the ladder may cause non-uniform steps but cannot cause a nonmonotonic response so often fatal in closed loop system applications (See *Figure 7*).

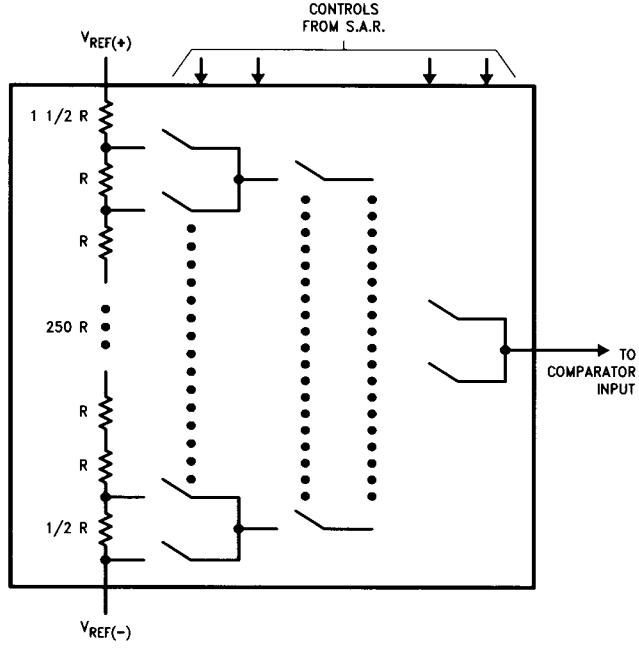

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FIGURE 7. Resistor Ladder and Switch Tree

Actually, of the 256 resistors in the ladder, 254 have the same value while the end point resistors are equal to 1½R and ½R. This ensures the system output characteristic is symmetrical with the zero and full scale points of its input to output, or transfer curve.

The tree decoder routes the 256 voltages from the ladder to a single point at the comparator input. This allows comparisons between the A/D input and any voltage the SAR directs the decoder to route to the comparator.

Since the ladder is dependent upon only the matching of resistors, the voltages it generates are very stable with temperature and have excellent repeatability and long term drift.

Analog Multiplexer

The analog multiplexer selects one of sixteen channels and directs them to the input of the A/D converter. The multiplexer was designed to minimize the effects of leakage currents and multiplexer output capacitance.

Special input protection is used to prevent damage from static voltages or voltages exceeding the specified range from −0.3V to V_{CC} + 0.3V. However, normal precautions are recommended to avoid such situations whenever possible.

Discrete Inputs

The ADC0830 has 12 digital inputs to sense TTL voltage levels. Six of these inputs (DIAN10–DIAN15) are connected to the analog multiplexer. Care must be taken when these inputs are interpreted since TTL levels may not always be present. Three digital inputs (DIA0–DIA2) are connected to three TRI-STATE outputs (DIA0–DIA2). When the mode select (BIT 7, LSH, control word), is low, the three outputs are put in TRI-STATE so DIA0–DIA2 act as inputs. When the mode select bit is high the TRI-STATE outputs are active and the status of the outputs is read back into the ADC0830. Three more digital inputs D13–D15 are dedicated to sensing TTL levels exclusively.

The six digital inputs (DIA0–DIA2, DI13–DI15), not connected to the MUX should be used for signals with AC components since transients on the multiplexer inputs may have some effect on accuracy.

Bus Interface

The ADC0830 communicates to the microprocessor through an 8-bit I/O port. The I/O port is composed of a TTL to CMOS buffer and a TRI-STATE output driver.

The TTL to CMOS Buffer translates the TTL voltage levels into CMOS levels very rapidly and is quite stable with supply and temperature. The buffer has a small amount of hysteresis (about 100 mV) to improve both noise immunity and internal rise and fall times.

The TRI-STATE bus driver is a bipolar and N-channel pair that easily drive the bus capacitance. Since the bus drivers collectively can sink or source a quarter of an amp total, a non-overlap circuit is used which guarantees that only one of the two drive transistors is on at a time.

Since this output drives the bus capacitance, even the non-overlapping circuit cannot prevent noise on V_{CC}. The amount of noise depends on the V_{CC} current used to charge the bus capacitance.

The external filter capacitor on V_{CC} provides some of the transient current while the bus is being driven. A capacitor with good AC characteristics and low series resistance is a good choice to prevent V_{CC} transients from affecting accuracy.

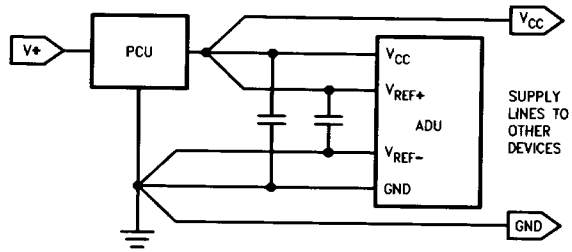
Chopper Stabilized Comparator

Probably the most important section of the A/D converter is the comparator since the comparator's offset voltage and stability determine the converter's ultimate accuracy. The low voltage offset of the chopper-stabilized comparator of this converter optimizes performance by minimizing temperature dependent input offset errors as well as drift.

The DC signal appearing at the amplifier input is converted to an AC signal, amplified by an AC amplifier and restored to a DC signal. The drift of the comparator is minimized since the drift signal is a DC component blocked by the AC amplifier.

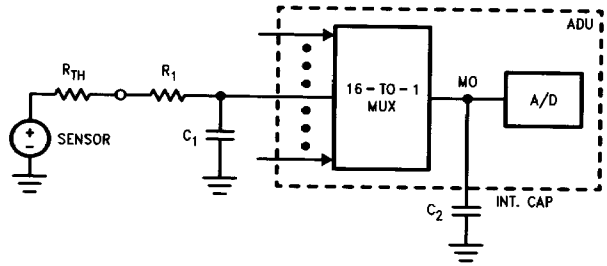
The comparator has very high input impedance to DC voltages since it looks like a capacitor. Because the comparator, is chopping the DC voltages at the input, the difference between the A/D input voltage and ladder voltage appears on the comparator's input capacitor. The input voltage difference, chopping frequency, and comparator input capacitor causes a CVF current. The CVF current is a small bias current which will not produce any error when the A/D input is connected to a low impedance voltage source. If the voltage source has an output impedance of less than 10k, the error is still insignificant since the bias current exponentially decays.

Adding a capacitor to the input of the comparator integrates the exponential charging current, converting it into DC bias current (see *Figure 9*). Two main considerations on the integration capacitor are charge sharing with a filter capacitor and settling time. (See charge sharing section.)



TL/H/10600–8

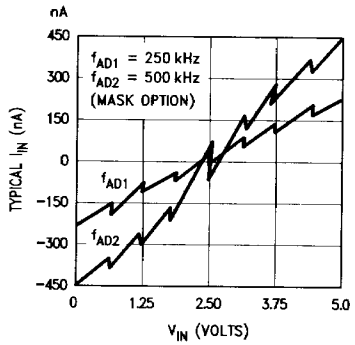
a. Recommended Supply



TL/H/10600–9

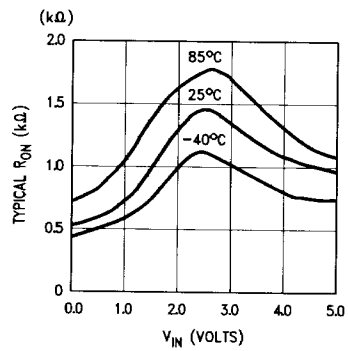
b. Recommended Integration Capacitor

FIGURE 8. Noise Immunity Analysis



TL/H/10600–10

FIGURE 9. Comparator I_{IN} vs V_{IN} (V_{CC} = V_{REF} = 5V, f_C = 1.048 MHz)



TL/H/10600–11

FIGURE 10. Multiplexer R_{ON} vs V_{IN} (V_{CC} = V_{REF} = 5V)

Operation

To utilize the ADC0830 to its fullest extent, several aspects of its design deserve special consideration.

Noise Immunity

Classic communications theory defines noise as any unwanted signal. Immunity from these signals is accomplished by proper design consideration in three areas:

1. Limit noise generation
2. Provide isolation to prevent noise transmission
3. Reduce the effects of noise.

Circuit design in each of three areas provides optimal noise immunity. To limit internal noise generation, the non-overlap circuit on the bus drivers reduces current spikes on V_{CC}. Isolation from supply noise is obtained by providing a separate analog V_{CC} and ground paths. Electrostatic isolation is used around the internal capacitors, the ladder is isolated from substrate current.

The effects of supply noise are reduced by strobing the comparator output so that noise has no effect during most of the conversion cycle.

However, several recommendations are in order to obtain maximum performance:

1. Do not read or write into the device while a conversion is being performed.
2. If the status bit must be checked during a conversion, use a single byte read to reduce generated noise.
3. Provide adequate supply filtering.
4. Provide single point ground and supply separate from other digital devices. (See *Figure 8a* .)

Charge Sharing

The analog multiplexer brings all sixteen channels to a common point called Integration Capacitor (Int. Cap.). A capacitor at this point is not required; in fact, the multiplexer is designed to have very low output capacitance. There are several considerations involved when an external capacitor is placed here (see *Figure 8b*).

If no filter capacitor exists (i.e., C1 = 0) the value of C2, the integrating capacitor, is determined by the RC time constant at the input. The R is $R_{TH} + R_{MUX}$, the C is C2 and C_{MUX}. Since the channel acquisition time is 30 μs and at least 8 time constants are needed for proper settling before conversion begins, the equation for C2 is:

$$8\ RC = 30\ \mu s$$

$$8[(R_{TH} + R1) + R_{MUX}].(C2 + C_{MUX}) = 30\ \mu s$$

$$C_2 = \frac{30\ \mu s}{8[(R_{TH} + R1) + R_{MUX}]} - C_{MUX}$$

Since

$$R_{TH} + R1 = 10k,\ R_{MUX} = 4k,\ C_{MUX} = 15\ pF$$

$$C2 = \frac{30\ \mu s}{8(10k + 4k)} - 15\ pF = 252\ pF\ \text{Maximum}$$

If C1 is larger than zero, then the value of C2 is determined by the charge sharing that occurs between C1 and C2. The worst case is when the input is at zero volts discharging C2 from 5.0V. The equation for the change in voltage on C1 is:

$$\Delta V = \frac{5.0V}{1 + C1/C}$$

where $C = C2 + C_{MUX}$

If ¼ LSB or 5.0 mV is an acceptable error, then the ratio of C1/C is

$$5.0\ mV = \frac{5.0V}{1 + C1/C} \text{ or } C1/C \cong 1000$$

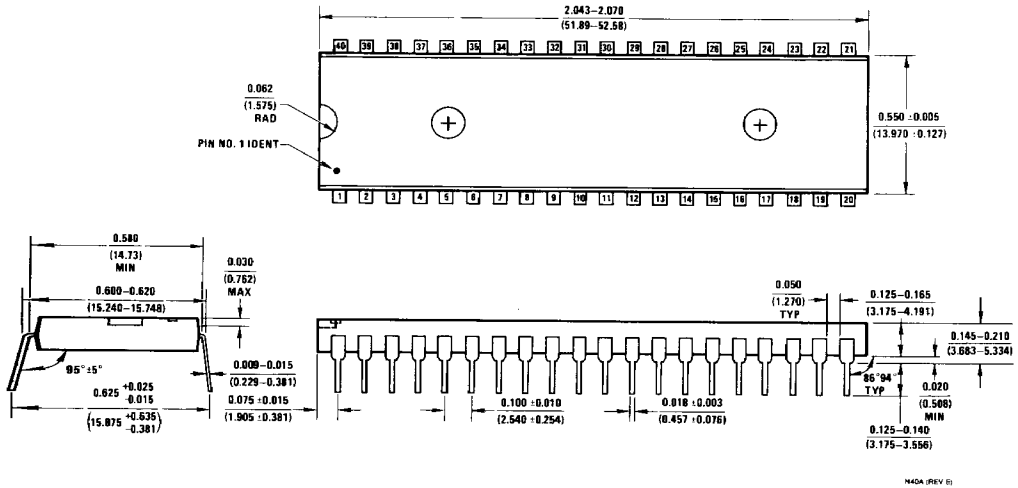
If C1 = 0.1 μF then C = 100 pF

$$C2 = C - C_{MUX} = 85\ pF\ \text{Maximum}$$

Since charge sharing occurs, why have any capacitor at all at the multiplexer output? The answer is noise immunity. Rapid voltage transients near the package may couple charge into this sensitive node. A transient may cause an error if it occurs during a comparison. Since the comparator is strobed, the actual critical time during a comparison is small.

Proper layout and component placement will minimize charge coupling and eliminate the need for an integration capacitor in most applications.

Physical Dimensions inches (millimeters)



Order Number ADC0830CCN
NS Package Number N40A

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