

Product Features

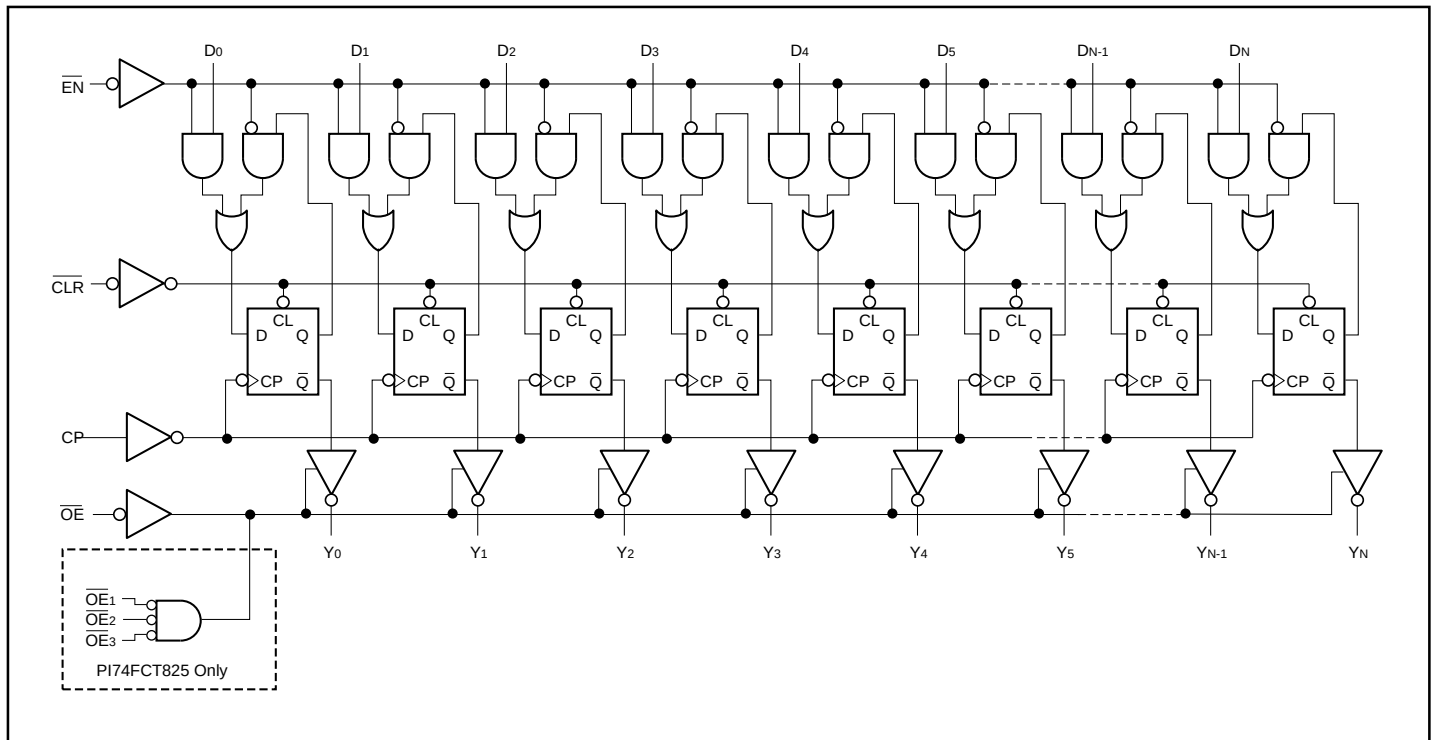
- PI74FCT821T/823T/825T/2821T/2823T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 24-pin 300 mil wide plastic DIP (P)
 - 24-pin 150 mil wide plastic QSOP (Q)
 - 24-pin 150 mil wide plastic TQSOP (R)
 - 24-pin 300 mil wide plastic SOIC (S)
- Device models available upon request

Product Description

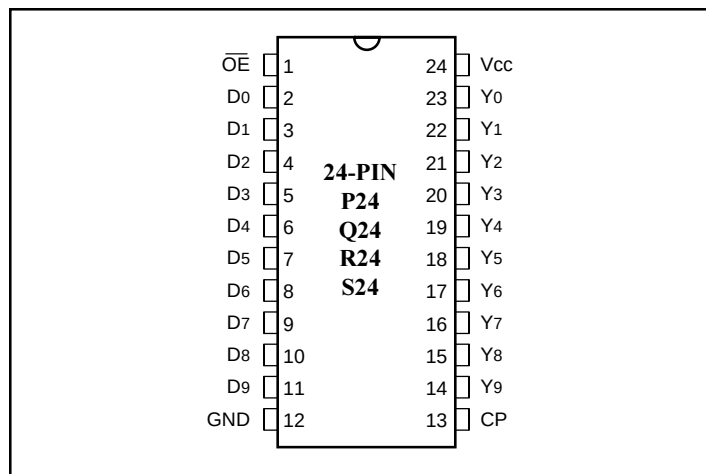
Pericom Semiconductor's PI74FCT series of logic circuits are produced using the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25-ohm series resistor on all outputs to reduce noise because of reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT821T/2821T is a 10-bit wide register designed with ten D-type flip-flops with a buffered common clock and buffered 3-state outputs. The PI74FCT823/2823T is a 9-bit wide register designed with Clock Enable and Clear. The PI74FCT825T is an 8-bit wide register with all PI74FCT823T controls plus multiple enables. When output enable ($\overline{OE}$) is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

Logic Block Diagram



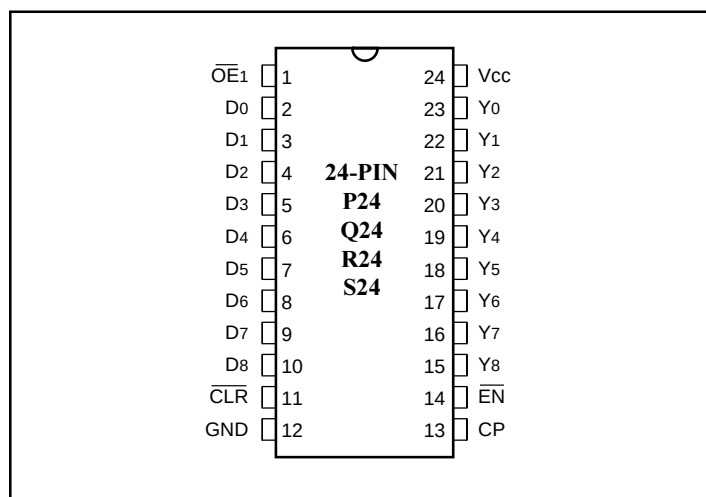
PI74FCT821/2821T Product Pin Configuration



Product Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition
DN	Data Inputs
YN	3-State Outputs
$\overline{CLR}$	Clear Input (Active LOW) (823/825/2823 Only)
$\overline{EN}$	Clock Enable Input (Active LOW)
GND	Ground
Vcc	Power

PI74FCT823/2823T Product Pin Configuration

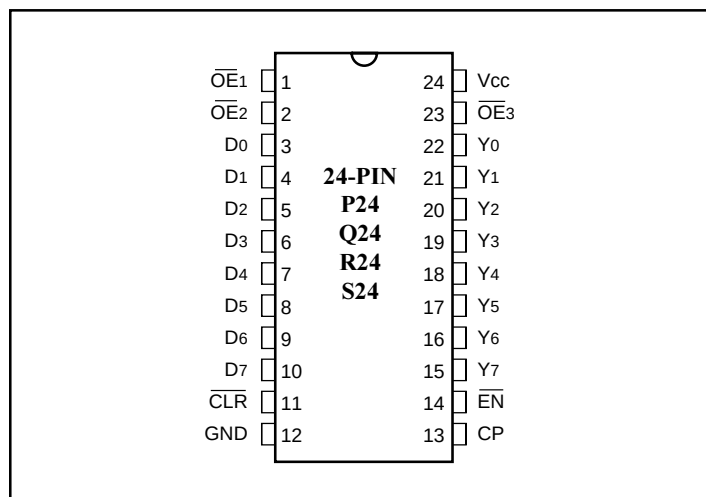


PI74FCT821/823/825/2821/2823T Truth Table⁽¹⁾

Function	Inputs					Outputs	Internal
	$\overline{CLR}$	$\overline{EN}$	$\overline{OE}$	CP	DN	YN	QN
High-Z	H	L	H	↑	L	Z	L
	H	L	H	↑	H	Z	H
Clear	L	X	H	X	X	Z	L
	L	X	L	X	X	L	L
Hold	H	H	H	X	X	Z	NC
	H	H	L	X	X	NC	NC
Load	H	L	H	↑	L	Z	L
	H	L	H	↑	H	Z	H
	H	L	L	↑	L	L	L
	H	L	L	↑	H	H	H

1. H = High Voltage Level
 L = Low Voltage Level
 X = Don't Care
 Z = High Impedance
 NC = No Change
 ↑ = LOW-to-HIGH transition

PI74FCT825T Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	−0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = −40°C to +85°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = −15.0 mA	2.4	3.0		V
V _{OL}	Output LOW Current	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48 mA		0.3	0.50	V
V _{OL}	Output LOW Current	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 12 mA (25Ω Series)		0.3	0.50	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max.	V _{IN} = GND			−1	μA
I _{OZH}	High Impedance	V _{CC} = MAX.	V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current		V _{OUT} = 0.5V			−1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = −18 mA			−0.7	−1.2	V
I _{OFF}	Power Down Disable	V _{CC} = GND, V _{OUT} = 4.5V		—	—	100	μA
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND		−60	−120		mA
V _H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	500	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open OE = EN = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = EN = GND fi = 5 MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		1.5	3.5 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.0	5.5 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = EN = GND Eight Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		3.8	7.3 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		6.0	16.3 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC} D_HN_T + I_{CCD} (f_{CP}/2 + fiN_I)
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4 V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
fi = Input Frequency
N_I = Number of Inputs at fi
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT821/2821T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	821AT/2821AT		821BT/2821BT		821CT/2821CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tplh tphl	Propagation Delay CP to Y _N ($\overline{OE}$ = LOW)	C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	ns
tsu	Setup Time HIGH or LOW, D _N to CP	C _L = 50 pF R _L = 500Ω	4.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW, D _N to CP		2.0	—	1.5	—	1.5	—	ns
tsu	Setup Time HIGH or LOW, $\overline{EN}$ to CP		4.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW, $\overline{EN}$ to CP		2.0	—	0	—	0	—	ns
tphl	Propagation Delay, $\overline{CLR}$ to Y _N		1.5	14.0	1.5	9.0	1.5	8.0	ns
trem	Recovery Time, ⁽³⁾ $\overline{CLR}$ to CP		6.0	—	6.0	—	6.0	—	ns
tw	Clock Pulse Width ⁽³⁾ HIGH or LOW		7.0	—	5.0	—	6.0	—	ns
tw	$\overline{CLR}$ Pulse Width ⁽³⁾ LOW		6.0	—	6.0	—	6.0	—	ns
tpZH tpZL	Output Enable Time $\overline{OE}$ to Y _N	C _L = 50 pF R _L = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	ns
tpHZ tpLZ	Output Disable Time ⁽³⁾ $\overline{OE}$ to Y _N	C _L = 50 pF R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT823/2823T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	823AT/2823AT		823BT/2823BT		823CT/2823CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tplH tphL	Propagation Delay CP to Y _N ($\overline{OE}$ = LOW)	C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	ns
tsU	Setup Time HIGH or LOW, D _N to CP	C _L = 50 pF R _L = 500Ω	4.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW, D _N to CP		2.0	—	1.5	—	1.5	—	ns
tsU	Setup Time HIGH or LOW, $\overline{EN}$ to CP		4.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW, $\overline{EN}$ to CP		2.0	—	0	—	0	—	ns
tphL	Propagation Delay, $\overline{CLR}$ to Y _N		1.5	13.0	1.5	9.0	1.5	8.0	ns
trem	Recovery Time, ⁽³⁾ $\overline{CLR}$ to CP		6.0	—	6.0	—	6.0	—	ns
tw	Clock Pulse Width ⁽³⁾ HIGH or LOW		7.0	—	5.0	—	6.0	—	ns
tw	$\overline{CLR}$ Pulse Width ⁽³⁾ LOW		6.0	—	6.0	—	6.0	—	ns
tpZH tpZL	Output Enable Time $\overline{OE}$ to Y _N	C _L = 50 pF R _L = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	ns
tpHZ tpLZ	Output Disable Time ⁽³⁾ $\overline{OE}$ to Y _N	C _L = 50 pF R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT825T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	825AT		825BT		825CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tplH tphL	Propagation Delay CP to Y _N ($\overline{OE}$ = LOW)	C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	ns
tsU	Setup Time HIGH or LOW, D _N to CP	C _L = 50 pF R _L = 500Ω	4.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW, D _N to CP		2.0	—	1.5	—	1.5	—	ns
tsU	Setup Time HIGH or LOW, $\overline{EN}$ to CP		4.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW, $\overline{EN}$ to CP		2.0	—	0	—	0	—	ns
tphL	Propagation Delay, $\overline{CLR}$ to Y _N		1.5	13.0	1.5	9.0	1.5	8.0	ns
trem	Recovery Time, $\overline{CLR}$ to CP		6.0	—	6.0	—	6.0	—	ns
tw	Clock Pulse Width HIGH or LOW		7.0	—	5.0	—	6.0	—	ns
tw	$\overline{CLR}$ Pulse Width ⁽³⁾ LOW		6.0	—	6.0	—	6.0	—	ns
tpZH tpZL	Output Enable Time $\overline{OE}$ to Y _N	C _L = 50 pF R _L = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	ns
tpHZ tplZ	Output Disable Time ⁽³⁾ $\overline{OE}$ to Y _N	C _L = 50 pF R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.