

Product Features:

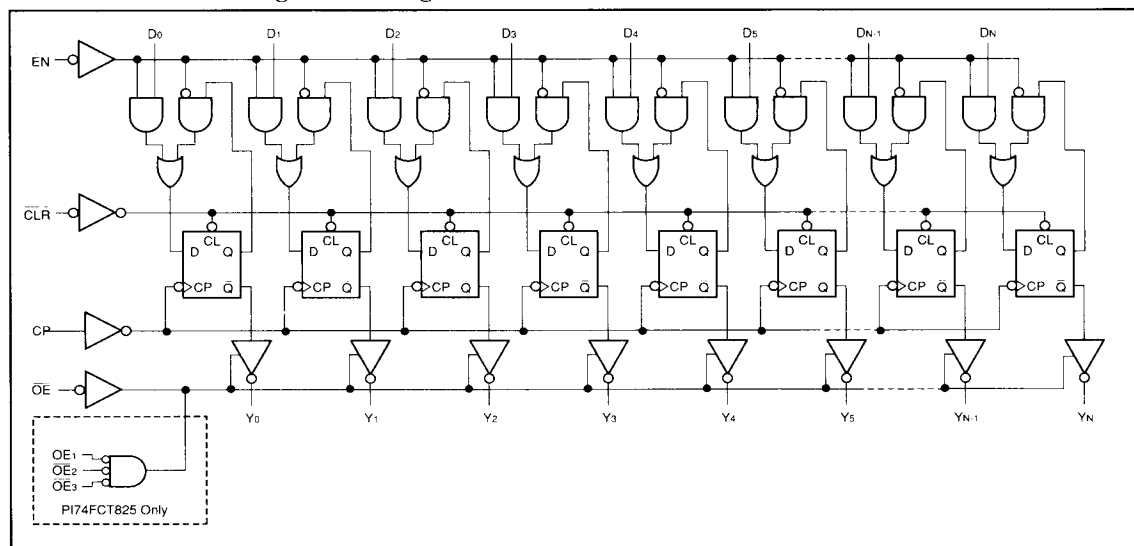
- PI74FCT821/823/825T have the same speed and drive of Bipolar FAST™ "F" series, at CMOS power levels.
"B" speeds at 7.5 ns max.
"C" speeds at 6.0 ns max.
"D" speeds are an industry first, at 4.2 to 5.0 ns max.
- TTL input and output levels, reducing problematic "ground bounce"
- High output drive, $I_{OL} = 48 \text{ mA}$
- Extremely low static power (1 mW, typ.)
- Industry standard pinout, plug into existing "74F" sockets for speed enhancement at reduced power levels
- Positive edge triggered D-type flip-flops
- Buffered common clock and asynchronous Clear input
- Hysteresis on all inputs
- Packaged in 24-pin plastic DIP, surface mount SOIC, or the industry's new "1/4 size" surface mount QSOP

Product Description:

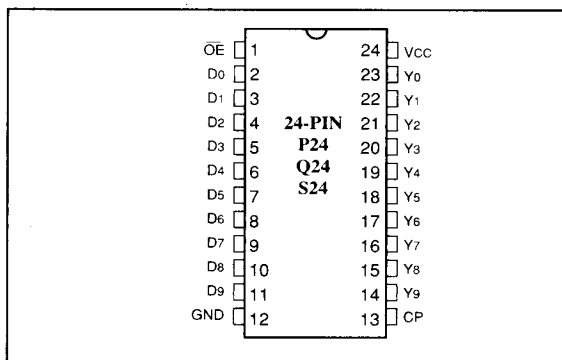
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT821T is a 10-bit wide register designed with ten D-type flip-flops with a buffered common clock and buffered 3-state outputs. The PI74FCT823T is a 9-bit wide register designed with Clock Enable and Clear. The PI74FCT825T is an 8-bit wide register with all PI74FCT823T controls plus multiple enables. When output enable ($\overline{OE}$) is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

All products are available in three package types: 24-pin, 300 mil wide plastic DIP, 300 mil wide plastic SOIC, and the industry's new 150 mil wide QSOP (one quarter the size of an SOIC).

PI74FCT821/823/825 Logic Block Diagram


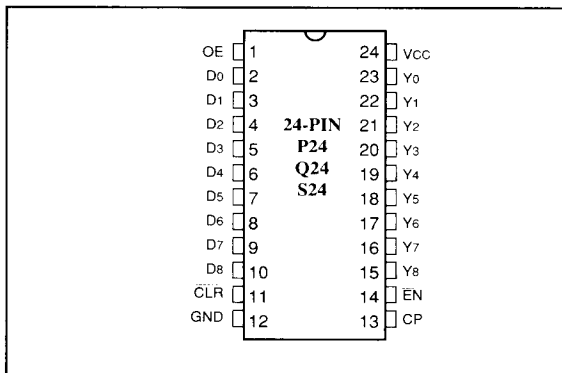
PI74FCT821T Product Pin Configuration



Product Pin Description

Pin Name	Description
OE	Output Enable Input (Active LOW)
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition
DN	Data Inputs
YN	3-State Outputs
CLR	Clear Input (Active LOW) (FCT823/5 Only)
EN	Clock Enable Input (Active LOW)
GND	Ground
Vcc	Power

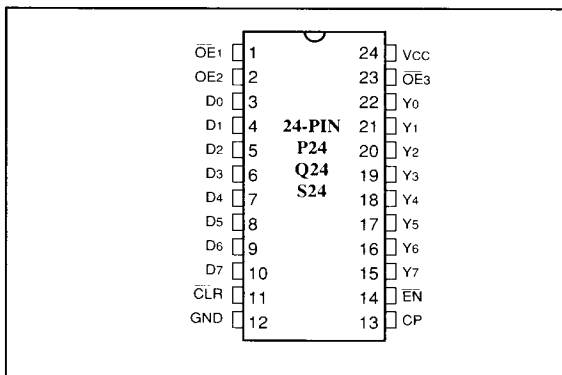
PI74FCT823T Product Pin Configuration



PI74FCT821/823/825T Truth Table⁽¹⁾

Function	Inputs					Outputs	Internal
	CLR	EN	OE	CP	DN	YN	QN
High-Z	H	L	H	↑	L	Z	L
	H	L	H	↑	H	Z	H
Clear	L	X	H	X	X	Z	L
	L	X	L	X	X	L	L
Hold	H	H	H	X	X	Z	NC
	H	H	L	X	X	NC	NC
Load	H	L	H	↑	L	Z	L
	H	L	H	↑	H	Z	H
	H	L	L	↑	L	L	L
	H	L	L	↑	H	H	H

PI74FCT825T Product Pin Configuration



1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance
NC = No Change
↑ = LOW-to-HIGH transition

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to Vcc
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = 0°C to +70°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL IOH = -8.0 mA	2.4	3.3		V
			2.0	3.0		V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL IOL = 48 mA		0.3	0.5	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
IiH	Input HIGH Current	VCC = Max., VIN = 2.7 V			5	μA
IiL	Input LOW Current	VCC = Max., VIN = 0.5 V			-5	μA
IOZH	High Impedance	VCC = Max., VOUT = 2.7 V			+10	μA
IOZL	Output Current	VCC = Max., VOUT = 0.5 V			-10	μA
Ii	Input HIGH Current	VCC = Max., VIN = VCC (Max.)			20	μA
Vik	Clamp Diode Voltage	VCC = Min., Iin = -18 mA		-0.7	-1.2	V
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-120		mA
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5 V			100	μA
VH	Input Hysteresis			200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0 V	6	10	pF
COUT	Output Capacitance	VOUT = 0 V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.2	1.5	mA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4 V ⁽³⁾		0.5	2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open OE = EN = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = EN = GND fi = 5 MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4 V V _{IN} = GND		2.2	6.0 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = EN = GND Eight Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		4.0	7.8 ⁽⁵⁾	
			V _{IN} = 3.4 V V _{IN} = GND		6.2	16.8 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0 V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + fi Ni)
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4 V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
fi = Input Frequency
Ni = Number of Inputs at fi
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT821T Switching Characteristics over Operating Range
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Parameters	Description	Conditions ⁽¹⁾	FCT821AT		FCT821BT		FCT821CT		FCT821DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay CP to Y _N (OE = LOW)	C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	1.5	4.2	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.0	ns
tSU	Set-up Time HIGH or LOW, D _N to CP	C _L = 50 pF R _L = 500Ω	4.0	—	3.0	—	3.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, D _N to CP		2.0	—	1.5	—	1.5	—	1.0	—	ns
tSU	Set-up Time HIGH or LOW, EN to CP		4.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW, EN to CP		2.0	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, CLR to Y _N		1.5	14.0	1.5	9.0	1.5	8.0	1.5	5.0	ns
tREM	Recovery Time, CLR to CP		6.0	—	6.0	—	6.0	—	3.0	—	ns
t _w	Clock Pulse Width HIGH or LOW		7.0	—	5.0	—	6.0	—	3.0	—	ns
t _w	CLR Pulse Width LOW		6.0	—	6.0	—	6.0	—	3.0	—	ns
tPZH tPZL	Output Enable Time OE to Y _N	C _L = 50 pF R _L = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	1.5	4.8	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	1.5	9.0	ns
tPHZ tPLZ	Output Disable Time OE to Y _N	C _L = 50 pF R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	1.5	4.0	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	1.5	4.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT823T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	FCT823AT		FCT823BT		FCT823CT		FCT823DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay CP to Y _N (OE = LOW)	C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	ns
tPHL		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.5	ns
tSU	Set-up Time HIGH or LOW, D _N to CP	C _L = 50 pF R _L = 500Ω	4.0	—	3.0	—	3.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, D _N to CP		2.0	—	1.5	—	1.5	—	1.0	—	ns
tSU	Set-up Time HIGH or LOW, EN to CP		4.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW, EN to CP		2.0	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, CLR to Y _N		1.5	13.0	1.5	9.0	1.5	8.0	1.5	5.0	ns
tREM	Recovery Time, CLR to CP		6.0	—	6.0	—	6.0	—	3.0	—	ns
tW	Clock Pulse Width HIGH or LOW		7.0	—	5.0	—	6.0	—	3.0	—	ns
tW	CLR Pulse Width LOW		6.0	—	6.0	—	6.0	—	3.0	—	ns
tPZH	Output Enable Time OE to Y _N	C _L = 50 pF R _L = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	1.5	4.8	ns
tPZL		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	1.5	9.0	ns
tPHZ	Output Disable Time OE to Y _N	C _L = 50 pF R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	1.5	4.0	ns
tPLZ		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	1.5	4.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT825T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	FCT825AT		FCT825BT		FCT825CT		FCT825DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay CP to Y _N (OE = LOW)	CL = 50 pF RL = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.5	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	1.5	9.6	ns
tSU	Set-up Time HIGH or LOW, DN to CP	CL = 50 pF RL = 500Ω	4.0	—	3.0	—	3.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, DN to CP		2.0	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW, EN to CP		4.0	—	3.0	—	3.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, EN to CP		2.0	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, CLR to Y _N		1.5	13.0	1.5	9.0	1.5	8.0	1.5	5.5	ns
tREM	Recovery Time, CLR to CP		6.0	—	6.0	—	6.0	—	3.0	—	ns
tW	Clock Pulse Width HIGH or LOW		7.0	—	5.0	—	6.0	—	3.0	—	ns
tW	CLR Pulse Width LOW		6.0	—	6.0	—	6.0	—	3.0	—	ns
tPZH tPZL	Output Enable Time OE to Y _N	CL = 50 pF RL = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	1.5	4.8	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	1.5	10.2	ns
tPHZ tPLZ	Output Disable Time OE to Y _N	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	1.5	4.0	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	1.5	6.1	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.