DATEL

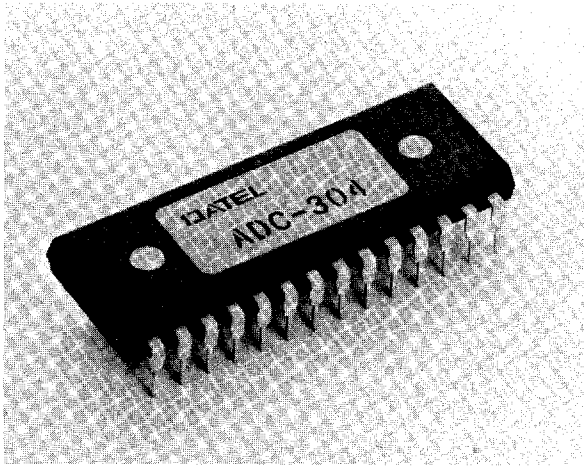
T-51-10-08

# ADC-304

## 8-Bit, 20 MHz Low-Power, Flash A/D

### FEATURES

- **8-Bit resolution**
- **± ½ LSB non-linearity**
- **20 MHz conversion rate**
- **8 MHz input bandwidth (-3 dB)**
- **Low-power consumption (390 mW)**
- **TTL-compatible**
- **Single or dual supply operation**



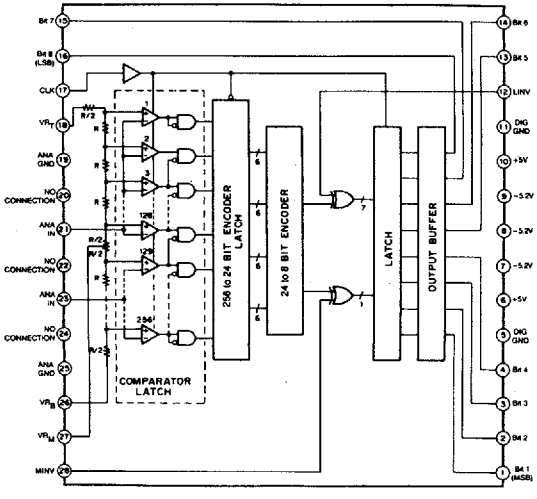

GENERAL DESCRIPTION

DATEL's ADC-304 is an 8-bit, 20 MHz analog-to-digital flash converter. The ADC-304 offers many performance features not obtainable from other flash A/D's.

Key features include a low-power dissipation of 390 mW and TTL compatible outputs. A wide analog input bandwidth of 8 MHz (-3 dB) allows operation without the need of a sample-hold. Also, single +5V supply operation is obtainable with an input range of +3 to +5V, eliminating the need for an additional power supply. A 0 to -2 V input range is available with ±5V supply operation.

Another novel feature of the ADC-304 is its user-selectable output coding. The MINV and LINV pins allow selection of binary, complementary binary, and if external offset circuitry is used for bipolar inputs, offset binary, two's complement, and complementary two's complement coding.

The ADC-304 is supplied in a 28-pin dual in-line package and operates over a -20°C to +75°C temperature range. Storage temperature range is from -65°C to +150°C.




**MECHANICAL DIMENSIONS**

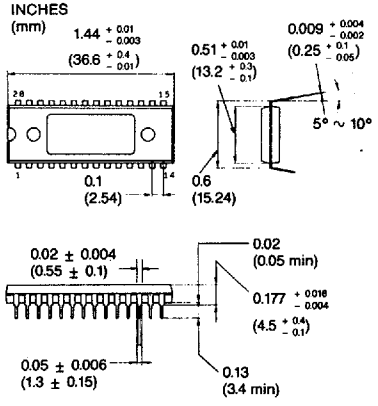



**Table 1. ADC-304 Input/Output Connections**

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | BIT 1 OUT (MSB) | 15 | BIT 7 OUT |
| 2 | BIT 2 OUT | 16 | BIT 8 OUT (LSB) |
| 3 | BIT 3 OUT | 17 | CLOCK INPUT |
| 4 | BIT 4 OUT | 18 | $V_{RT}$ |
| 5 | DIG GND | 19 | ANA GND |
| 6 | + 5V POWER ($V_{CC}$) | 20 | NO CONNECTION |
| 7 | − 5.2V POWER ($V_{EE}$) | 21 | ANA IN |
| 8 | − 5.2V POWER ($V_{EE}$) | 22 | NO CONNECTION |
| 9 | − 5.2V POWER ($V_{EE}$) | 23 | ANA IN |
| 10 | + 5V POWER ($V_{CC}$) | 24 | NO CONNECTION |
| 11 | DIG GND | 25 | ANA GND |
| 12 | LINV | 26 | $V_{RB}$ |
| 13 | BIT 5 OUT | 27 | $V_{RM}$ |
| 14 | BIT 6 OUT | 28 | MINV |

| ABSOLUTE MAXIMUM RATINGS (Ta = 25°C) | | | |
|---|---|---|---|
| Supply Voltage | $V_{CC}$-GND<br>$V_{EE}$-GND | 0 to +6<br>0 to −6 | V<br>V |
| Input Voltage (analog) | Vin<br>(Dual Power Supply) | $V_{EE}$ to ANA GND +0.3 | V |
| Input Voltage (reference) | $V_{RT}$, $V_{RB}$, $V_{RM}$<br>(Dual Power Supply)<br>\| $V_{RT}$—$V_{RB}$ \| | $V_{EE}$ to ANA GND +0.3<br>2.5 | V<br>V |
| Input Current | $I_{VRM}$ | −3.0 to +3.0 | mA |
| Input Voltage | Digital Inputs | −0.5 to $V_{CC}$ | V |

## FUNCTIONAL SPECIFICATIONS

Unless otherwise noted, the following specifications apply to the ADC-304 when used either with a single or dual power source. The test conditions are:

For Single Power Supply Operation:
$V_{CC}$ (Pins 6 + 10) = +5V, DIG GND = 0V
$V_{EE}$ (Pins 7, 8 + 9) = 0V, $V_{RT}$ (Pin 18) = +5V
$V_{RB}$ (Pin 26) = +3V, Ta = 25°C
ANA GND (Pins 19 + 25) = +5V

For Dual Power Supply Operation:
$V_{CC}$ (Pins 6 + 10) = +5V, DIG GND (Pins 5 + 11) = 0V
ANA GND = 0V, $V_{EE}$ = -5V
$V_{RT}$ (Pin 18) = 0V, $V_{RB}$ (Pin 26) = -2V
Ta = 25°C

| DESCRIPTION | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| **Inputs** | | | | |
| **Analog** | | | | |
| Input Range | $V_{RB}$ | | $V_{RT}$ | V |
| Input Capacitance | - | 30 | 35 | pF |
| Input Bias Current | - | 50 | 100 | μA |
| Offset Voltage: | | | | |
| ($V_{RT}$) | 8 | 13 | 19 | mV |
| ($V_{RB}$) | 0 | 5 | 11 | mV |
| **Digital** | | | | |
| Logic Levels: | | | | |
| Logic "1" | 2.0 | - | - | V |
| Logic "0" | - | - | 0.8 | V |
| Logic Input Currents : | | | | |
| Logic "1" | - | −100 | 0 | μA |
| Logic "0" | - | −0.32 | −0.5 | mA |
| **Outputs** | | | | |
| Resolution | 8 | | | Bits |
| Output Coding | Straight Binary<br>Complementary Binary<br>2's Complement<br>Complementary 2's Complement | | | |
| Logic levels: | | | | |
| Logic "1" | 2.7 | 3.4 | - | V |
| Logic "0" | - | - | 0.5 | V |
| Logic Level Loading: | | | | |
| Logic "1" | - | −500 | - | μA |
| Logic "0" | - | - | 3 | mA |
| Output Data Delay | | | | |
| (TDLH) | - | 25 | 30 | nSec. |
| (TDHL) | - | 26 | 35 | nSec. |

## TECHNICAL NOTES

1. DIG GND pins (5 and 11) and $V_{CC}$ pins (6 and 10) connect to separate internal circuits within the ADC-304. Connect these pins to their respective PCB patterns.
2. Layout of the analog and digital sections should be separated to reduce interference from noise. To further guard against unwanted noise, it is recommended to bypass, as close as possible, the voltage supply pins (6,10) to their respective ground pins (5,11) with a 1 μF and a 0.01 μF ceramic disk capacitor in parallel.
3. The input capacitance of the analog input is much smaller than that of a typical Flash A/D Converter. It is necessary to use an amplifier with sufficient bandwidth and driving power. The analog input pins (21,23) are separated internally, so they should be connected together externally. If the ADC-304 is driven with a low- output impedance amplifier, parasitic oscillations may occur.

   These parasitic oscillations can be prevented by introducing a small resistance of 2 to 10Ω between the amplifier output and the ADC-304's A/D input. This resistance must be of very low value of inductance at high frequencies.

   Note that each of the analog input pins are divided in this manner with these resistances. Connect the driving amplifier as close as possible to the A/D input of the ADC-304.
4. The voltage between $V_{RT}$ (pin 18) and $V_{RB}$ (pin 26) is equivalent to the dynamic range of the analog input. Bypass $V_{RB}$ to ANA GND (pins 19 and 25) by means of a 1 μF and 0.01 μF capacitor in parallel. To balance the characteristics of the ADC-304 at high frequencies, bypass $V_{RM}$ (pin 27) with a 0.01μF capacitor to ANA GND (pins 19 and 25).

   Also, $V_{RM}$ (pin 27) can be used as a trimming pin for more precise linearity compensation. A stable voltage source with a potential equal to −FSR and a 1 KΩ potentiometer can be connected to $V_{RM}$ (pin 27) as shown in Figure 3 for this purpose.
5. Separate the clock input, CLK (pin 17), from other leads as much as possible, observing proper EMI and RFI wiring techniques. This will reduce the inductive pick-up of this lead from interfering with the "clean" operation of the ADC-304.

| Performance | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| Conversion Rate[1] | 20 | - | - | MHz |
| Non-Linearity | - | - | ±1/2 | LSB |
| Differential Non-Linearity | - | - | ±1/2 | LSB |
| Differential Gain Error[2] | - | - | 1.5 | % |
| Differential Phase Error[2] | - | - | 0.5 | Degrees |
| Aperture Delay | 5 | 7 | 9 | nSec. |
| Aperture Jitter | - | 30 | - | pSec. |
| Clock pulse width: Tpw1 | 35 | - | - | nSec. |
| Tpw0 | 10 | - | - | nSec. |
| Reference Pin Current | - | 15 | 18 | mA |
| Reference Resistance (VRT to VRB) | - | 130 | - | ohms |
| Reference Input (Dual Supply) | | | | |
| (VRT) | −0.1 | 0 | +0.1 | V |
| (VRB) | −1.8 | −2.0 | −2.2 | V |
| **Power Supply Requirements** | | | | |
| **Single Power Supply** | | | | |
| Supply voltage | | | | |
| (VCC) | 4.75 | - | 5.25 | V |
| (VEE) | - | 0 | - | V |
| Supply Current: | | | | |
| (ICC + IEE) | - | 71 | 88 | mA |
| Power Dissipation | - | 360 | 442 | mW |
| **Dual Power Supply** | | | | |
| Supply Voltage: | | | | |
| (VCC) | 4.75 | 5.0 | 5.25 | V |
| (VEE) | −4.75 | −5.2 | −5.5 | V |
| Supply Current | | | | |
| (ICC) | - | 10 | 14 | mA |
| (IEE) | - | 62 | 75 | mA |
| Power Dissipation | - | 390 | 440 | mW |
| **Physical/Environmental** | | | | |
| Operating Temperature | −20 | - | +75 | °C |
| Storage Temperature | −55 | - | +150 | °C |

1. fin = 1 KHz, ramp
2. NTSC 40 IRE-modulated ramp, Fc = 14.3 MSPS

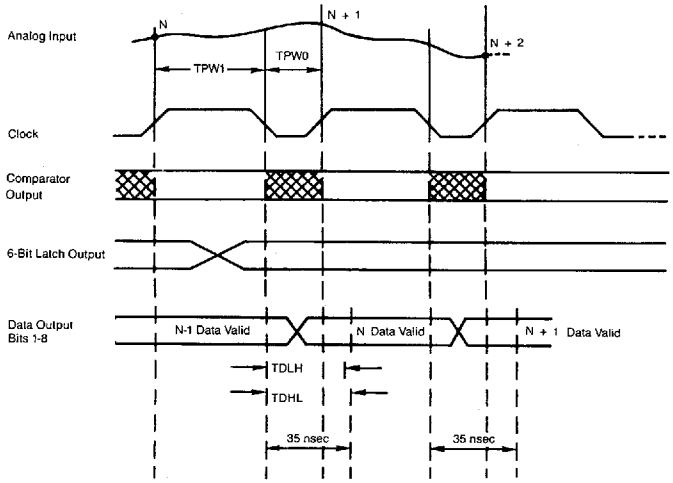



**Figure 2: ADC-304 Timing Diagram**

**TECHNICAL NOTES (CONT.)**

6. The analog input signal is sampled on the positive-going edge of CLK. Corresponding digital data appears at the output on the negative-going edge of the CLK pulse after a small delay of 35 nSec. maximum (TDLH, TDHL). Refer to the Timing diagram, Figure 4, for more information.
7. Connect all free pins to ANA GND (pins 19 and 25) to reduce unwanted noise.

   The analog input range is equal to a 2V spread. The voltage on VRT-VRB will equal 2V. The connection of VRT and ANA GND is 2V higher than VRB. Whether using a single or dual power supply, the analog input will range from the value of VRT to VRB. If VRT equals +5V, then VRB will equal +3V and the analog input range will be from +5 to +3V.

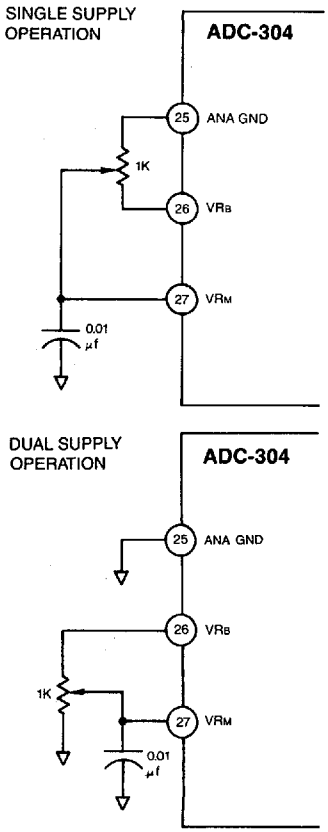



**Figure 3: Improving Linearity Compensation**

**Table 2. Output Coding for +5V Power Supply Operation (+5 to +3V Signal Input)**

| | | Straight Binary | Complement 2's Complement | 2's Complement | Complement Binary |
|---|---|---|---|---|---|
| Unipolar Scale | MINV | 0 | 0 | 1 | 1 |
| | LINV | 0 | 1 | 0 | 1 |
| +FS – 1 LSB | +4.9922V | 11111111 | 10000000 | 01111111 | 00000000 |
| +7/8 FS | +4.7500V | 11011111 | 10100000 | 01011111 | 00100000 |
| +3/4 FS | +4.5000V | 10111111 | 11000000 | 00111111 | 01000000 |
| +1/2 FS | +4.0000V | 01111111 | 00000000 | 11111111 | 10000000 |
| +1/4 FS | +3.5000V | 00111111 | 01000000 | 10111111 | 11000000 |
| +1/8 FS | +3.2500V | 00011111 | 00100000 | 11011111 | 11100000 |
| +1 LSB | +3.0078V | 00000001 | 01111110 | 10000001 | 11111110 |
| Zero | +3.0000V | 00000000 | 01111111 | 10000000 | 11111111 |

**Table 3. Output Coding for ±5V Power Supply Operation (0 to –2V Signal Input)**

| | | Straight Binary | Complement 2's Complement | 2's Complement | Complement Binary |
|---|---|---|---|---|---|
| Unipolar Scale | MINV | 0 | 0 | 1 | 1 |
| | LINV | 0 | 1 | 0 | 1 |
| 0 | 0V | 11111111 | 10000000 | 01111111 | 00000000 |
| –1 LSB | –7.813 mV | 11111110 | 10000001 | 01111110 | 00000001 |
| –1/8 FS | –250.00 mV | 11011111 | 10100000 | 01011111 | 00100000 |
| –1/4 FS | –500.00 mV | 10111111 | 11000000 | 00111111 | 01000000 |
| –1/2 FS | –1.0V | 01111111 | 00000000 | 11111111 | 10000000 |
| –3/4 FS | –1.5V | 00111111 | 01000000 | 10111111 | 11000000 |
| –7/8 FS | –1.75V | 00011111 | 00100000 | 11011111 | 11100000 |
| –FS + 1 LSB | –1.9922V | 00000000 | 01111111 | 10000000 | 11111111 |

## APPLICATION CIRCUITS

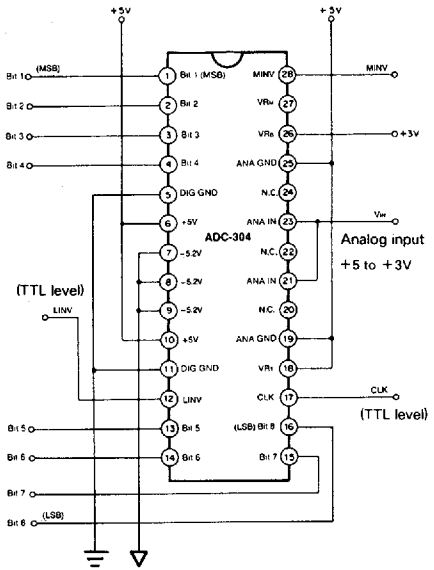



**Figure 5: Connections for +5V Power Supply Operation**

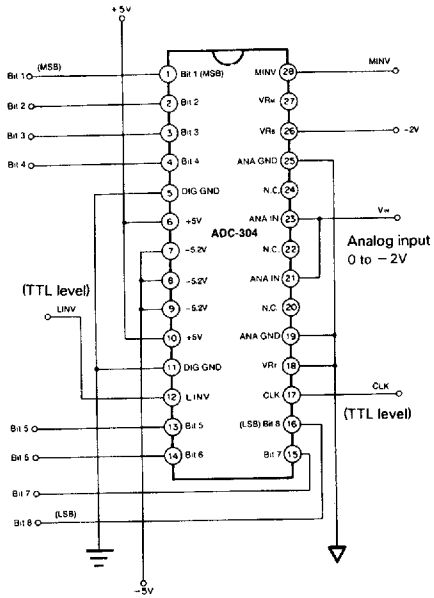



**Figure 6: Connections for ±5V Power Supply Operation**

**ORDERING INFORMATION**

| MODEL | DESCRIPTION |
|---|---|
| ADC-304 | 8-bit, 20 MHZ, Low-power, flash A/D |