

PI74ALPTX16244

16-Bit Buffer/Driver with 3-State Outputs

Product Features:

- PI74ALPTX family is designed for low voltage operation,
- Supports Live Insertion
- $V_{DD} = 1.8V$ to $3.6V$
- 3.6V Tolerant Inputs and Outputs
- Bus Hold
- High Drive, $-32/64mA$
- Typical V_{OLP} (Output Ground Bounce) $< 0.4V$
at $V_{DD} = 2.5V$, $T_A = 25^\circ C$
- Typical V_{OHV} (Output V_{OH} Undershoot) $< 0.4V$
at $V_{DD} = 2.5V$, $T_A = 25^\circ C$
- Industrial operation at $-40^\circ C$ to $+85^\circ C$
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A48)
 - 48-pin 173 mil wide plastic TVSOP (K48)

Product Description:

Pericom Semiconductor's PI74ALPTX series of logic circuits are produced in the Company's advanced 0.35 micron CMOS technology, achieving industry leading speed.

The buffer/driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

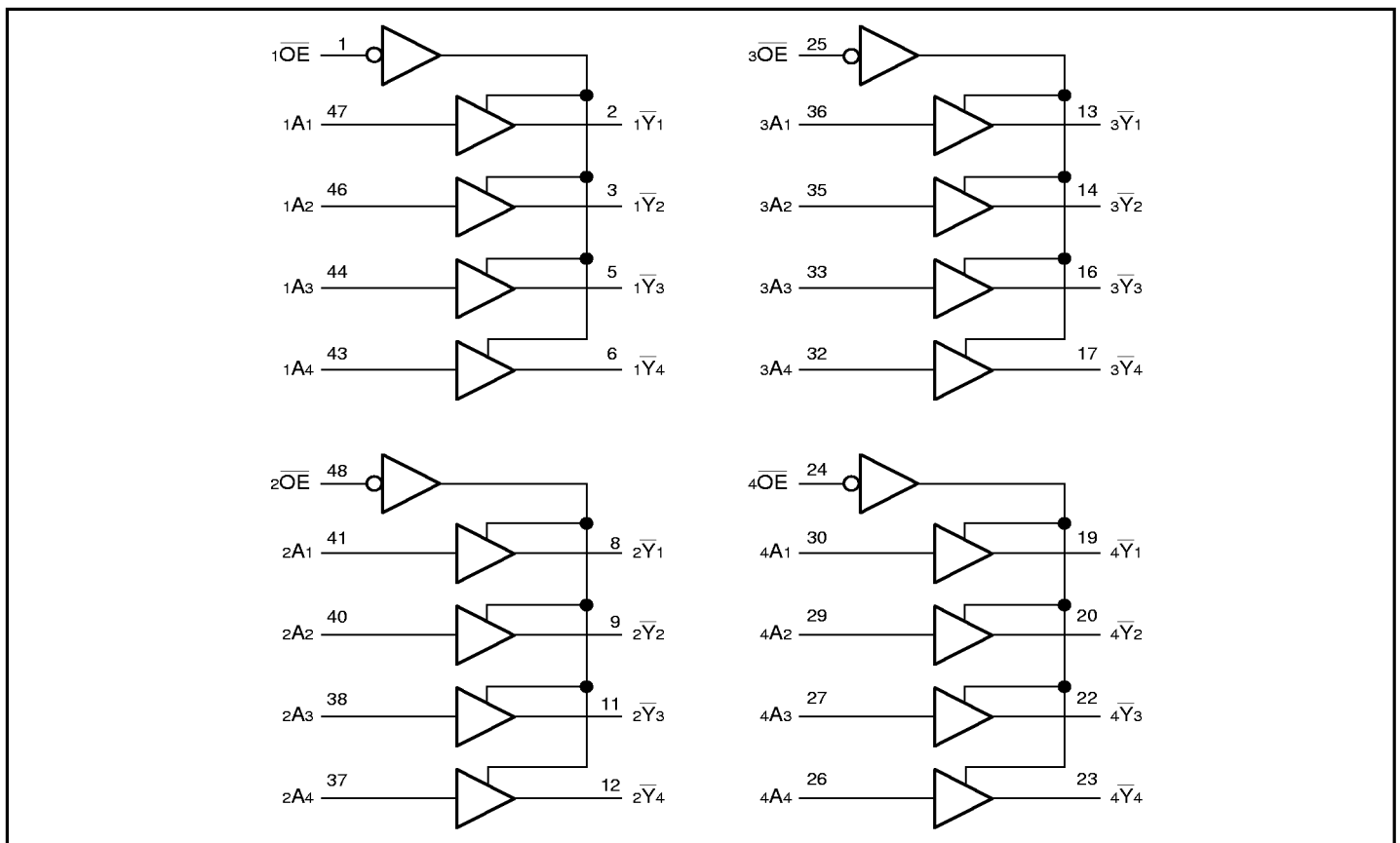
The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable (OE) inputs.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The PI74ALPTX16244 can be used as a translator, allowing it to operate in mixed 3V/5V systems.

The PI74ALPTX16244 has "Bus Hold," which retains the data input's last state whenever the data input goes to high-impedance, preventing "floating" inputs and eliminating the need for pullup/down resistors.

Logic Block Diagram



Product Pin Description

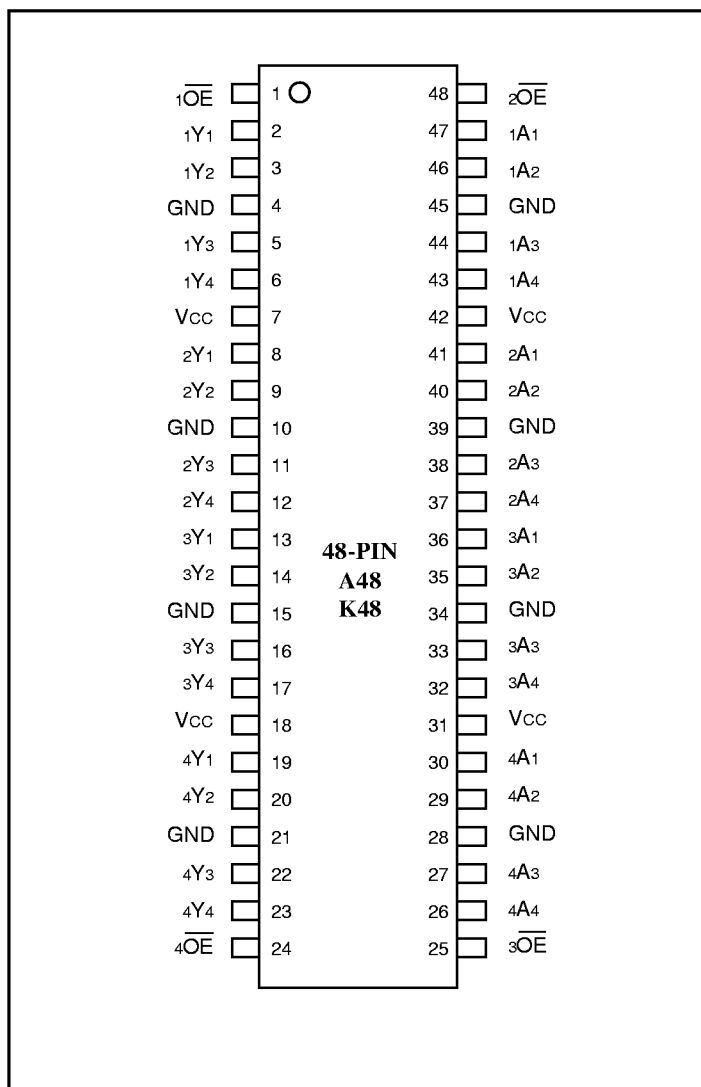
Pin Name	Description
$\overline{nOE}$	3-State Output Enable Inputs (Active LOW)
nAx	Inputs
nYx	3-State Outputs
GND	Ground
VCC	Power

Truth Table⁽¹⁾

Inputs		Outputs
$\overline{nOE}$	nAx	nYx
L	H	H
L	L	L
H	X	Z

Note:

1. H = High Signal Level
L = Low Signal Level
X = Don't Care or Irrelevant
Z = High Impedance

Product Pin Configuration


Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage Range, V_{DD}	-0.5V to 4.6V
Input Voltage Range, V_I	-0.5V to 4.6V
Output Voltage Range, V_O (3-States)	-0.5V to 4.6V
Output Voltage Range, $V_O^{(1)}$ (Active)	-0.5V to $V_{DD}+0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50mA
$V_O > V_{DD}$	$\pm 50mA$
DC Output Source/Sink Current (I_{OH}/I_{OL})	-64/128mA
DC V_{DD} or GND Current per Supply Pin (I_{CC} or GND)	$\pm 100mA$
Storage Temperature Range, T_{stg}	-65°C to 150°C

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions²

			Min.	Max.	Unit
V_{DD}	Supply voltage	Operating	1.8	3.6	V
		Data Retention Only	1.2	3.6	
V_{IH}	High-level input voltage	$V_{DD} = 2.7V$ to 3.6V	2.0		
V_{IL}	Low-level input voltage	$V_{DD} = 2.7V$ to 3.6V		0.8	
V_I	Input voltage		-0.3	3.6	
V_O	Output voltage	Active State	0	V_{DD}	
		Off State	0	3.6	
	Output current in I_{OH}/I_{OL}	$V_{DD} = 3.0V$ to 3.6V		-32/64	mA
		$V_{DD} = 3.0V$ to 3.6V		± 24	
		$V_{DD} = 2.3V$ to 2.7V		± 18	
		$V_{DD} = 1.8V$		± 6	
$\Delta t/\Delta v$	Input transistion rise or fall rate ⁽³⁾		0	10	ns/V
T_A	Operating free-air temperture		-40	85	C

Notes

1. Absolute maximum of I_O must be observed.
2. Unused control inputs must be held HIGH or LOW to prevent them from floating.
- 3 As measured between 0.8V and 2.0V, $V_{DD} = 3.0V$.

Electrical Characteristics over Recommended Operating Free-Air Temperature Range

(unless otherwise noted)

DC Characteristics 74ALPTX16244 ($2.7V < V_{DD} \leq 3.6V$)

	Parameter	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0			V
V_{IL}	LOW Level Input Voltage					0.8	
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$		$V_{DD} - 0.2$			
		$I_{OH} = -12 \text{ mA}$	2.7	2.2			
		$I_{OH} = -18 \text{ mA}$	3.0	2.4			
		$I_{OH} = -24 \text{ mA}$		2.2			
		$I_{OH} = -32 \text{ mA}$		2.3			
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.7 - 3.6			0.2	
		$I_{OL} = 12 \text{ mA}$	2.7			0.4	
		$I_{OL} = 18 \text{ mA}$	3.0			0.4	
		$I_{OL} = 24 \text{ mA}$				0.5	
		$I_{OL} = 32 \text{ mA}$				0.5	
		$I_{OL} = 64 \text{ mA}$				0.55	
I_I	Input Leakage Current	$V_I = 0.0V, V_I = 3.6V$	3.6			± 5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH} \text{ or } V_{IL}$	2.7 - 3.6			± 10	
I_{OFF}	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0			10	
I_{HOLD}	Bus Hold Current A or B Outputs	$V_I = 0.8V$	3.0	75			
		$V_I = 2.0V$		-75			
I_{DD}	Quiescent Supply Current	$V_I = V_{DD} \text{ to GND}$	2.7 - 3.6			20	
		$V_{DD} \leq (V_I, V_O) \leq 3.6V$				± 20	
ΔI_{DD}	Increase in I_{DD} per input	$V_{IH} = V_{DD} - 0.6V$, Other inputs at V_{DD} or Gnd				750	

DC Characteristics ALPTX16244 ($2.3V \leq V_{DD} \leq 2.7V$)

	Parameters	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IH}	HIGH Level Input Voltage		2.3 - 2.7	1.6			V
V_{IL}	LOW Level Input Voltage					0.7	
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.3	$V_{DD} - 0.2$			
		$I_{OH} = -6 \text{ mA}$		2.0			
		$I_{OH} = -12 \text{ mA}$		1.8			
		$I_{OH} = -16 \text{ mA}$		1.7			
		$I_{OH} = -24 \text{ mA}$		1.7			
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 - 2.7			0.2	
		$I_{OL} = 12 \text{ mA}$	2.3			0.4	
		$I_{OL} = 18 \text{ mA}$				0.4	
		$I_{OL} = 24 \text{ mA}$				0.5	
I_I	Input Leakage Current	$V_I = 0.0V, V_I = 2.7V$	2.7			± 5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH} \text{ or } V_{IL}$	2.3 - 2.7			± 10	
I_{OFF}	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0			10	
$I_{HOLD}^{(1)}$	Bus Hold Current A or B Outputs	$V_I = 0.7V$	2.5		90		
		$V_I = 1.7V$			-90		
I_{DD}	Quiescent Supply Current	$V_I = V_{DD} \text{ or GND}$	2.3 - 2.7			20	
		$V_{DD} \leq (V_I, V_O) \leq 3.6V$				± 20	
ΔI_{DD}	Increase in I_{DD} per input	$V_{IH} = V_{DD} - 0.6V$, Inputs at V_{DD} or Gnd				TBD	

Electrical Characteristics over Recommended Operating Free-Air Temperature Range

(unless otherwise noted) (continued from previous page)

DC Characteristics ALPTX16244 ($1.8V \leq V_{DD} \leq 2.3V$)

	Parameters	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IH}	HIGH Level Input Voltage		1.8 - 2.3	$0.7 \times V_{DD}$			V
V_{IL}	LOW Level Input Voltage					$0.2 \times V_{DD}$	
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.8	$V_{DD} - 0.2$			
		$I_{OH} = -6 \text{ mA}$		1.4			
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$				0.2	
		$I_{OL} = 6 \text{ mA}$				0.3	
I_I	Input Leakage Current	$V_I = 0.0V, V_I = 1.8V$				± 5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH} \text{ or } V_{IL}$				± 10	
I_{OFF}	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0			10	
$I_{HOLD}^{(1)}$	Bus Hold Current A or B Outputs	$V_I = 0.4$	1.8		50		
		$V_I = 1.3$			-50		
I_{DD}	Quiescent Supply Current	$V_I = V_{DD} \text{ or GND}$				20	
		$V_{DD} \leq (V_I, V_O) \leq 3.6V$				± 20	
ΔI_{DD}	Increase in I_{DD} per input	$V_I = V_{DD} - 0.6V$, Other inputs at V_{DD} or Gnd				TBD	

Note: 1. Not guaranteed

AC Electrical Characteristics 74ALPTX16244

Symbol	Parameter	TA = -40°C to +85°C, C _L = 50pF, R _L = 500Ω						Units
		V _{DD} = 3.3V ±0.3V		V _{DD} = 2.5V ±0.2V		V _{DD} = 1.8V		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PHL} , t _{PLH}	Prop Delay	1.0	2.4	1.0	3.5	1.5	5.7	ns
t _{PZL} , t _{PZH}	Output Enable Time	1.5	3.8	2.0	5.9	1.5	7.0	
t _{PLZ} , t _{PHZ}	Output Disable Time	1.5	4.0	2.0	5.2	1.5	5.0	
t _{OSH L} t _{OSL H}	Output to Output Skew (Note 1)		0.5		0.5		0.5	

Note

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (tOSH L) or LOW to HIGH (tOSL H).

Dynamic Switching Characteristics (Target Spec, Eng. Ref Only)

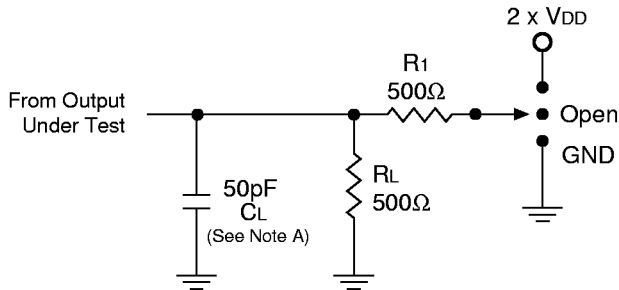
Symbol	Parameter	Conditions	VDD	TA = +25°C Typical	Units
VOLP	Quiet Output Dynamic Peak VOL	CL = 50pF, VIH = VDD, VIL = 0V	1.8 2.5 3.3	0.25 0.6 0.8	V
VOLP	Quiet Output Dynamic Valley VOL	CL = 50pF, VIH = VDD, VIL = 0V	1.8 2.5 3.3	-0.25 -0.6 -0.8	
VOLP	Quiet Output Dynamic Valley VOH	CL = 50pF, VIH = VDD, VIL = 0V	1.8 2.5 3.3	1.5 1.9 2.2	

Capacitance

Symbol	Parameter	Conditions	TA = +25°C Typical	Units
CIN	Input Capacitance	VDD = 1.8, 2.5V or 3.3V, VI = 0V or VDD	TBD	pF
COU T	Output Capacitance	VI = 0V or VDD, VDD = 1.8V, 2.5V or 3.3V	TBD	
CPD	Power Dissipation Capacitance	VI = 0V or VDD, F = 10 MHz VDD = 1.8V, 2.5V or 3.3V	TBD	

Test Circuits and Switching Waveforms

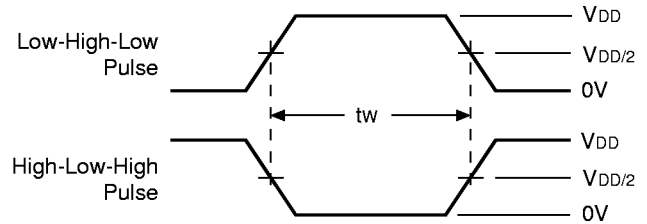
Parameter Measurement Information ($V_{DD} = 1.8V - 3.6V$)



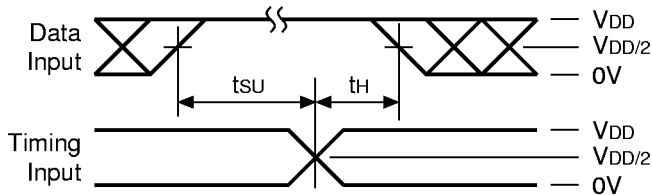
Switch Position

Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{DD}$
t_{PHZ}/t_{PZH}	GND

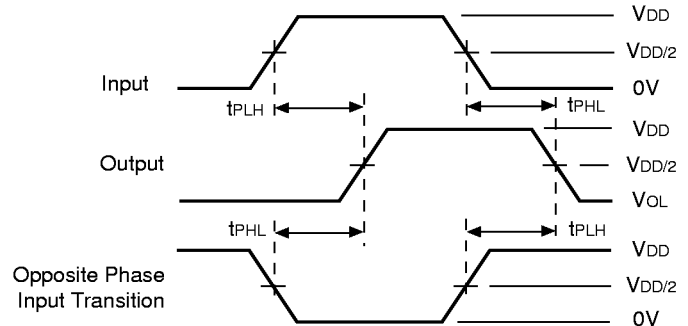
Pulse Width



Setup, Hold, and Release Timing



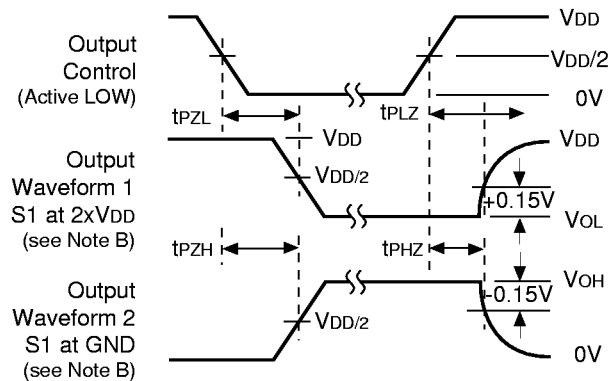
Propagation Delay



Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50\Omega$, $t_r \leq 2\text{ns}$, $t_f \leq 2\text{ns}$, *measured from 10% to 90%, unless otherwise specified.*
- The outputs are measured one at a time with one transition per measurement.

Enable Disable Timing



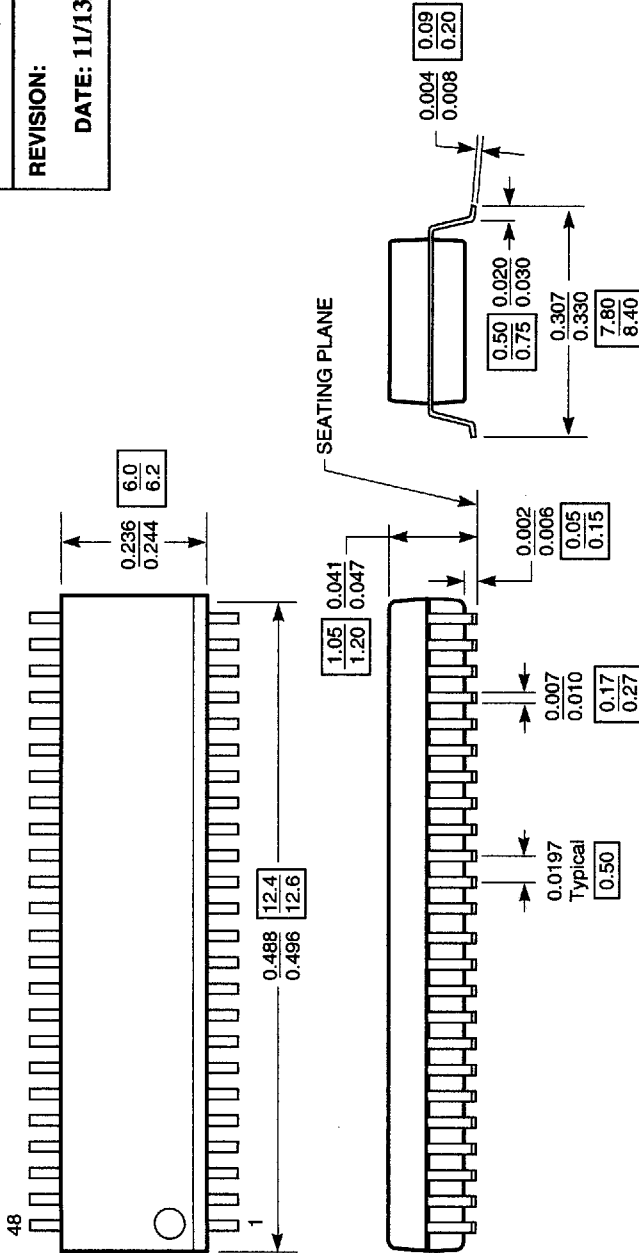
PACKAGE MECHANICAL DIMENSIONS

DOCUMENT CONTROL NO.

PD- 1501

REVISION:

DATE: 11/13/95



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DENOTES DIMENSIONS
IN MILLIMETERS



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DESCRIPTION: 48-PIN TSSOP (240 MIL WIDE)

PACKAGE CODE: A48