Very High Speed 16-Bit, 2 MHz Sampling A/D Converter

Introduction

The ADC4322 is a complete 16-bit, 2 MHz A/D converter subsystem with a built-in sample-and-hold amplifier in a space-saving 46 pin hybrid package. It offers pin-programmable input voltage ranges of ±2.5V, ±5V, ±10V and 0 to +10V. It has been designed for use in applications requiring high speed and high resolution front ends, such as ATE, digital oscilloscopes, medical imaging, radar, sonar, and analytical instrumentation. The ADC4322 is capable of digitizing a 1 MHz signal at a 2 MHz sampling rate with a guarantee of no missing codes from –10°C to +40°C. Equally impressive in frequency domain applications, the ADC4322 features 86 dB signal-to-noise ratio with input signals from dc to 100 kHz.

The ADC4322 utilizes the latest semiconductor technologies to produce a cost effective, high performance part in a 46 pin hybrid package. It is designed around a two-pass, sub-ranging architecture that integrates a low distortion sample-and-hold amplifier, precision voltage reference, ultra-stable 16-bit linear reference D/A converter, all necessary timing circuitry and tri-state CMOS/TTL compatible output lines for ease of system integration.

Superior performance and ease of use make the ADC4322 the ideal solution for those applications requiring a sample-and-hold amplifier directly at the input to the A/D converter. Having the S/H amplifier integrated with the A/D converter benefits the system designer in two ways. First, the S/H has been designed specifically to complement the performance of the A/D converter; for example, the acquisition time, hold mode settling and droop rate have been optimized for the A/D converter, resulting in exceptional overall performance. Second, the designer achieves true 16-bit performance, avoiding degradation due to ground loops, signal coupling, jitter and digital noise introduced when separate S/H and A/D converters are interconnected. Furthermore, the accuracy, speed, and quality of the ADC4322 are fully ensured by thorough, computer controlled factory tests of each unit.

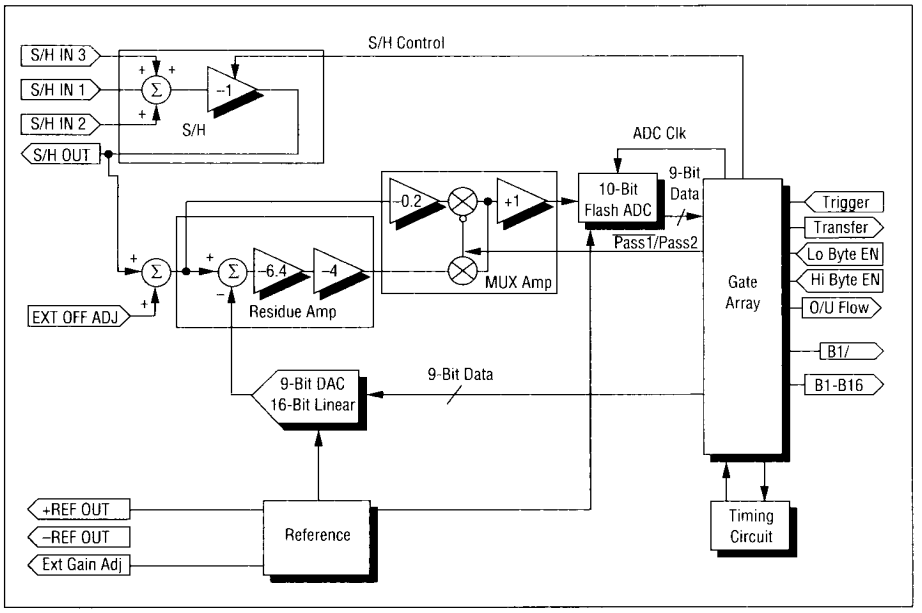

Figure 1. ADC4322 Functional Block Diagram.

Features

- Built-in S/H Amplifier
- Unique 2-Pass Sub-Ranging Architecture
- 16-Bit Resolution
- 2 MHz Conversion Rate
- 0.003% Maximum Integral Nonlinearity
- No Missing Codes
- Peak Distortion: –92 dB (100 kHz Input)
- Signal to Noise Ratio: 86 dB
- Total Harmonic Distortion: –86 dB (100 kHz Input)
- TTL/CMOS Compatibility
- Low Noise
- Compact Size: 46 Pin Hybrid DIP
- Electromagnetic/Electrostatic Shielding

Applications

- Digital Signal Processing
- Sampling Oscilloscopes
- Automatic Test Equipment
- High-Resolution Imaging
- Analytical Instrumentation
- Medical Instrumentation
- CCD Detectors
- IR Imaging
- Sonar/Radar

ANALOGIC®
The World Resource for Precision Signal Technology

ADC4322

Specifications[1]

ANALOG INPUT

Input Voltage Range
Bipolar
±2.5V, ±5V, ±10V

Unipolar
0 to +10V

Maximum Input Without Damage
±15.5V Typ.

S/H Direct Input Resistance
3k, ±10V
1.5k, ±5V (0–10V range)
750Ω, ±2.5V

Ext. Offset and Gain Adj. Sensitivity
300 ppm FSR/V

DIGITAL INPUTS

Compatibility
TTL, HCT, and ACT

Logic "0"
+0.8V Max.

Logic "1"
+2.0V Min.

Trigger
Negative Edge Triggered

Loading
2 HCT Loads

Trigger Pulse Width
50 ns Min.

High Byte Enable
Active Low, B1-B8, $\overline{B1}$

Low Byte Enable
Active Low, B9-B16

INTERNAL REFERENCE

Voltage
+5V, ±0.5% Max.

Stability
25 ppm/°C Max.

Available Current[2]
1.0 mA Max.

DIGITAL OUTPUTS

Fan-Out
1 TTL Load

Logic "0"
+0.4V

Logic "1"
+2.4V

Output Coding
Binary, Offset Binary, 2's complement

Transfer Pulse
Data valid on positive edge

Over/Under Flow
Valid = logic "0" (occurs only when ±FS have been exceeded)

DYNAMIC CHARACTERISTICS

Maximum Throughput Rate
2.0 MHz

A/D Conversion Time
300 ns Typ.

S/H Acquisition Time
200 ns Typ.

S/H Aperture Delay
15 ns Max.

S/H Aperture Jitter
5 ps RMS Max.

S/H Feedthrough[3]
–90 dB Max.; –96 dB Typ.

Full Power Bandwidth
6 MHz Min.

Small Signal Bandwidth
8 MHz Typ.

Signal to Noise Ratio[4]
100 kHz Input @ 0 dB
86 dB Min.

540 kHz Input @ –10 dB
76 dB Min.

980 kHz Input @ –10 dB
75 dB Min.

Peak Distortion[5]
100 kHz Input @ 0 dB
–92 dB Max.

540 kHz Input @ –10 dB
–84 dB Max.

980 kHz Input @ –10 dB
–81 dB Max.

Total Harmonic Distortion[6]
100 kHz Input @ 0 dB
–86 dB Max.

540 kHz Input @ –10 dB
–79 dB Max.

980 kHz Input @ –10 dB
–76 dB Max.

THD + Noise[7]
100 kHz Input @ 0 dB
83 dB Min.

540 kHz Input @ –10 dB
75 dB Min.

980 kHz Input @ –10 dB
–72 dB

Step Response[8]
250 ns Max. to 2 LSBs

TRANSFER CHARACTERISTICS

Resolution
16 bits

Quantization Error
±0.5 LSB Max.

Integral Nonlinearity
±0.003% FSR Max.

Differential Nonlinearity
±0.75 LSB Max.

Monotonicity
Guaranteed

No Missing Codes
Guaranteed –10°C to +40°C

Offset Error
±0.1% FSR Max. (Adj. to Zero)

Gain Error
±0.1% FSR Max. (Adj. to Zero)

Noise[9]
10V p-p FSR
90 µV RMS Typ.

5V p-p FSR
65 µV RMS Typ.

STABILITY (–10°C TO +40°C)

Differential Nonlinearity TC
±1 ppm/°C Max.

Offset TC
±15 ppm/°C Max.

Gain TC
±15 ppm/°C Max.

Warm-Up Time
5 Min. Max.

Supply Rejection per % change in any supply
Offset
±15 ppm/% Max.

Gain
±15 ppm/% Max.

POWER REQUIREMENTS

±15V Supplies
14.55V Min., 15.45V Max.

+5V Supplies
+4.75V Min., +5.25V Max.

+15V Current Drain
63 mA Typ.

–15V Current Drain
54 mA Typ.

+5V Current Drain
53 mA Typ.

Total Power Consumption
2.02W Typ.

ENVIRONMENTAL & MECHANICAL

Specified Temperature Range[10]
0°C to +70°C

Storage Temperature Range
–25°C to 125°C

Dimensions
1.5" x 2.38" x 0.225"
(38.1 mm x 60.45 mm x 5.7 mm)

Shielding
Electromagnetic 6 sides,
Electrostatic 6 sides

Case Potential
Ground

NOTES:

1. All specifications guaranteed at 25°C unless otherwise noted and supplies at ±15V and +5V.
2. Reference Load to remain stable.
3. Measured with a full scale step input.
4. Signal to noise ratio represents the ratio of the RMS value of the signal to the total RMS noise below the Nyquist rate with an analysis bandwidth of DC to 1 MHz.
5. Peak distortion represents the ratio of the highest spurious frequency component below the Nyquist rate to the signal.
6. Total harmonic distortion represents the ratio of the RMS sum of all harmonics up to the 100th harmonic to the RMS value of the signal with an analysis bandwidth of DC to 1.0 MHz.
7. THD + noise represents the ratio of the RMS value of the signal to the total RMS noise below the Nyquist plus the total harmonic distortion up to the 100th harmonic with an analysis bandwidth of DC to 1.0 MHz.
8. Step response represents the time required to achieve the specified accuracies after an input full scale step change.
9. Includes noise from S/H and A/D converter.
10. The specified temperature range is guaranteed for the case temperature.

Specifications subject to change without notice.

ADC4322 SPECIFICATIONS

Input Scaling

The ADC4322 can be configured for four input voltage ranges: 0 to +10V, ±2.5V, ±5V and ±10V. The analog input range should be scaled as close as possible to the maximum input to utilize the full dynamic range of the converter. Figure 2 describes the input connections.

PIN #	4	5	6
RANGE	S/H IN 1	S/H IN2	S/H IN 3
0V to +10V	Input	Input	–5V Ref
±5V	Input	Input	SIG RTN
±2.5V	Input	Input	Input
±10V	Input	SIG RTN	SIG RTN

Figure 2. Input Scaling Connections.

Coding and Trim Procedure

Figure 4 shows the output coding and trim calibration voltages of the ADC4322 A/D converter. For two's complement operation, simply use the available B1 (MSB) instead of B1 (MSB). Refer to Figure 3 for use of external offset and gain trim potentiometers. Voltage DACs with a ±5V output can be easily utilized when digital control is required. The input sensitivity of the external offset and gain control pins is 300 ppm FSR/V.

To trim the offset of the ADC4322, apply the offset voltage shown in Figure 3 for the appropriate voltage range. Adjust the offset trim potentiometer such that the 15 MSBs are "0" and the LSB alternates equally between "0" and "1" for the unipolar ranges or all 16 bits are in transition for the bipolar ranges.

To trim the gain of the ADC4322, apply the range (+FS) voltage shown in Figure 3 for the appropriate range. Adjust the gain trim potentiometer such that the 15 MSBs are "1" and the LSB alternates equally between "0" and "1".

To check the trim procedure, apply 1/2 full scale voltage for a unipolar range or –full scale voltage for the bipolar ranges and check that the digital code is ±1 LSB of the stated code.

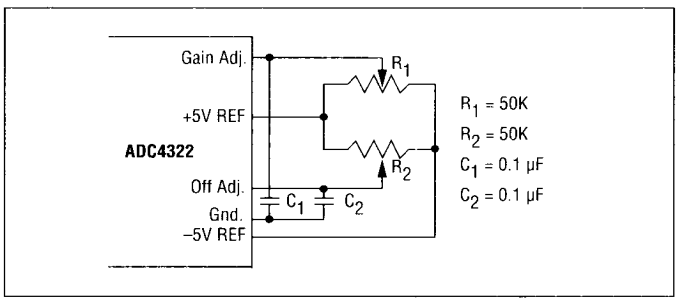

Figure 3. Offset and Gain Adjustment Circuit.

UNIPOLAR BINARY				0V TO +10V	
	MSB LSB				
+FS	1111111111111111*	=		+9.99977V	
1/2 FS	1000000000000000	=		+5.00000V	
Offset	0000000000000000*	=		+0.0000*V	
OFFSET BINARY				**±2.5V Input**	**±5V Input**
	MSB LSB				
+FS	1111111111111111*	=		+2.49989V	+4.99977V
Offset	**********	=		–0.00004V	–0.00008V
–FS	0000000000000000*	=		–2.49996V	–4.99992V
2'S COMPLEMENT				**±2.5V Input**	**±5V Input**
	MSB LSB				
+FS	0111111111111111*	=		+2.49989V	+4.99977V
Offset	**********	=		–0.00004V	–0.00008V
–FS	1000000000000000*	=		–2.49996V	–4.99992V

* denotes a 0/1 or 1/0 transition

Figure 4. Coding and Trim Calibration Table.

Layout Considerations

Because of the high resolution of the ADC4322 A/D converter, it is necessary to pay careful attention to the printed-circuit layout for the device. It is, for example, important to return analog and digital grounds separately to their respective power supplies. Digital grounds are often noisy or "glitchy" and these glitches can have adverse effects on the performance of the ADC4322 if they are introduced to the analog portions of the A/D converter's circuitry. At 16-bit resolution, the size of the voltage step between one code transition and the succeeding one for a 5V full scale range is only 76 µV. It is evident that any noise in the analog ground return can result in erroneous or missing codes. It is important in the design of the PC board to configure a low-impedance ground-plane return on the printed-circuit board. It is only at this point where the analog and digital power returns should be made common.

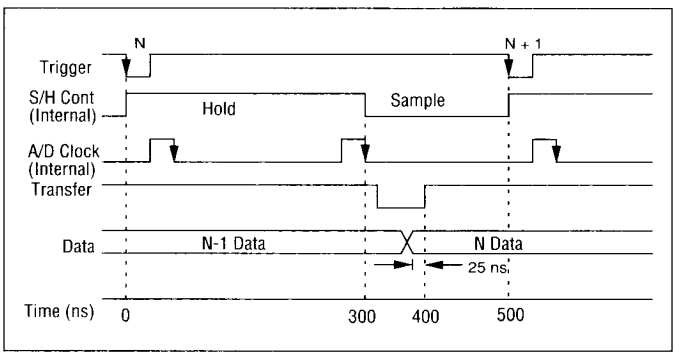

Figure 5. ADC4322 Timing Diagram.

PRINCIPLE OF OPERATION

The ADC4322 is a 16-bit sampling A/D converter with a throughput rate of 2 MHz. This converter is available in three externally configured full scale ranges of 5V p-p, 10V p-p and 20V p-p. Options are externally or user programmable for bipolar and unipolar inputs of ±2.5V, ±5V, ±10V and 0 to +10V. Two's complement format can be obtained by utilizing $\overline{B1}$ instead of B1.

To understand the operating principles of the ADC4322 A/D converter, refer to the timing diagram of Figure 5 and the simplified block diagram of Figure 6. The simplified block diagram illustrates the two successive passes in the sub-ranging scheme of the ADC4322.

The A/D converter section of the ADC4322 is factory trimmed and optimized to operate with a 10V p-p input voltage range. Scaling resistors at the S/H inputs configure the three input ranges and provide a S/H output voltage to the A/D converter of 10V p-p.

The first pass starts with a high-to-low transition of the trigger pulse. This signal places the S/H into the Hold mode and starts the timing logic. The path of the 10V p-p input signal during the first pass is through a 5:1 attenuator circuit to the 9-bit ADC with an input range of 2V p-p. At 35 ns, the ADC converts the signal and the 9 bits are latched both into the logic as the MSBs and into the 16-bit accurate DAC for the second pass.

The second pass subtracts the S/H output and the 9-bit, 16-bit accurate DAC output with the result equal to the 9-bit quantization error of the DAC, or 19.5 mV p-p. The "error" voltage is then amplified by a gain of 25.6 and is now 0.5V p-p or 1/4 the full scale range of the ADC allowing a 2-bit overlap safety margin. At approximately 300 ns, the DAC and the "error" amplifier have had sufficient time to settle to 16-bit accuracy and the amplifier "error" voltage is then digitized by the ADC with the 9-bit second pass result latched into the logic. At this time the S/H returns to the sample mode to begin acquiring the next sample.

The 1/4 full scale range in the second pass produces a 2-bit overlap of the two passes. This provides an output word that is accurate and linear to 16 bits. This method corrects for any gain and linearity errors in the amplifying circuitry, as well as the 10-bit flash A/D converter. Without the use of this overlapping correction scheme, it would be necessary that all the components in the ADC4322 be accurate to the 16-bit level. While such a design might be possible to realize on a laboratory benchtop, it would be clearly impractical to achieve on a production basis. The key to the conversion technique used in the ADC4322 is the 16-bit accurate and 16-bit linear D/A converter which serves as the reference element for the conversion's second pass. The use of proprietary sub-ranging architecture in the ADC4322 results in a sampling A/D converter that offers unprecedented speed and transfer characteristics at the 16-bit level.

The ADC4322 has a 3-state output structure. Users can enable the eight MSBs and $\overline{B1}$ with $\overline{HIBYTEN}$ and the eight LSBs with $\overline{LOBYTEN}$. (Both are active low.) This feature makes it possible to transfer data from the ADC4322 to an 8-bit microprocessor bus. However, to prevent the coupling of high frequency noise from the microprocessor bus into the A/D converter, the output data must be buffered; see Figure 11.

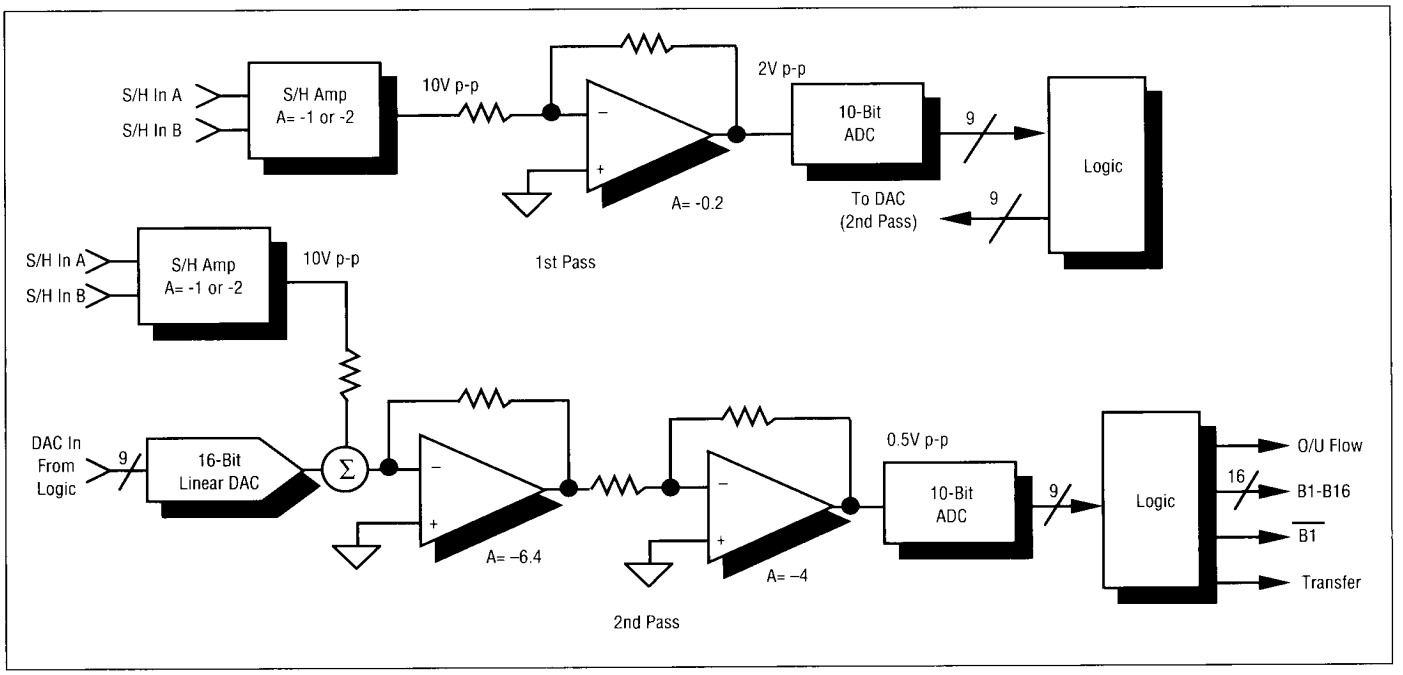

Figure 6. Operating Principle of the ADC4322.

ADC4322 PERFORMANCE TESTING

In order to guarantee that all ADC4322s shipped meet or exceed published specifications, Analogic performs a multitude of tests on each hybrid prior to shipment. Such results are then sent to the customer in conjunction with each ADC4322 as testimony of the performance results.

Amplitude Domain Testing

The Amplitude Domain Testing is performed by means of proprietary Automatic Test Equipment inclusive of a 22-bit digital-to-analog converter, whose reference is traceable to the National Institute of Standards Technology. A block diagram is outlined in Figure 7. By means of this test equipment, Analogic can test such parameters as integral linearity, differential linearity, A/D converter noise, maximum positive and negative errors, conversion time, gain error, offset error, power supply current, power supply rejection. A typical "Amplitude Domain" data sheet is shown in Figure 9. For further information on the definitions of such specifications, please refer to the "Analogic Data Conversion Systems Digest."

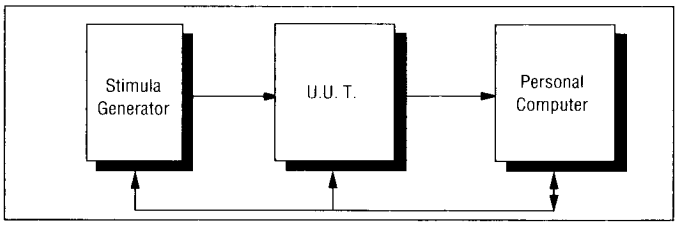

Figure 7. "Amplitude Domain" Test System.

Frequency Domain Testing

Frequency Domain Testing is performed to simulate real-time applications where a constantly varying input signal is applied to the ADC4322. A block diagram of the Analogic "Frequency Domain" test system is shown in Figure 8. As a result, a data sheet, such as the one reproduced in Figure 10, is delivered to the customer with each ADC4322.

The data sheet is divided into two sections including the nature of the input data, the type of FFT performed and the results of the FFT test. This data can be misleading if not thoroughly understood. For example, in an audio application, one of the most important parameters is the absence of aliased harmonic distortion. While harmonic distortion directly related to the fundamental does not produce audible discomfort, aliased harmonics can be very bothersome. Such characterization is not often provided or is calculated as part of the total harmonic distortion, thus, misleading the end user. Analogic definitions are summarized as follows:

Peak Distortion: Ratio, expressed in dB, between the RMS value of the highest spurious spectral component below the Nyquist rate and the RMS value of the input signal.

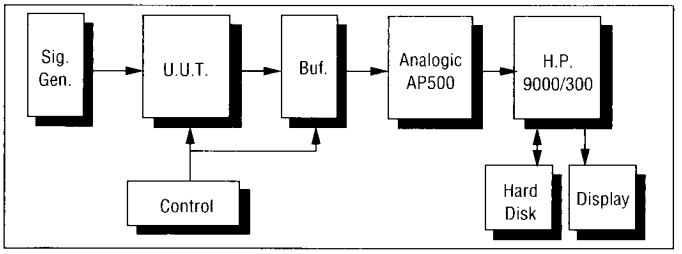

Figure 8. "Frequency Domain" Test System.

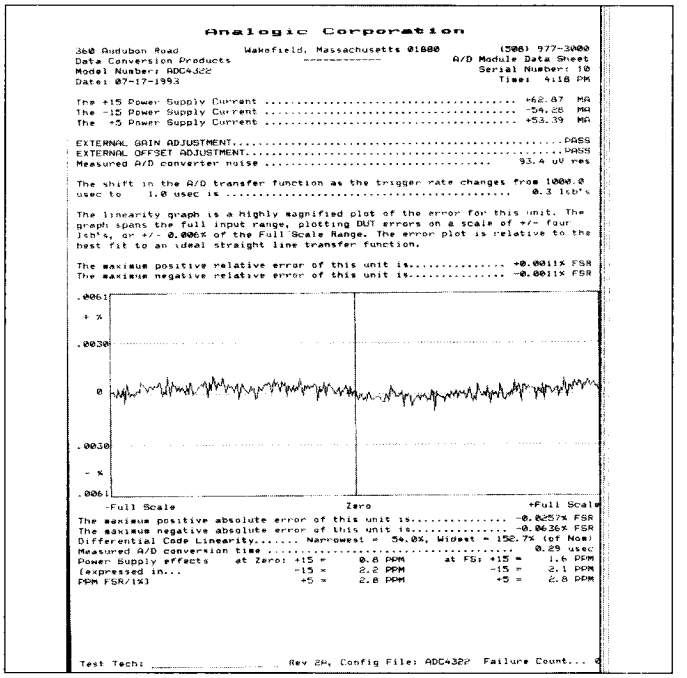

Figure 9. "Amplitude Domain" Data Sheet.

$$\text{Peak Distortion} = 20 \log \frac{\text{RMS value of max. spurious component}}{\text{RMS value of input signal}}$$

Signal to Noise Ratio: Ratio, expressed in dB, between the RMS value of the signal and the total RMS noise below the Nyquist rate.

Total Harmonic Distortion: Ratio, expressed in dB, between the RMS sum of all harmonics up to the 100th harmonic and the RMS value of the signal.

Direct Harmonic Distortion: Ratio, expressed in dB, between the RMS sum of all the components below the Nyquist rate that are harmonically related to the signal and the RMS value of the signal.

Reflected Harmonic Distortion: Ratio, expressed in dB, between the RMS sum of all aliased harmonics and the RMS value of the signal.

Note that the estimated RMS noise, based on those frequency bins not correlated with the test signal, is first removed from the harmonic frequency bins before the above distortion values are calculated.

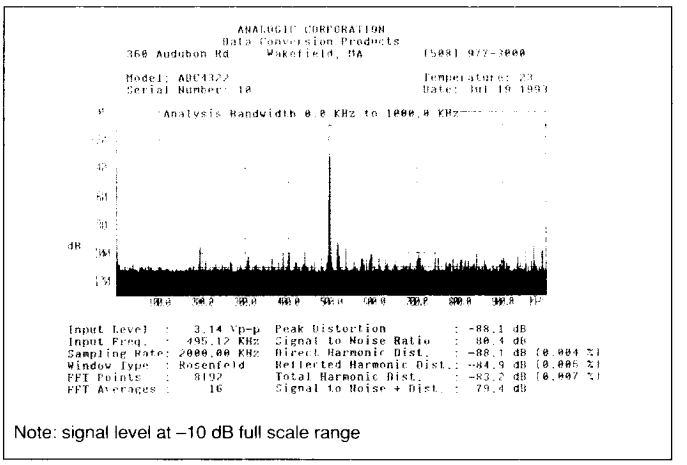

Figure 10. "Frequency Domain" Data Sheet.

Figure 11 shows a typical application circuit for the ADC4322 A/D converter: a four channel, high speed, high resolution A/D conversion system tied into an 8-bit bus structure. This circuit could be part of the front end of a medical imaging system, an ATE system or a sampling oscilloscope. The 16-bit resolution provides 96 dB dynamic range for each channel, and the 2 MHz throughput rate provides approximately 100 kHz throughput per channel. (In certain CT imaging applications, it may be possible to multiplex as many as 48 channels into the ADC4322.)

By addressing the multiplexer at the time of the ADC trigger (Figure 5), the mux and buffer settling times do not add to the system throughput rates.

For interfacing into a 16-bit bus, the Tri-state latch or digital buffers may still be required to prevent coupling of high frequency noise from the microprocessor bus into the A/D converter. Note that in Figure 11 the signal return is NOT tied to the external common ground-plane return but instead is common at a strategic point inside the ADC4322.

The ability of the ADC4322 sample-and-hold amplifier to acquire new data to within ±2 LSB after a full-scale step change at the analog input, in addition to the superb dc characteristics exhibited by the ADC4322, are the key factors is establishing this part as the ideal choice for high speed, high performance data acquisition systems.

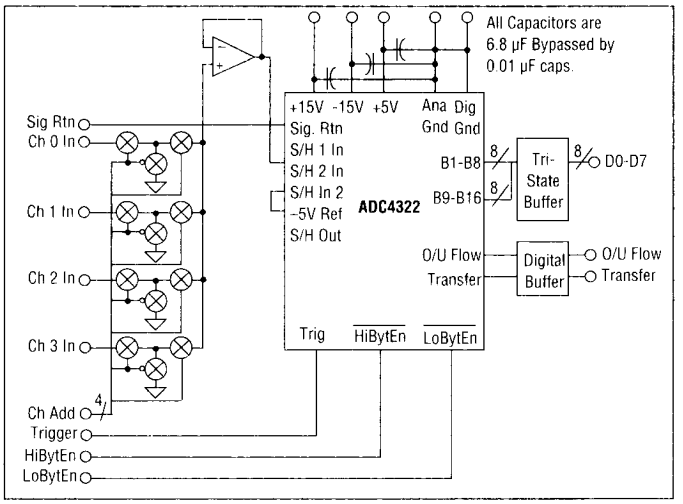

Figure 11. ADC4322 configured for: 4-CH input, 0V to +10V input range, true binary data driving an 8-bit bus.

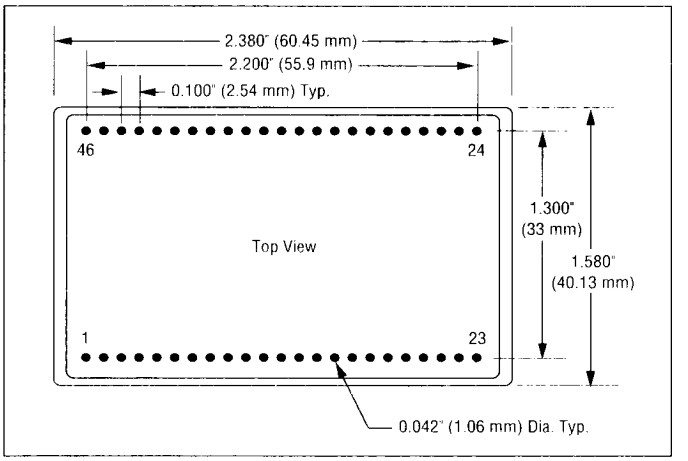

Figure 12. ADC4322 Mechanical.

PIN #		PIN#	
1	ANA RTN	46	+5V
2	+15V	45	DIG RTN
3	–15V	44	O/U FLOW
4	S/H IN 1	43	BIT 1N
5	S/H IN 2	42	BIT 1
6	S/H IN 3	41	BIT 2
7	SIG RTN	40	BIT 3
8	DNC	39	BIT 4
9	ANA RTN	38	BIT 5
10	+15V	37	BIT 6
11	–15V	36	BIT 7
12	DNC	35	BIT 8
13	EXT OFFSET ADJ	34	BIT 9
14	ANA RTN	33	BIT 10
15	EXT GAIN ADJ	32	BIT 11
16	+REF OUT	31	BIT 12
17	–REF OUT	30	BIT 13
18	ANA RTN	29	BIT 14
19	TRIGGER	28	BIT 15
20	DIG RTN	27	BIT 16
21	DIG RTN	26	TRANSFER
22	HI BYTE EN	25	+5V
23	LO BYTE EN	24	DIG RTN

Figure 13. ADC4322 Pin Assignment.

Ordering Guide

ADC4322	16-bit, 2 MHz Sampling A/D Converter
ADC4322-EB1	Evaluation Board for the ADC4322

Analogic Corporation
Data Conversion Products Group
360 Audubon Road
Wakefield, MA 01880-9863, USA
Tel: (508) 977-3000
Fax: (617) 245-1274
Technical support: (800) 446-8936

Analogic GmbH
Siemensstrasse 13
D-65205 Wiesbaden
Federal Republic of Germany
Tel: 49-6122-70060
Telex: 4064611
Fax: 49-6122-15262

Analogic Ltd.
Ascot House
Doncastle Road
Bracknell, Berks. RG12 8PE
England
Tel: 44-344-860111
Telex: 847145
Fax: 44-344-860478

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