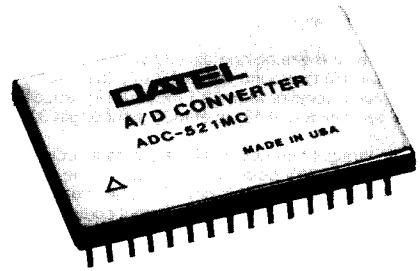
ADC-520, ADC-521
12-Bit, Ultra-Fast, Low-Power A/D Converters

FEATURES

- **12-Bit resolution**
- **800 Nanosecond maximum conversion time**
- **Pin-programmable input ranges**
- **Internal high impedance buffer**
- **Low 1.6 watts power consumption**
- **Three-state output buffers**
- **Small 32-pin DIP**
- **No missing codes**

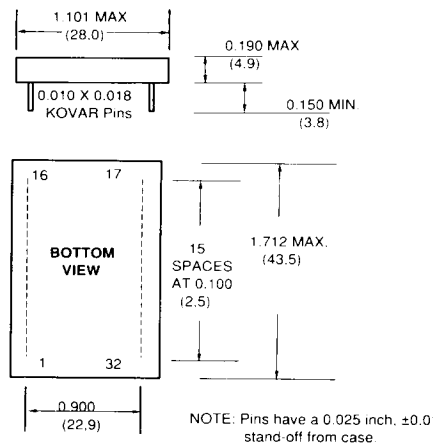


GENERAL DESCRIPTION

DATEL's ADC-520 and ADC-521 are 12-bit analog-to-digital converters with conversion speeds of up to 800 nanoseconds. Both models are identical except for the analog input voltage ranges.

The performance of these converters is based upon a digitally-correcting subranging architecture. DATEL further enhances this technology by using unique laser trimming schemes. The ADC-520 and ADC-521 are packaged in a 32-pin ceramic DIP and consume 1.6 watts.

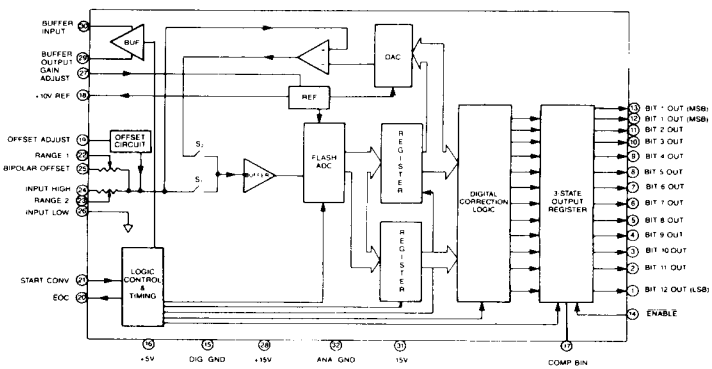
MECHANICAL DIMENSIONS
INCHES (mm)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K ohm trimming potentiometer for gain adjjustment with the wirper tied to pin 27 (ground pin 27 for operation without adjustments). Use a 20K ohm trimming potentiometer with the wiper tied to pin 19 for zero/offset adjustment (leave pin 19 open for operation without adjustment).



I/O CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	COMP BIN
2	BIT 11 OUT	18	REF. OUT (+10V dc)
3	BIT 10 OUT	19	OFFSET ADJUST
4	BIT 9 OUT	20	EOC
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	RANGE 1
7	BIT 6 OUT	23	RANGE 2
8	BIT 5 OUT	24	INPUT HIGH
9	BIT 4 OUT	25	BIPOLAR OFFSET
10	BIT 3 OUT	26	INPUT LOW
11	BIT 2 OUT	27	GAIN ADJUST
12	BIT 1 OUT (MSB)	28	+15V
13	BIT 1 OUT (MSB)	29	BUFFER OUTPUT
14	ENABLE	30	BUFFER INPUT
15	DIGITAL GROUND	31	-15V
16	+5V	32	ANALOG GROUND

2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass all the analog and digital supplies and the +10V reference (pin 18) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 18) to analog ground (pin 32) the same way.

4. Obtain straight binary/offset binary output coding by tying $\overline{\text{COMP BIN}}$ (pin 7) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the COMP BIN pin to ground. In the bipolar mode, two's complement output coding is available by using the $\overline{\text{MSB}}$ output (pin 13). The COMP BIN signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. Enable the three-state outputs by connecting $\overline{\text{ENABLE}}$ (pin 14) to a logic 0 (low). The $\overline{\text{ENABLE}}$ signal has no effect on $\overline{\text{MSB}}$ (pin 13) which is not a three-state output and therefore is not controlled by the enable pin.

6. Satisfy high-speed drive requirements of the ADC-520, -521 with a wide-bandwidth, low output impedance input source such as DATEL's SHM-45 sample-and-hold or AM-1435 amplifier.

7. The ADC-520,-521 provide an internal buffer amplifier. Using this buffer provides an inut impedance of 10^{12} ohms, allowing the A/D to be driven from a high impedance source or directly from an analog multiplexer. When using the input buffer, allow a delay equal to its settling time between input level change and the negative going edge of the START CONVERT pulse. If the buffer is not required, its input should be connected to analog ground to avoid introducing noise into the converter.

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 28)	0 to +18	Volts dc
-15V Supply (Pin 31)	0 to -18	Volts dc
+5V Supply (Pin 16)	-0.5 to +7.0	Volts dc
Digital Inputs (Pins 14, 17, 21)	-0.3 to +6.0	Volts dc
Analog Input (Pin 24)	-15 to +15	Volts dc
Lead Temp.(10 Sec.)	300	°C

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Range				
(ADC-520)	–	±10	–	Volts dc
	–	0 to +10	–	Volts dc
	–	0 to +20	–	Volts dc
	–	0 to -20	–	Volts dc
(ADC-521)	–	±2.5	–	Volts dc
	–	0 to +5	–	Volts dc
Input Impedance				
(ADC-520)				
Unipolar:	1.75	2.5	–	K Ohms
Bipolar:	3.75	5.0	–	K Ohms
(ADC-521)				
Unipolar:	2.0	2.5	–	K Ohms
Bipolar:	1.6	2.0	–	K Ohms
Input Capacitance	–	–	50	pf
Buffer Amplifier				
Input Voltage	+10	–	–	Volts dc
Input Impedance	–	10^{12}	–	Ohms
Settling Time	–	700	1000	nSec.
DIGITAL INPUTS				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5	µA
Logic Loading "0"	–	–	-200	µA
OUTPUTS				
Resolution	12	–	–	Bits
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference Voltage, +25 °C	9.98	10.0	10.02	Volts dc
Drift	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA
Output Coding				
(Pin 17 HI)	Straight binary/offset binary			
(Pin 17 Low)	Complementary binary Complementary offset binary			
(Note 4)	Two's complement			
(Note 4)	Complementary two's complement			
PERFORMANCE				
Integral Non-Linearity				
+25 °C	–	–	±1/2	LSB
0 °C to +70 °C	–	–	±1/2	LSB
Integral Non-Lin. Tempco	–	±3	±8	ppm/ °C
Differential Non-Linearity				
+25 °C	–	–	±1/2	LSB
0 °C to +70 °C	–	–	±1/2	LSB
Differential Non-Lin. Tempco	–	–	±2.5	ppm/ °C
Full Scale Absolute Accuracy				
+25 °C	–	±3	±8	LSB
0 °C to +70 °C	–	±4	±14	LSB
Unipolar Operation				
Zero Error ①	–	±1	±5	LSB
Zero Tempco	–	±13	±25	ppm/ °C
Zero Adjust Range	±5	–	–	LSB

Bipolar Operation	MIN.	TYP.	MAX.	UNITS
Zero Error ①	–	±1	±5	LSB
Zero Tempco	–	±2	±5	ppm/ °C
Zero Adjust Range	±5	–	–	LSB
Offset Error ①	–	±2	±5	LSB
Offset Tempco	–	±17.5	±35	ppm/ °C
Offset Adjust Range	±5	–	–	LSB
Gain Error ①	–	±2	±5	LSB
Gain Tempco	–	±17.5	±35	ppm/ °C
Gain Error Adjust Range	±5	–	–	LSB
Conversion Times				
+25 °C	–	–	800	nSec.
0 °C to +70 °C	–	–	850	nSec.
Harm. Distort. (-FS) ②				
+25 °C		-72 dB min.		
0 to +70 °C		-72 dB min.		
-55 to +125 °C		-65 dB min.		
No Missing Codes (12 Bits)		Over the Operating Temperature Range		
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+52	+65	mA
-15V dc Supply	–	-36	-45	mA
+5V dc Supply*	–	+66	+70	mA
Power Dissipation	–	1.6	1.9	Watts
Power Supply Rejection	–	–	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range	0	–	+70	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	32-Pin hermetic sealed, ceramic DIP			
Pins	0.010 x 0.018 inch Kovar			
Weight	0.42 ounces (12 grams)			

* +5V power usage at 1 TTL logic loading per data output bit.
① Specifications cited are at +25 °C. See Technical Note 1 for further information.
② With DATEL SHM-45, see Figure 3.

INPUT CONNECTIONS

Table 2a. ADC-520 Input Connections

INPUT RANGE	INPUT PIN W/O BUFFER	INPUT PIN WITH BUFFER	CONNECT
±10V dc	Pin 24	Pin 30, tie 29 to 24	Pin 18 to 25
0 to +10V dc	Pin 24	Pin 30, tie 29 to 24	Pin 24 to 25
0 to +20V dc	Pin 24	DO NOT USE	Pin 26 to 25
0 to -20V dc	Pin 25	DO NOT USE	Pin 18 to 24, 22 to 23 to 24

Table 2b. ADC-521 Input Connections

INPUT RANGE	INPUT PIN W/O BUFFER	INPUT PIN WITH BUFFER	CONNECT
±2.5V dc	Pin 24,22,23	Pin 30, tie 29 to 24	Pin 25 to 18
0 to +5V dc	Pin 24,22,23	Pin 30, tie 29 to 24	Pin 25 to 26

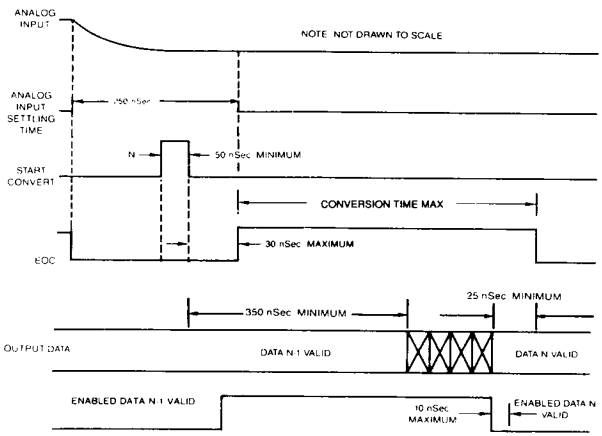


Figure 2. ADC-520, ADC-521 Timing Diagram

TIMING

Figure 2 shows the relationship between the various input signals. The timing cited applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3 and Tables 2a and 2b for the appropriate full-scale range (FSR). Apply a pulse of 50 nanoseconds minimum to the START CONVERT input (pin 21) at a rate of 500 KHz. This rate reduces flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments - Apply a precision voltage reference source between the analog input and ground. Refer to Tables 2a and 2b for the correct input pin. Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 17) tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with the COMP BIN tied low (complementary binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with COMP BIN (pin 17) tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN (pin 17) tied low (complementary offset binary).

Two's complement and complementary two's complement requires the use of MSB (pin 13) versus MSB (pin 12) as given for offset binary or complementary offset binary respectively.

3. Full-Scale Adjustment - Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for COMP BIN (pin 17) tied high or between 0000 0000 0001 and 0000 0000 0000 for COMP BIN tied low. Two's complement and complementary two's complement respectively requires using MSB, pin 13.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 4 and 5.

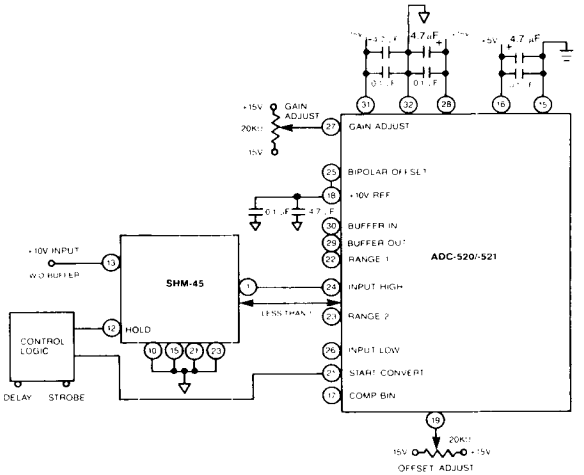


Figure 3. ADC/SHM Connection Diagram

Table 3. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS -1 1/2 LSB
0 to +5V	+0.610 mV dc	+4.9971V dc
0 to +10V dc	+1.22 mV dc	+9.9963V dc
0 to +20V dc	+2.44 mV dc	+19.9927V dc
0 to -20V dc	-2.44 mV dc	-19.9927V dc
+10V dc	+2.44 mV dc	+9.9927V dc
+2.5V dc	+0.610 mV dc	+2.4982V dc

Table 4. Output Coding for Unipolar Operation

UNIPOLAR SCALE	INPUT RANGES,VOLTS dc			OUTPUT CODING			
				STRAIGHT BINARY		COMP. BINARY	
	0 to +5V	0 to +10V	0 to +20V	MSB	LSB	MSB	LSB
+FS-1LSB	+4.9988V	+9.9976V	+19.9951V	1111 1111 1111		0000 0000 0000	
7/8 FS	+4.3750V	+8.7500V	+17.500V	1110 0000 0000		0001 1111 1111	
3/4 FS	+3.7500V	+7.5000V	+15.000V	1100 0000 0000		0011 1111 1111	
1/2 FS	+2.5000V	+5.0000V	+10.000V	1000 0000 0000		0111 1111 1111	
1/4 FS	+1.2500V	+2.5000V	+5.0000V	0100 0000 0000		1011 1111 1111	
1/8 FS	+0.0024V	+1.2500V	+2.5000V	0010 0000 0000		1101 1111 1111	
1 LSB	+0.0012V	+0.0024V	+0.0048V	0000 0000 0001		1111 1111 1110	
0	0.0000V	0.0000V	0.0000V	0000 0000 0000		1111 1111 1111	

Table 5. Output Coding for Bipolar Operation

BIPOLAR SCALE	INPUT RANGES,VOLTS dc		OUTPUT CODING				
			OFFSET BINARY		COMP TWO'S COMP	TWO'S COMP.	
	±2.5V	±10V	MSB	LSB	MSB LSB	MSB	LSB
+FS -1 LSB	+2.4988V	+9.9951V	1111 1111 1111		1000 0000 0000	0111 1111 1111	
+3/4 FS	+1.8750V	+7.5000V	1110 0000 0000		1001 1111 1111	0110 0000 0000	
+1/2 FS	+1.2500V	+5.0000V	1100 0000 0000		1011 1111 1111	0100 0000 0000	
0	0.0000V	0.0000V	1000 0000 0000		1111 1111 1111	0000 0000 0000	
-1/2 FS	-1.2500V	-5.0000V	0100 0000 0000		0011 1111 1111	1100 0000 0000	
-3/4 FS	-1.8750V	-7.5000V	0010 0000 0000		0101 1111 1111	1010 0000 0000	
-FS +1 LSB	-2.4988V	-9.9951V	0000 0000 0001		0111 1111 1110	1000 0000 0001	
-FS	-2.5000V	-10.000V	0000 0000 0000		0111 1111 1111	1000 0000 0000	

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
ADC-520MC	0 to +70 °C
ADC-521MC	0 to +70 °C

Order PC board mounting receptacle through AMP Inc. part #3-331272-8 (Component Lead Socket), 32 required.