ADVANCED ANALOG

A Division of intech

ADC5245

1 MHz, 12-Bit A/D CONVERTER HYBRID

DESCRIPTION

Less than one microsecond is all the time required for the ADC5245/5246 to reliably convert an analog input signal into a precise digital output word with 12-bits of resolution. This speed and precision combination in conjunction with the units small size make them truly state-of-the-art analog-to-digital converters.

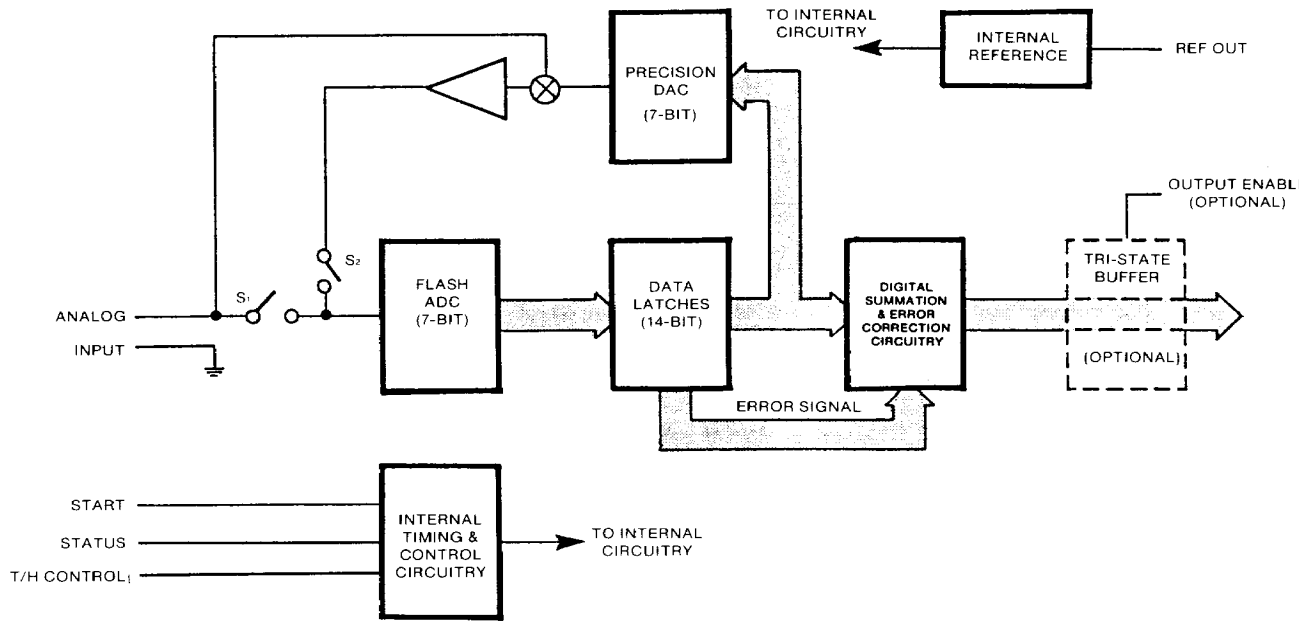
These hybrid converters are complete with internal timing/control circuitry and precision reference. They operate with full scale input signal ranges of 0 to +5V (ADC5245) or ±2.5V (ADC5246) and provide TTL compatible digital outputs. The converters have an internally generated signal to control an input track and hold amplifier and are available with optional tri-state output buffers for data bus applications. They exhibit excellent performance characteristics at normal operating temperatures and very good performance (with no missing codes) over extended temperature ranges. The units are packaged in a standard 40-pin DIP and are available with MIL-STD-883 Method 5008 screening.

The units are an ideal converter for applications requiring both high accuracy and conversion speed and where package size and reliability are a major concern.

FEATURES

- **900 ns conversion time**
  1 MHz throughput guaranteed
- **Small 40-pin DIP**
- **TTL/CMOS compatible**
- **Generates a control signal for input T/H amplifier**
- **Tri-state outputs**
- **Military screening**

BLOCK DIAGRAM



SPECIFICATIONS

SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V unless otherwise indicated)[1]

	Min.	Typ.	Max.	Units
RESOLUTION		12		Bits
CONVERSION TIME[8]			900	ns
ANALOG INPUT				
Voltage Range - ADC5245		0 to +5		V
ADC5246		±2.5		V
Input Impedance		2		KΩ
Capacitance		20		pF
ACCURACY				
Absolute[4]	±0.05		±0.15	% FSR[3]
Integral Linearity Error		±¼	±1	LSB
Full Temp Range[1]		±½		LSB
Differential Linearity			±1	LSB
No Missing Codes Over Full Temp Range[1]				
OFFSET (Unipolar)[5] ADC5245	±0.05		±0.10	% FSR
Full Temp Range			±0.15	% FSR
TEMPCO		±10		ppm/°C
ZERO (Bipolar)[5] ADC5246	±0.05		±0.1	% FSR
Full Temp Range			±0.2	% FSR
TEMPCO		±10		ppm/°C FSR
GAIN[6]	±0.05		±0.1	%
Full Temp Range		0.3		%
Tempco		±20		ppm/°C FSR
CONTROL INPUTS				
Logic Levels "1"	+2			V
"0"			+0.8	V
Loading[2]		0.2		μA
Start Convert[9]	50			ns
Pulse width				
(active on logic "1" to "0" edge)				
Output Enable				
Active State		Logic "0"		
Output Delay			70	ns
DIGITAL OUTPUTS				
Data, status, T/H control				
Logic Levels "1"	3.9			V
"0"			0.26	V
Output drive - Logic "1"	-4			mA
Logic "0"	4			mA
Coding[7] — Unipolar (ADC5245)		Binary		
— Bipolar (ADC5246)		Offset Binary		
Status output				
Converter busy		Logic "1"		
T/H control				
Track command		Logic "0"		
Hold command		Logic "1"		
REFERENCE OUTPUT	4.90	+5.00	5.10	V
Current			5	μA
Tempco		±10		ppm/°C
POWER SUPPLIES				
+15V Supply				
Voltage		+15 ±0.45		V
Absolute Max	-0.5		+18	V
Current		50		mA
-15V Supply				
Voltage		-15 ±0.55		V
Absolute Max	+0.5		-18	V
Current		55		mA
+5V Supply				
Voltage		+5 ±0.25		V
Absolute Max	-0.5		+7	V
Current		120		mA
POWER CONSUMPTION		2	2.7	W
TEMPERATURE				
Operational (case)	0		+70	°C
Storage	-65		+150	°C

Consult factory for devices with mil screening.

ABSOLUTE MAXIMUM RATINGS	
Operating Temperature Range	-55°C to +125° (case)
Specified Temperature Range ADC5245/A	0°C to +70° (case)
Storage Temperature Range	-65°C to +150°C
+15V Supply (+V_{CC}, Pin 9)	-0.5 to +18 Volts
-15V Supply (-V_{CC}, Pin 3)	+0.5 to -18 Volts
+5V Supply (+V_{dd}, Pins 15, 22, 39)	-0.5 to +7 Volts
Digital Inputs (Pins 36 and 37)	-0.5 to +5.5 Volts
Analog Input (Pin 1):	-1 to +6 Volts (ADC5245)
	-3.5V to +3.5V (ADC5246)

NOTES:

1. Drift specifications apply over each device's specified temperature range as selected by part number suffix.
2. One LS TTL load is defined as sinking 20μA with a logic "1" applied and sourcing 0.4mA with a logic "0" applied.
3. FSR = Full Scale Range. FSR = 5 volts. For a 12-bit converter, 1LSB = 0.024% FSR.
4. Full Scale Absolute Accuracy Error is defined as the difference between the actual and the ideal input voltage at which the 1111 1111 1110 to 1111 1111 1111 digital-output transition occurs. It includes offset, gain, linearity and noise errors and encompasses the drifts of those errors when specified over temperature.
5. Unipolar offset error is defined for the ADC5245 and ADC5245A as the difference between the actual and ideal input voltage at which the 0000 0000 0000 to 0000 0000 0001 transition occurs.
6. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000. Initial gain error is adjustable to zero with an external potentiometer.
7. See Output Coding table for details.
8. Conversion time is defined as the width of the converter's status output pulse. The combination of 50nsec start convert pulses and 900nsec status pulses permits minimum 1MHz conversion rates. See Timing Diagram.
9. Actual conversion process is initiated on the falling edge of the start convert signal. See Timing Diagram.

DIGITAL OUTPUT CODING

Analog Input		Digital Output	
ADC5245	ADC5246	MSB	LSB
+4.9988	+2.49988	1111 1111 1111	
+4.9976	+2.49976	1111 1111 1110	
+2.5012	+0.0012	1000 0000 0000	
+2.5000	0.0000	0000 0000 0000	
+2.4988	-0.0012	0111 1111 1110	
+0.0012	-2.4988	0000 0000 0000	
0.0000	-2.5000	0000 0000 0000	

THEORY OF OPERATION

A unique state-of-the-art conversion method known as the subranging technique is used in the ADC5245/5246. This method makes it possible for the unit to accomplish its highly accurate analog-to-digital conversions within the very short time span of less than one microsecond.

The conversion sequence is initiated when a start convert pulse goes from logic "1" to logic "0". The analog input signal is connected to the 7 bit flash ADC through "S_1" - see Block Diagram. This signal is converted to a digital word, almost instantaneously. This is done with only 7 bits of resolution. This word is latched into the first seven positions of a 14-bit latch circuit and is also connected to the inputs of a precision DAC. The precision DAC has a very high accuracy/linearity but only has 7 bits of resolution. Therefore, the signal at the output of the DAC is equal to the original input signal, with only 7 bits of accuracy.

As the Block Diagram shows, this signal is summed with the original analog input signal at the input to an operational amplifier. This means that the input to the amplifier is a signal which is equal to the difference between the analog input signal and another signal which is similar to the first, but with an error caused by the fact that the A/D conversion that was made had only 7 bits of resolution.

In the next conversion sequence, "S_1" is opened and "S_2" connects the amplified error signal (described above) to the input of the flash ADC. The A/D now makes another conversion. In this sequence, the output of the A/D is latched in the other seven positions of the 14-bit latch.

The latch now contains two 7 bit words. One is an equivalent of the analog input signal, but with only 7 bits of accuracy. The other is an equivalent of the error signal caused by the fact that the original conversion was only 7 bits accurate. These two words are connected to the digital summing and error correction circuitry.

The digital summation and error correction circuitry is designed to combine the two 7 bit words (described above) in such a way that a 12 bit word is generated which is a very accurate representation of the magnitude of the original analog input. This word is connected to the output pins, or if specified (optional), to the output through a tri-state buffer.

The Timing Diagram shows the timing sequences between the inputs and outputs of the ADC5245/5246. The times are referenced to the start convert pulse.

Within 25n nsec after the start convert, pulse goes from logic "1" to a logic "0". The T/H control output goes to logic "1" generating a hold command for a track and hold amplifier at the input. This output will maintain this state for approximately 700 nsec to allow the amplifier to hold a constant input to the A/D while the conversion is made.

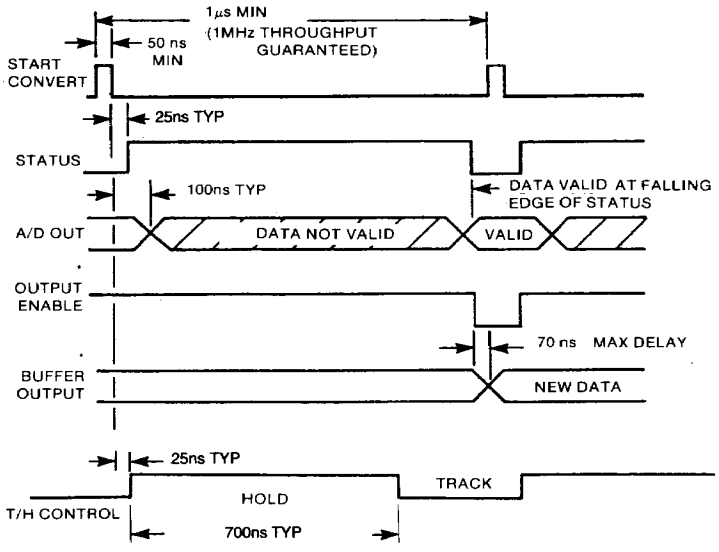
In approximately 25 nsec after the start convert goes low the status line goes to a logic "1" indicating that the conversion cycle is in process. Data from the previous conversion is still valid for 100 nsec after the new conversion is initiated. After that, the data output is changing and is not valid for the remainder of the conversion cycle unless the optional tri-state buffers are used. If these buffers are employed, the data will remain valid until the conversion cycle is completed and the new data is available.

After the second 7 bit conversion is made by the flash ADC, as described above, and the two 7 bit words are latched into the 14 bit latch circuit, the T/H control goes back low. This permits the track and hold amplifier to once again track the input signal in preparation for the next conversion cycle.

After the conversion cycle is completed and the new data is available (within 900 nsec) the status line goes low and the new data at the output of the A/D is now valid. If the optional tri-state buffers are used the status signal may be used to generate an output enable command to latch the new data into the buffers. If this is done, the new data will be valid 70 nsec later.

At this point, a new start convert pulse may be applied and next conversion cycle initiated.

TIMING DIAGRAM



PIN DESCRIPTION

ANALOG INPUT (Pin 1)

The analog signal to be converted should be connected to this pin. The full scale operating range for the input signal is from 0 to +5V for the ADC5245 and -2.5V to +2.5V ADC5246. This signal should be held constant during the conversion period and is normally supplied from the output of a track and hold amplifier. (See Theory of Operation section.)

Care should be exercised to prevent coupling or inducing unwanted signals or noise into the input signal. It should be noted that a noise spike of only six hundred microvolts is equal to one-half of an LSB. Long unshielded input leads or traces on input leads adjacent to logic or power circuits should be avoided. If it is necessary to route the input through a noisy environment, shielding/or filtering should be used.

The input impedance to these converters is 2KΩ with a capacitance of 20pF. Most track and hold or buffer amplifiers will drive this input with no problem. However, if the input signal is supplied by another source, it should have sufficient drive capability.

REFERENCE (Pin 16)

The internal reference voltage for the converter is connected to this pin and is available for external use. However, caution should be used when connecting external circuitry to it. It is a reference source only and will not withstand much of a load. If more than a 5μA load is needed, an external buffer with a high input impedance should be used. Any loading on the reference will result in a degradation of the accuracy and linearity performance specifications of the converter.

If it is desired to use a system reference to operate the converter, the external source may be connected directly to this pin. For optimum converter accuracy (absolute) this external reference voltage should match the internal voltage. The relative accuracy of the converter will be directly proportional to the accuracy and stability of the external source. The overall system accuracy may be optimized by adjusting this voltage.

TRACK AND HOLD CONTROL (Pin 20)

This output is generated by the control circuitry within the ADC5245/5246 and provides a convenient signal to control a track and hold amplifier used at the input to the converter. Within 18ns after the start convert signal goes low this output will go to logic "1" providing a "HOLD" command. When the second "flash conversion" step is completed within the converter (see Theory of Operation) and the information is latched in data latches (see Block Diagram) this output will go low and allow the track and hold amplifier to "TRACK" the input analog signal once more. Please note that this signal provides no track to hold settling time for the T/H. See Figure 1 for circuitry required to provide T/H settling time.

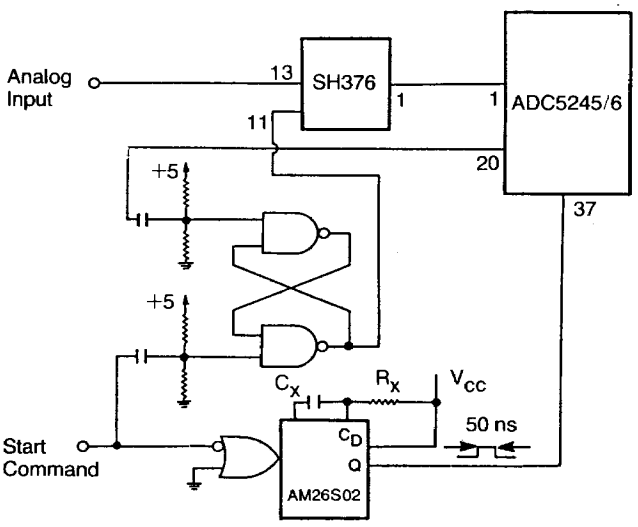


Figure 1

DATA OUTPUTS (Pins 23-24)

The digital output word from the converter is available on these pins. The data is not valid during the units' conversion cycle but is valid when the status line goes low (see the Timing Diagram). For units with the tri-state buffer output option, the data is valid when the enable input is driven to logic "0". as described under Output Enable.

The output coding is binary for the ADC5245 and offset binary for the ADC5246 (see the Digital Output Coding Table). The output pins have a drive capability of 10 LSTTL loads.

START CONVERT (Pin 36)

This input requires a positive pulse (TTL level) to initiate the conversion process. The pulse must stay positive for at least 50ns. Then on the falling edge, the conversion cycle is started (see the Timing Diagram.) Once the conversion is initiated, this input may be taken high again in preparation for the next cycle. The loading for this input is one LSTTL load.

OUTPUT ENABLE (Pin 37)

This input applies to the ADC5245A and ADC5246A models only. It is open on the other models. Its purpose is to transfer data from the output of the A/D circuitry within the unit to the output pins. A logic "0" on this input will execute this transfer while a logic "1" will disconnect the outputs (high output impedance.) It is normally taken low at the same time the status output goes low because the conversion cycle is complete at that time and the data is valid (see Timing Diagram.) It may be held low as long as required. However, in many applications it is wired to the status output pin and goes high again when the next conversion cycle starts.

STATUS OUTPUT

The falling edge of the start convert cycle will set the EOC output to logic "1" and it will remain high during conversion. It returns to logic "0" at completion of the conversion cycle. Digital output data is valid on the falling edge of status and remains valid for approximately 100nsec after start convert goes low, thus initiating the next conversion.

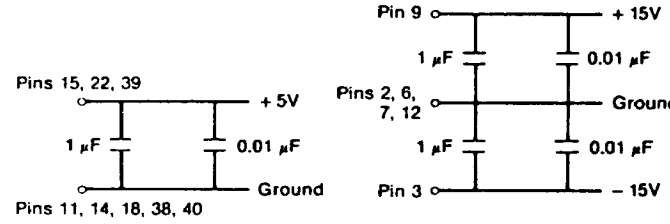
HANDLING OF GROUNDS

Layout and decoupling techniques: Analog ground pins 2, 6, 7 and 12 are not internally connected to digital ground pins 11, 14, 18, 38 and 40. They should be connected externally as directly or close to the package as possible. The ground pins must be connected to the system analog ground, preferably through a large ground plane under the package.

To run the grounds separately, connect a 0.01μF ceramic capacitor between the analog and digital pins.

Power supplies should be decoupled by using high frequency bypass capacitors. An optimum configuration is achieved by using 1μF capacitors in parallel with 0.01μF ceramic capacitors.

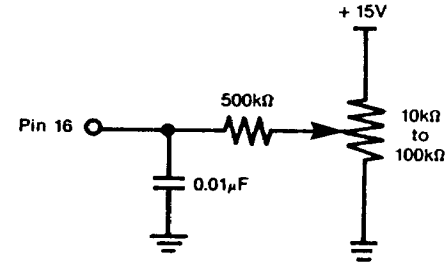
In a heavy EMI environment, a 0.1μF capacitor can be connected from pin 16 to analog ground and will provide additional protection.



REFERENCE IN/OUT, GAIN ADJUST

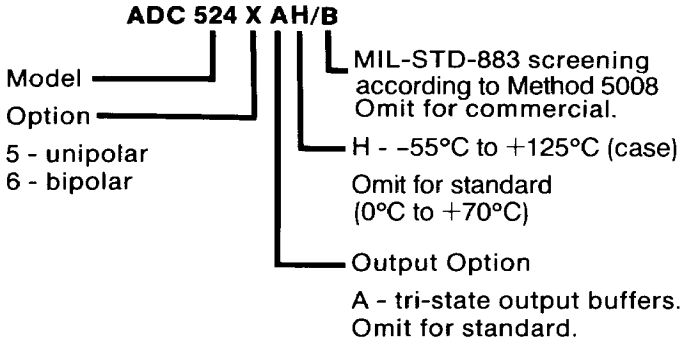
Pin 16. The ADC5245's internal +5V±2% reference can be brought out and used to drive external loads. When utilized for this purpose, pin 16 must be buffered with a FET input device. If more than 5μA is drawn from the internal reference, this will affect linearity and accuracy. This pin can also be used as REF IN if it is desirable to operate the ADC5245 from an external reference.

To use for gain adjustment, use a 10KΩ to 100KΩ trimming potentiometer and a 500KΩ series resistor. The series resistor should be ±20% carbon composition minimum. To minimize drift with temperature, use a multiturn potentiometer w/a TCR of 100 PPM/°C or less. Then apply the analog input voltage at the ideal digital output transition position (1111 1111 1110 to 1111 1111 1111) and adjust until transition is accomplished.

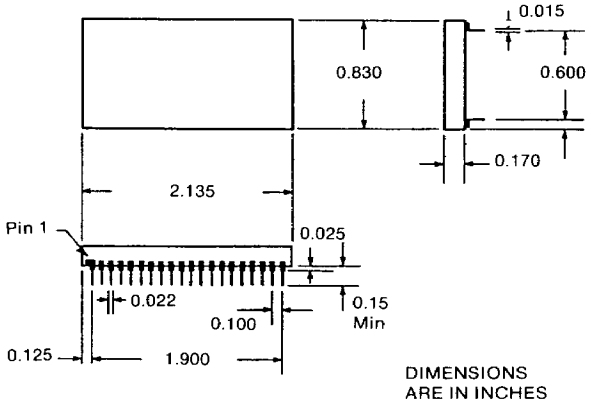


Gain Adjust Range = ±0.2% FSR

PART NUMBER



MECHANICAL OUTLINE



PIN DESIGNATIONS

1	Analog Input	40	Digital Ground
2	Analog Ground	39	+5V Supply
3	-15V Supply	38	Ditital Ground
4	Test Point (N/C)	37	N/C (Output Enable)
5	Test Point (N/C)	36	Start Convert
6	Analog Ground	35	N/C
7	Analog Ground	34	Bit 1 (MSB)
8	N/C	33	Bit 2
9	+15V Supply	32	Bit 3
10	Test Point N/C	31	Bit 4
11	Digital Ground	30	Bit 5
12	Analog Ground	29	Bit 6
13	(N/C)	28	Bit 7
14	Digital Ground	27	Bit 8
15	+5V Supply	26	Bit 9
16	Reference Output	25	Bit 10
17	Status (E.O.C.)	24	Bit 11
18	Digital Ground	23	Bit 12 (LSB)
19	(N/C)	22	+5V Supply
20	T/H Control	21	Test Point (N/C)

Note: Test points are connected to internal circuitry and should not be externally connected. Pin 37 is for 3-state output buffer option. It is N/C in standard ADC5245.

ADVANCED ANALOG

A Division of intech

MIL-STD-1772
Certified

2270 MARTIN AVENUE, SANTA CLARA, CALIFORNIA 95050-2781
TELEPHONE (408) 988-4930 TWX 910-338-2213

2001