PI74LPT646
PI74LPT652

Fast CMOS 3.3V 8-Bit Registered Transceiver

Product Features

- Compatible with LCX™ and LVT™ families of products
- Supports 5V tolerant mixed signal mode operation
  - Input can be 3V or 5V
  - Output can be 3V or connected to 5V bus
- Advanced low power CMOS operation
- Excellent output drive capability:
  Balanced drives (24 mA sink and source)
- Low ground bounce outputs
- Hysteresis on all inputs
- Industrial operating temperature range: –40°C to +85°C
- Packages available:
  – 24-pin 173-mil wide plastic TSSOP (L)
  – 24-pin 150-mil wide plastic QSOP (Q)
  – 24-pin 150-mil wide plastic TQSOP (R)
  – 24-pin 300-mil wide plastic SOIC (S)

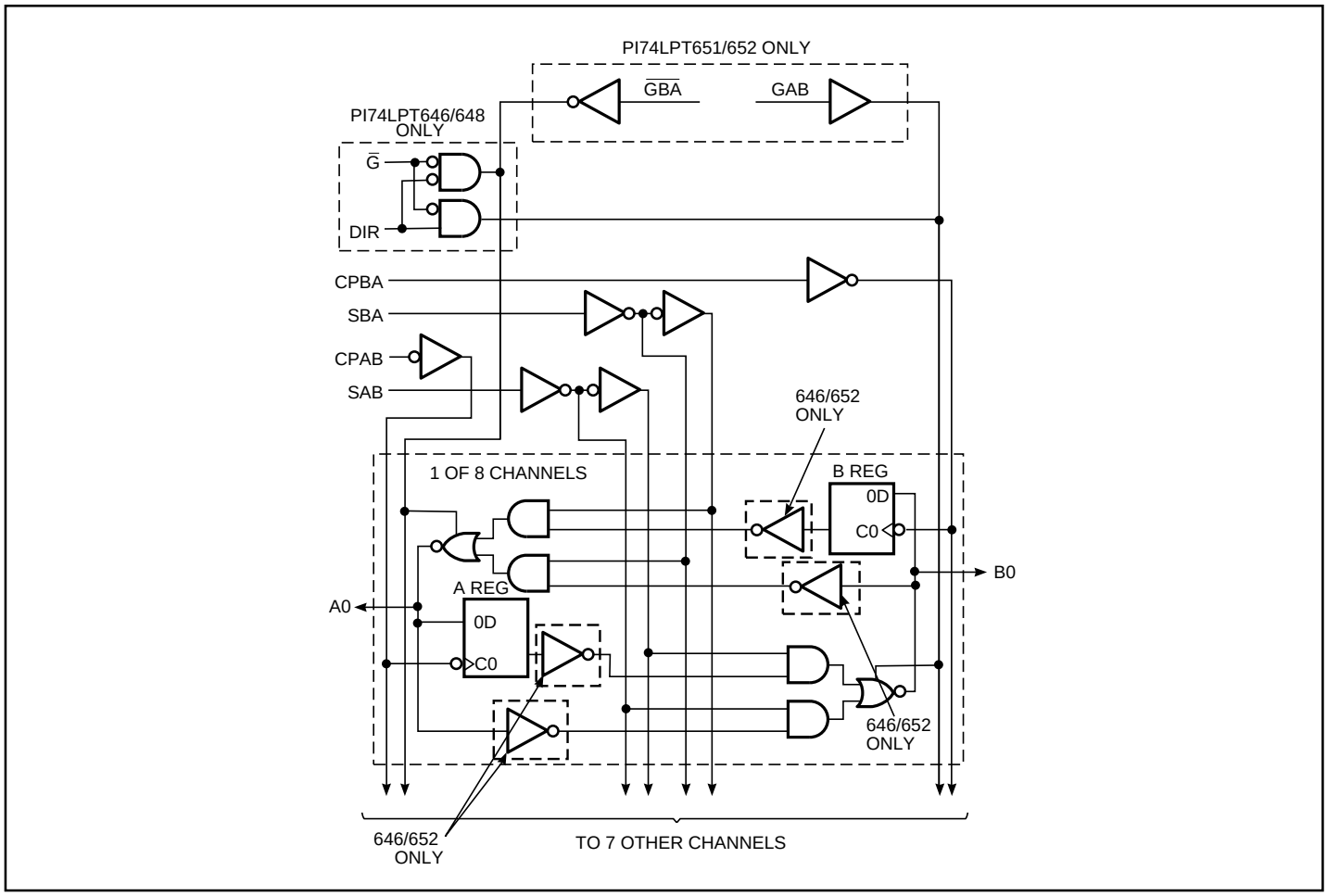
Product Description

Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

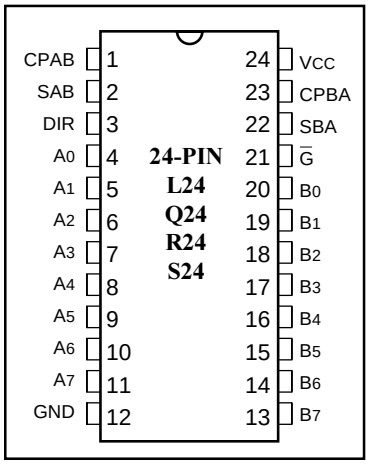
The PI74LPT646 and PI74LPT652 are designed with a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The PI74LPT652 utilizes GAB and $\overline{GBA}$ signals to control the transceiver functions. The PI74LPT646 utilizes the enable control ($\overline{G}$) and direction pins (DIR) to control the transceiver functions. SAB and SBA control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The PI74LPT646 and PI74LPT652 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

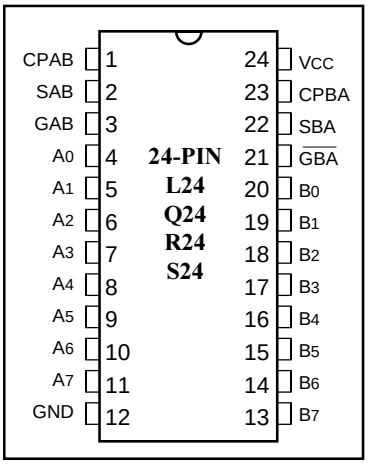
Logic Block Diagram



PI74LPT646 Product Pin Configuration



PI74LPT652 Product Pin Configuration



Product Pin Description

Pin Name	Description
A0-A7	Data Register A Inputs Data Register B Outputs
B0-B7	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs (LPT646)
GAB, $\overline{GBA}$	Output Enable Inputs (LPT652)
GND	Ground
VCC	Power

PI74LPT646 Truth Table

	Inputs						DATA I/O[2]	
Function/Operation	**$\overline{G}$**	**DIR**	**CPAB**	**CPBA**	**SAB**	**SBA**	**A0-A7**	**B0-B7**
Isolation	H	X	H or L	H or L	X	X	Input	Input
Store A and B Data	H	X	↑	↑	X	X		
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	L	H	X	X	L	X	Input	Output
Stored A Data to B Bus	L	H	H or L	X	H	X		

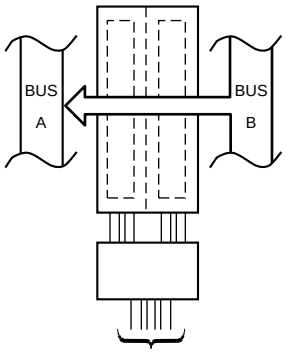
PI74LPT652 Truth Table

	Inputs						DATA I/O[2]	
Function/Operation	**GAB**	**$\overline{GBA}$**	**CPAB**	**CPBA**	**SAB**	**SBA**	**A0-A7**	**B0-B7**
Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B Data	L	H	↑	↑	X	X		
Store A, Hold B	X	H	↑	H or L	X	X	Input	Unspecified[1]
Store A in Both Registers	H	H	↑	↑	X[2]	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	Unspecified[1]	Input
Store B in Both Registers	L	L	↑	↑	X	X[2]	Output	Input
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored A Data to B Bus	H	H	H or L	X	H	X		
Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

Notes:

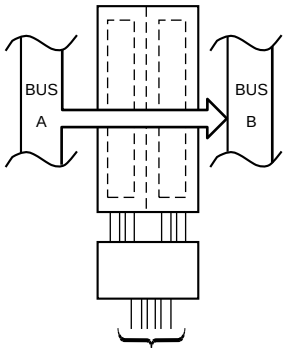
1. The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = LOW-to-HIGH transition

REAL-TIME TRANSFER
BUS B TO A



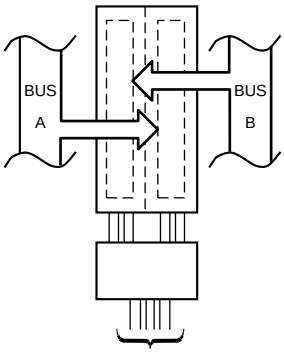
LPT646	**DIR**	**$\overline{G}$**	**CPAB**	**CPBA**	**SAB**	**SBA**
	L	L	X	X	X	L
LPT652	**GAB**	**$\overline{GBA}$**	**CPAB**	**CPBA**	**SAB**	**SBA**
	L	L	X	X	X	L

REAL-TIME TRANSFER
BUS A TO B



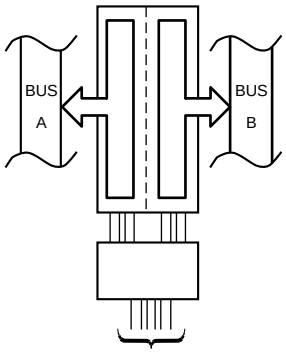
LPT646	**DIR**	**$\overline{G}$**	**CPAB**	**CPBA**	**SAB**	**SBA**
	H	L	X	X	L	X
LPT652	**GAB**	**$\overline{GBA}$**	**CPAB**	**CPBA**	**SAB**	**SBA**
	H	H	X	X	L	X

STORAGE FROM
A AND/OR B



LPT646	**DIR**	**$\overline{G}$**	**CPAB**	**CPBA**	**SAB**	**SBA**
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X
LPT652	**GAB**	**$\overline{GBA}$**	**CPAB**	**CPBA**	**SAB**	**SBA**
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X

TRANSFER STORES
DATA TO A AND/OR B



LPT646[(1)]	**DIR**	**$\overline{G}$**	**CPAB**	**CPBA**	**SAB**	**SBA**
	L	L	X	H or L	X	H
	H	L	H or L	X	H	X
LPT652	**GAB**	**$\overline{GBA}$**	**CPAB**	**CPBA**	**SAB**	**SBA**
	H	L	H or L	H or L	H	H

1. Note: The LPT646 cannot transfer data to A bus and B bus simultaneously.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{IH}	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level		2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)			2.0	—	5.5	V
V_{IL}	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_{IN} = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)	V_{CC} = Max.	V_{IN} = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Current (Input pins)	V_{CC} = Max.	V_{IN} = GND	—	—	±1	µA
	Input LOW Current (I/O pins)	V_{CC} = Max.	V_{IN} = GND	—	—	±1	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_{OUT} = 5.5V	—	—	±1	µA
I_{OZL}	(3-State Output pins)	V_{CC} = Max.	V_{OUT} = GND	—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1 mA	Vcc-0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3 mA	2.4	3.0	—	V
		V_{CC} = 3.0V,	I_{OH} = –8 mA	2.4[5]	3.0	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –24 mA	2.0	—	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1 mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	—	0.2	0.4	V
			I_{OL} = 24 mA	—	0.3	0.5	V
I_{OS}	Short Circuit Current[4]	V_{CC} = Max.[3], V_{OUT} = GND		–60	–85	–240	mA
I_{OFF}	Power Down Disable	V_{CC} = 0V, V_{IN} or V_{OUT} ≤ 4.5V		—	—	±100	µA
V_H	Input Hysteresis			—	150	—	mV

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} – 0.6V at rated current.

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[1]	Description	Test Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	pF

Note:
1. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	10	µA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]		2.0	30	µA
I_{CCD}	Dynamic Power Supply[4]	V_{CC} = Max., Outputs Open $\overline{G}$ = DIR = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10 MHz 50% Duty Cycle $\overline{G}$ = DIR = GND One Bit Toggling	V_{IN} = V_{CC} – 0.6V V_{IN} = GND		0.6	2.3	mA
		V_{CC} = Max., Outputs Open f_i = 2.5 MHz 50% Duty Cycle $\overline{G}$ = DIR = GND 8 Bits Toggling	V_{IN} = V_{CC} – 0.6V V_{IN} = GND		2.1	4.7[5]	

Notes:
1. ForMax. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_I)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_I = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

PI74LPT646 Switching Characteristics over Operating Range[1]

Parameters	Description	Conditions[2]	LPT646 Com. Min.[3]	LPT646 Com. Max.	LPT646A Com. Min.[3]	LPT646A Com. Max.	LPT646C Com. Min.[3]	LPT646C Com. Max.	Units
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	2.0	7.5	2.0	6.3	1.5	5.4	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{G}$, DIR to Bus		2.0	14.0	2.0	9.8	1.5	7.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{G}$, DIR to Bus		2.0	9.0	2.0	6.3	1.5	6.3	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus		2.0	9.5	2.0	7.7	1.5	6.2	ns
t_{SU}	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width[3] HIGH or LOW		6.0	—	5.0	—	5.0	—	ns

PI74LPT652 Switching Characteristics over Operating Range[1]

Parameters	Description	Conditions[2]	LPT652 Com. Min.[3]	LPT652 Com. Max.	LPT652A Com. Min.[3]	LPT652A Com. Max.	LPT652C Com. Min.[3]	LPT652C Com. Max.	Units
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	2.0	7.5	2.0	6.3	1.5	5.4	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{GBA}$, GAB to Bus		2.0	14.0	2.0	9.8	1.5	7.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{GBA}$, GAB to Bus		2.0	9.0	2.0	6.3	1.5	6.3	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus		2.0	9.5	2.0	7.7	1.5	6.2	ns
t_{SU}	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width[3] HIGH or LOW		6.0	—	5.0	—	5.0	—	ns

Notes:
1. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ±0.3V, normal range. For Vcc = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and waveforms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.